# USB 80G PHY Layer Analysis

USB-IF Electrical Workgroup

# Agenda

- Requirements
- Deriving FEC Characteristics
- Deriving Uncoded BER Specifications
- PHY Modulation Analysis

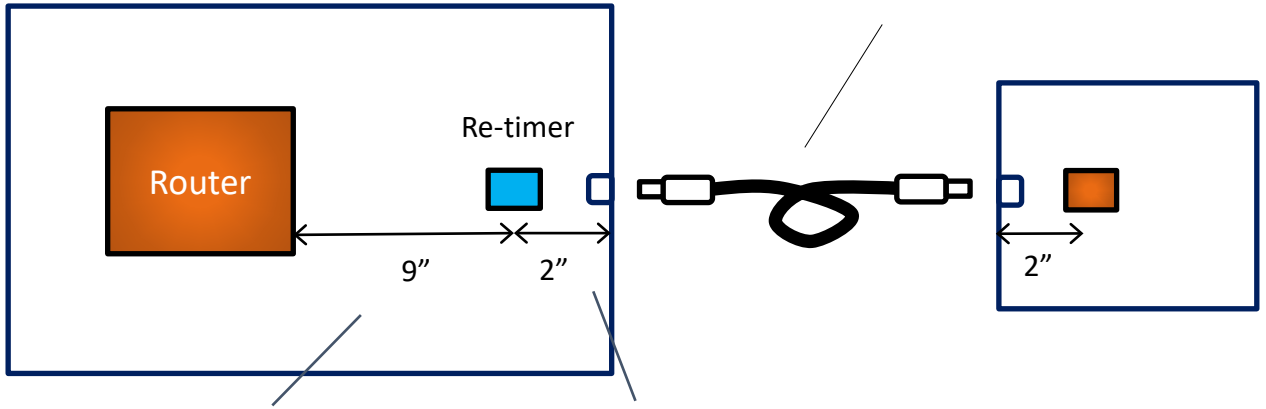
# Requirements

Goal: double USB4 link speed with the existing ecosystem constraints

- **Data Rate:** 80G gross rate with traffic available bandwidth ≥76Gb/s
- **Data Integrity:** BER <1E-19
- **Latency:** FEC latency <150ns
- **USB-C Compatibility:** Same cables, connectors, and PCB as in USB 40G

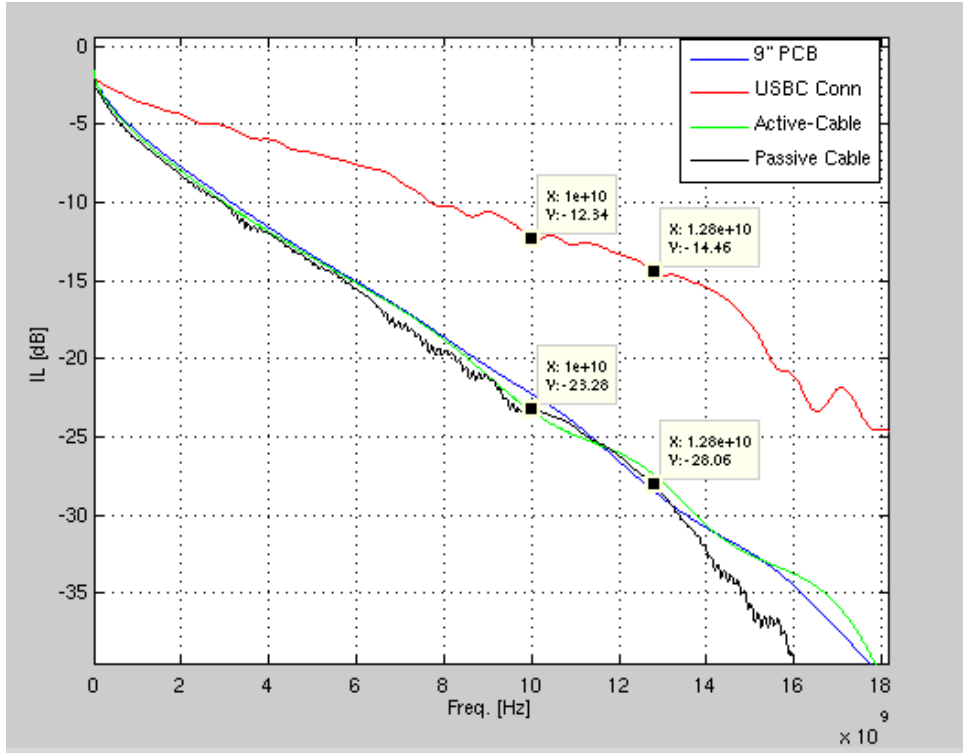
# USB-C Channels

**Active-Cable (2m) end-end channel:**
**24dB @ 10GHz; 47dB @ 20GHz**
**Passive-Cable (0.8m) end-end channel:**
**23dB @ 10GHz; 48dB @ 20GHz**

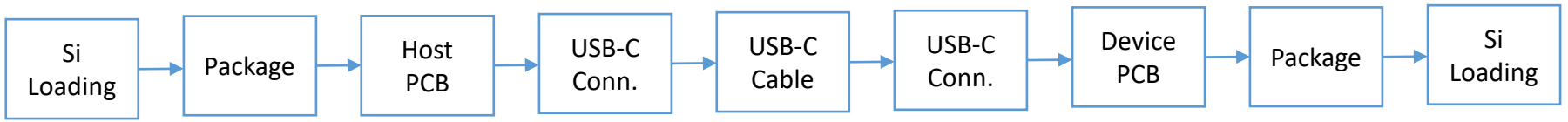



**PCB end-end channel:**
**22dB @ 10GHz; 49dB @ 20GHz**

**Retimer to Near Plug:**
**12dB @ 10GHz; 28dB @ 20GHz**

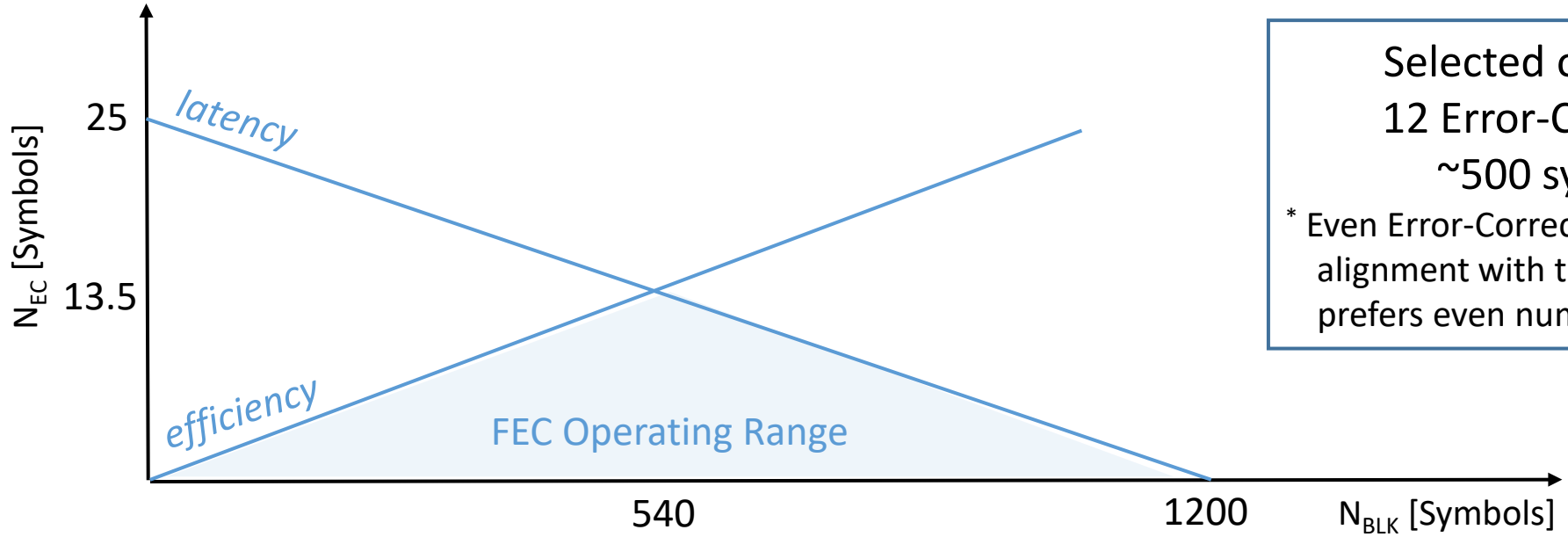



- Worst-Case reference model:



# RS-FEC Specifications

- RS-FEC requirements for meeting BW efficiency and latency specs:
  **(*) Latency ≤ 150ns** → $N_{BLK}*10*12.5ps + N_{EC}*6ns \leq 150ns$
  **(**) Efficiency ≥ 95%** → $2*N_{EC}/N_{BLK} \leq 0.05$
  // $N_{BLK}$ is the block size, $N_{EC}$ is the number of error-corrections per block
  // Assumptions: 10 bits per symbols; 6ns per error correction




Selected operating point:
12 Error-Corrections over
~500 symbols Block
* Even Error-Corrections number selected in alignment with the error statistics which prefers even numbers (see backup slide)

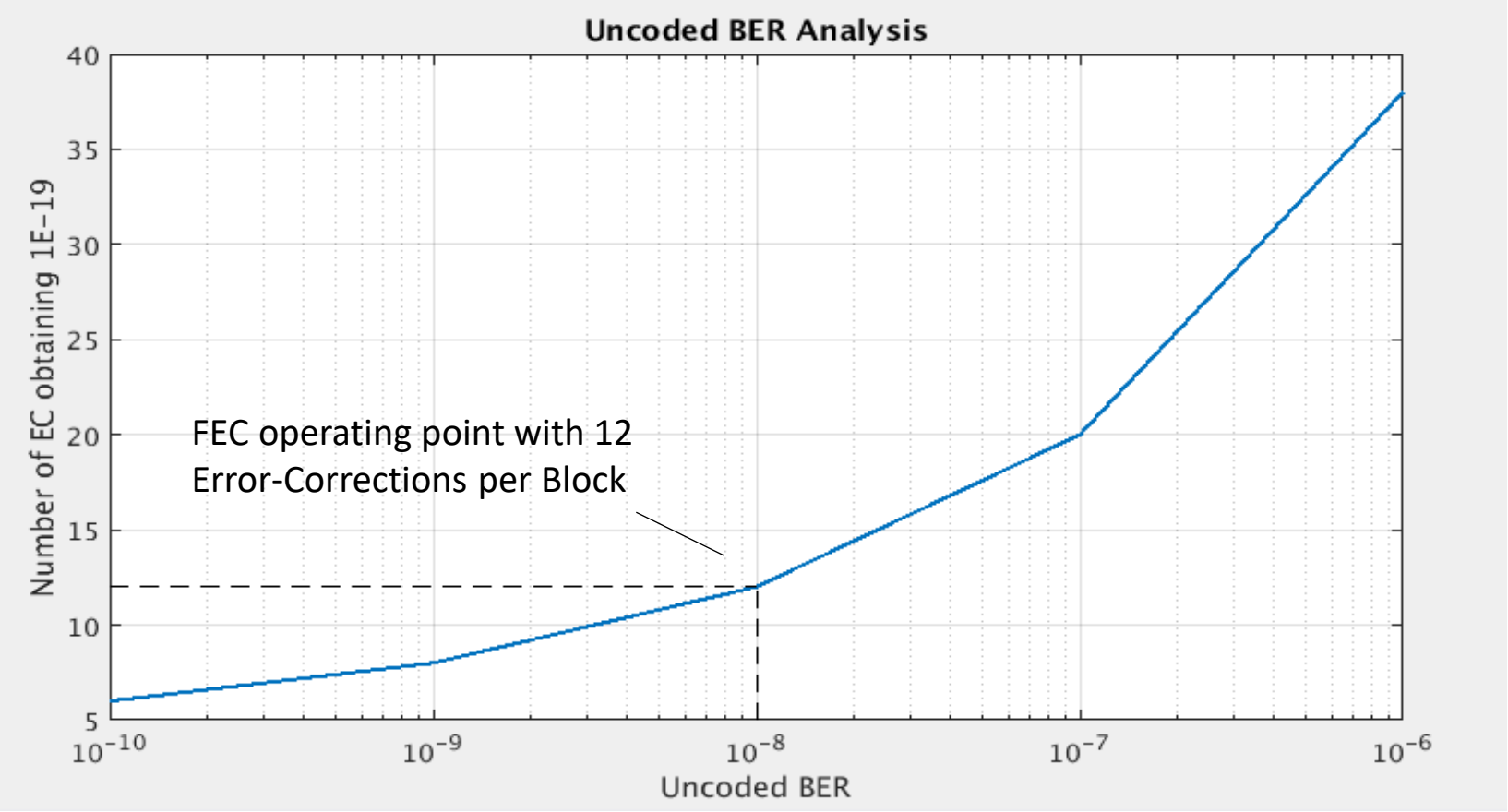
# Deriving the Uncoded BER Specifications (1)

- Analysis performed for deriving the relation between the uncoded BER and the FEC error corrections, given coded BER of 1E-19
- The calculation includes the following parameters:
  - Number of Error corrections
  - Uncoded BER (uncorrelated errors)
  - Block Size
  - RS symbol size
  - Pre-coding (“integrative” pre-coder addressing DFE error bursts)
  - Number of Re-timers
  - DFE error propagation probability
  - Burst restart probability (probability that a burst which ended will restart)

# Deriving the Uncoded BER Specifications (2)

- The analysis defines the required number of error corrections per different input BER levels such that: $10^{-19} > \frac{1}{N_{BLK}} \cdot \sum_i \{FEC\ failure\ event_i\}$
- "Safe zone" between the FEC input BER and the PHY uncoded BER added for budgeting correlated error effects that cannot be modeled and obtaining margin in the system level
  - Experience from the Networking segment indicates that most of the Ethernet vendors require 2.4 orders of magnitude as "safe zone" margin
  - In this work, 2 orders of magnitude are assumed (although USB segment has more interop challenges due to its huge volumes and large variety of multi-vendor links)

# Deriving the Uncoded BER Specifications (3)




Uncoded BER=1E-8 shall be targeted for enabling FEC with 12 Error-Corrections

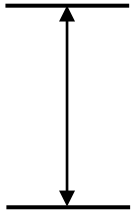
# PHY Modulation Analysis

- PAM-3 and PAM-4 modulations were examined using USB-C channel models
  - PAM-2 is not applicable as the frequency is too high; non-differential methods also examined but not applicable due to the mode conversion of the connector

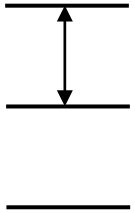
| Modulation | Baud Rate [GB] | Levels Separation | Comments |
|---|---|---|---|
| PAM-3 | 25.6 | 0.5 | Each symbol carries 1.57 bits(1) |
| PAM-4 | 20.0 | 0.33 | Each symbol carries 2 bits |

(1) Realized by a simple 11bits-to-7trits mapping obtaining >99% efficiency of the theoretical log2(3)=1.58 bits/symbol limit

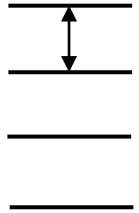
**PAM-2**
1bit/Symbol
Rate: 40GB
Margin: 1



**PAM-3**
1.57bits/Symbol
Rate: 25.6GB
Margin: 0.5



**PAM-4**
2bits/Symbol
Rate: 20GB
Margin: 0.33



# USB Reference Channels: Background

- Each end-to-end channel model consists of five models corresponding to sections of USB end-to-end channel, as shown below:

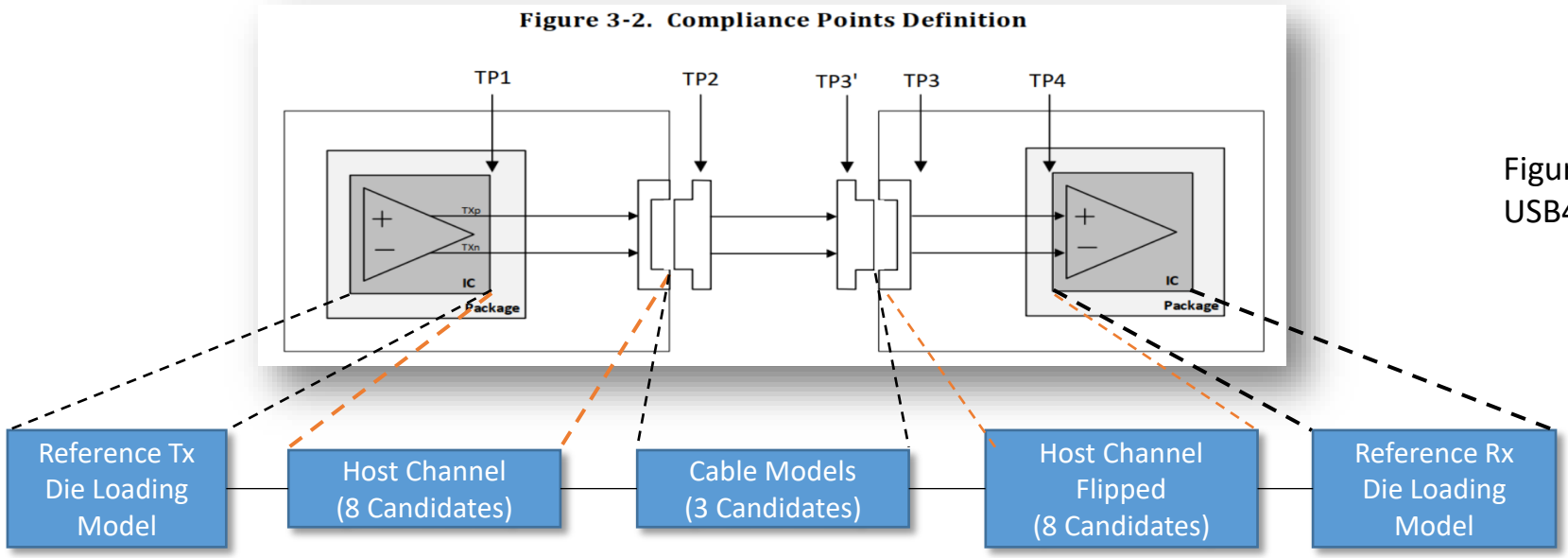
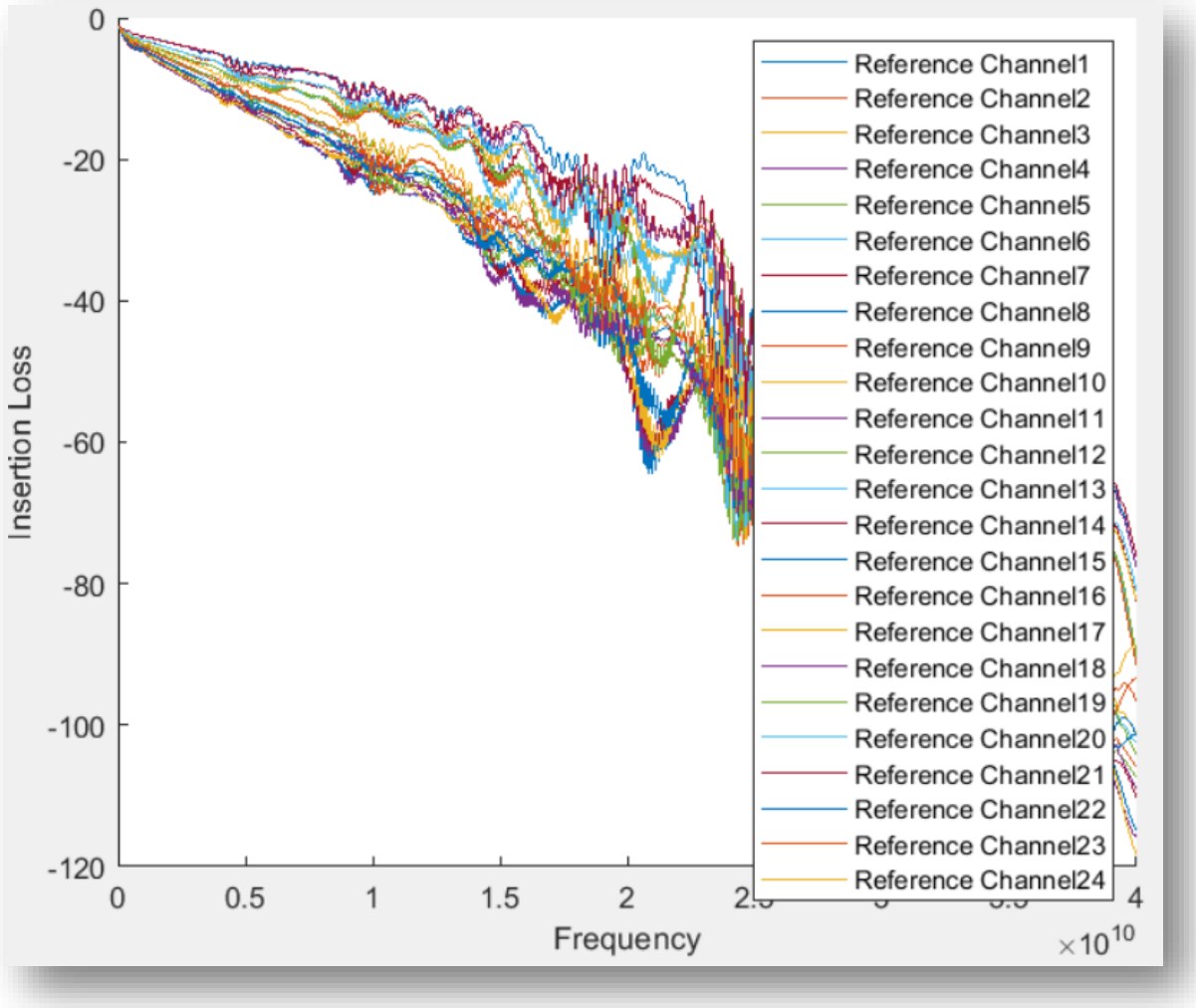



Figure 3-2
USB4™ Spec

# End-to-End Channel Characteristics: IL

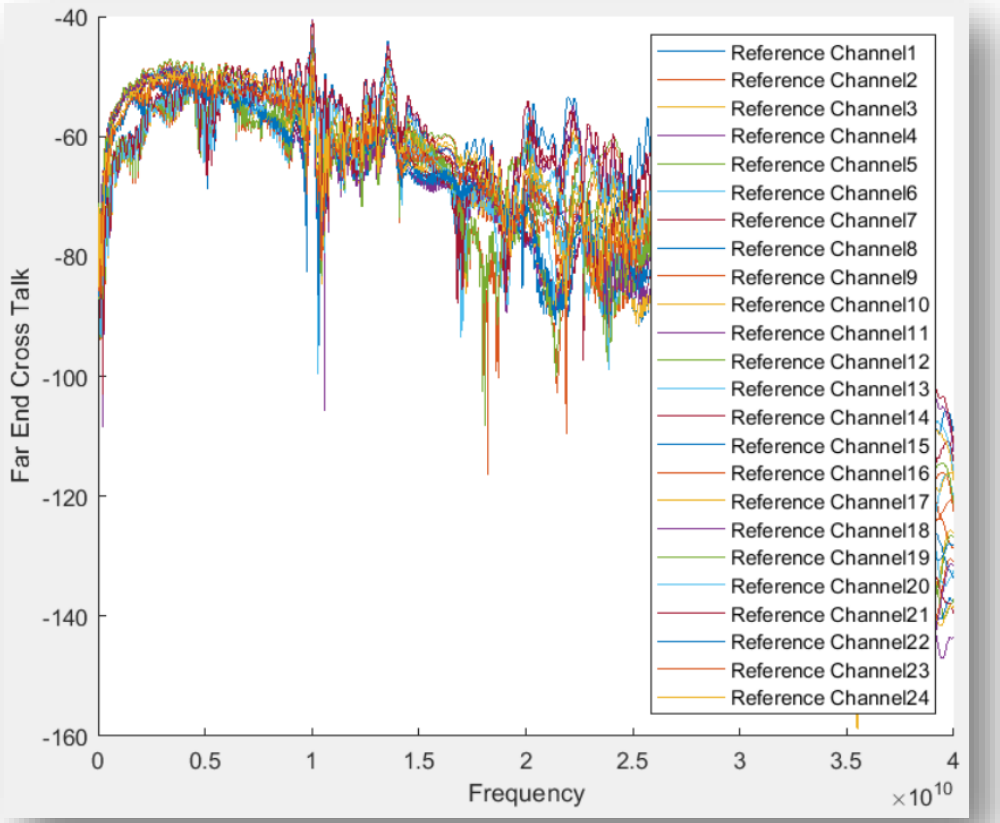
| End-to-end Channel | IL Fit @ 12.8GHz [dB] | IL Fit @ 10.0GHz [dB] |
|---|---|---|
| 1 | -29.40 | -23.55 |
| 2 | -27.67 | -22.14 |
| 3 | -25.61 | -20.14 |
| 4 | -29.27 | -23.53 |
| 5 | -27.54 | -22 |
| 6 | -25.53 | -20.13 |
| 7 | -27.66 | -22.44 |
| 8 | -25.93 | -20.92 |
| 9 | -24.01 | -19.06 |
| 10 | -27.66 | -22.55 |
| 11 | -25.94 | -21.03 |
| 12 | -23.99 | -19.03 |

| End-to-end Channel | IL Fit @ 12.8GHz [dB] | IL Fit @ 10.0GHz [dB] |
|---|---|---|
| 13 | -18.55 | -13.09 |
| 14 | -16.78 | -11.09 |
| 15 | -14.45 | -14.93 |
| 16 | -18.71 | -13.38 |
| 17 | -16.94 | -11.38 |
| 18 | -14.61 | -14.63 |
| 19 | -18.27 | -13.08 |
| 20 | -16.5 | -11.08 |
| 21 | -14.17 | -20.74 |
| 22 | -25.98 | -19.32 |
| 23 | -24.50 | -17.32 |
| 24 | -22.18 | -13.09 |

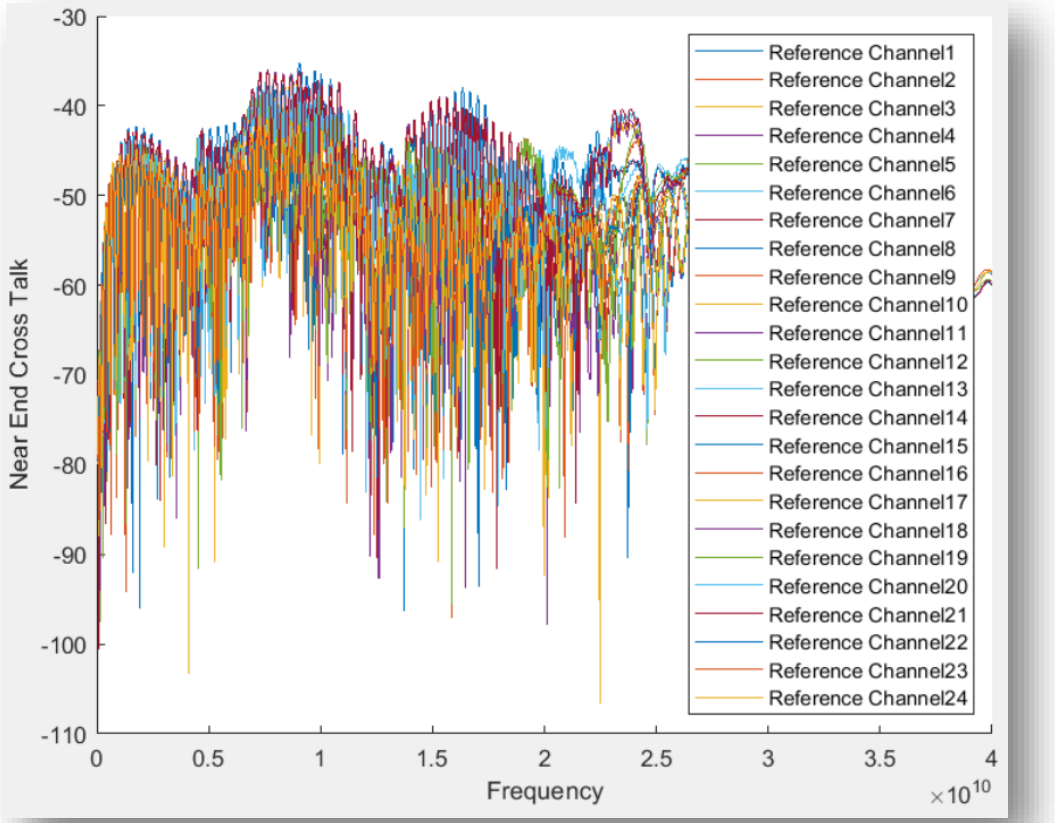


# End-to-End Channel Characteristics: XTALK

## Far-End Cross Talk

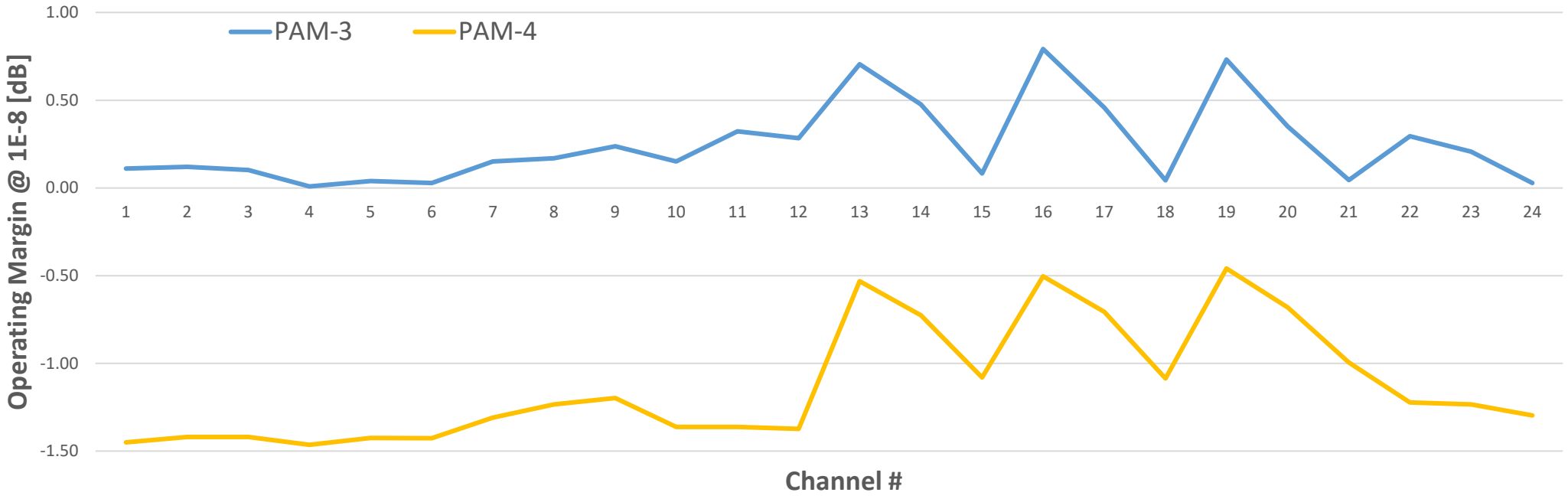



## Near-End Cross Talk



# Simulations Results: Summary

- Simulations were performed using eCOM analysis tool (details below)
- PAM-3 modulation was identified as the only direction that enables supporting un-coded BER of 1E-8



# Simulations Results: Details

- Simulations results over 24 reference USB Type-C channels:

**PAM3**

| | Host | 1 | | | 2 | | | 3 | | | 4 | | | 5 | | | 6 | | | 7 | | | 8 | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Cable | 1 | 4 | 7 | 1 | 4 | 7 | 1 | 4 | 7 | 1 | 4 | 7 | 1 | 4 | 7 | 1 | 4 | 7 | 1 | 4 | 7 | 1 | 4 | 7 |
| Operating Margin [dB] | 1.0E-08 | 0.11 | 0.12 | 0.10 | 0.01 | 0.04 | 0.03 | 0.15 | 0.17 | 0.24 | 0.15 | 0.32 | 0.28 | 0.71 | 0.48 | 0.08 | 0.79 | 0.46 | 0.04 | 0.73 | 0.35 | 0.04 | 0.30 | 0.21 | 0.03 |
| | 1.0E-07 | 0.67 | 0.68 | 0.66 | 0.57 | 0.60 | 0.59 | 0.70 | 0.73 | 0.79 | 0.70 | 0.87 | 0.83 | 1.23 | 1.01 | 0.62 | 1.32 | 0.98 | 0.58 | 1.25 | 0.86 | 0.58 | 0.85 | 0.77 | 0.58 |
| | 1.0E-06 | 1.32 | 1.35 | 1.33 | 1.22 | 1.26 | 1.24 | 1.34 | 1.37 | 1.45 | 1.33 | 1.50 | 1.47 | 1.87 | 1.64 | 1.25 | 1.94 | 1.61 | 1.20 | 1.86 | 1.48 | 1.21 | 1.50 | 1.42 | 1.24 |

**PAM4**

| | Host | 1 | | | 2 | | | 3 | | | 4 | | | 5 | | | 6 | | | 7 | | | 8 | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Cable | 1 | 4 | 7 | 1 | 4 | 7 | 1 | 4 | 7 | 1 | 4 | 7 | 1 | 4 | 7 | 1 | 4 | 7 | 1 | 4 | 7 | 1 | 4 | 7 |
| Operating Margin [dB] | 1.0E-08 | -1.45 | -1.42 | -1.42 | -1.47 | -1.43 | -1.43 | -1.31 | -1.23 | -1.20 | -1.36 | -1.36 | -1.37 | -0.53 | -0.73 | -1.08 | -0.50 | -0.71 | -1.09 | -0.46 | -0.68 | -1.00 | -1.22 | -1.23 | -1.30 |
| | 1.0E-07 | -0.87 | -0.85 | -0.84 | -0.88 | -0.85 | -0.85 | -0.73 | -0.67 | -0.62 | -0.79 | -0.79 | -0.80 | 0.03 | -0.17 | -0.52 | 0.07 | -0.14 | -0.52 | 0.11 | -0.12 | -0.44 | -0.65 | -0.66 | -0.72 |
| | 1.0E-06 | -0.18 | -0.17 | -0.16 | -0.19 | -0.17 | -0.17 | -0.04 | 0.00 | 0.05 | -0.12 | -0.12 | -0.13 | 0.68 | 0.47 | 0.13 | 0.73 | 0.51 | 0.13 | 0.76 | 0.54 | 0.22 | 0.03 | 0.02 | -0.05 |

# Summary

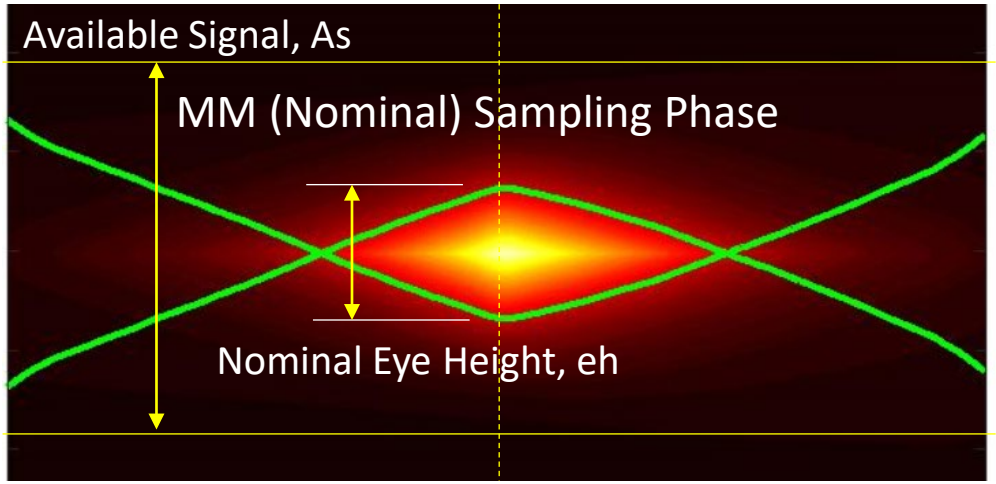
- Different modulation technologies were examined for meeting the goal of doubling USB link speed with the existing ecosystem constraints
- The analysis indicates that PAM-3 is the only modulation technology that supports un-coded BER<1E-8, which meets USB 80G goals
  - Meaningfully better performance than all other options over USB channels
  - PHY architecture/design is similar between PAM-3/PAM-4 (PAM-3 slightly simpler)
  - PAM-3 is a novel direction, yet test equipment already available

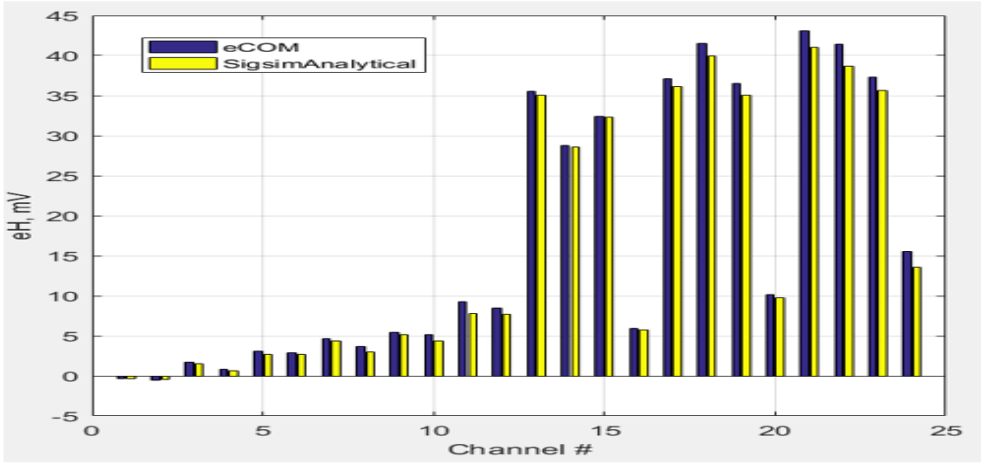
# Performance Analysis Details

# Analysis Method: eCOM Tool Background

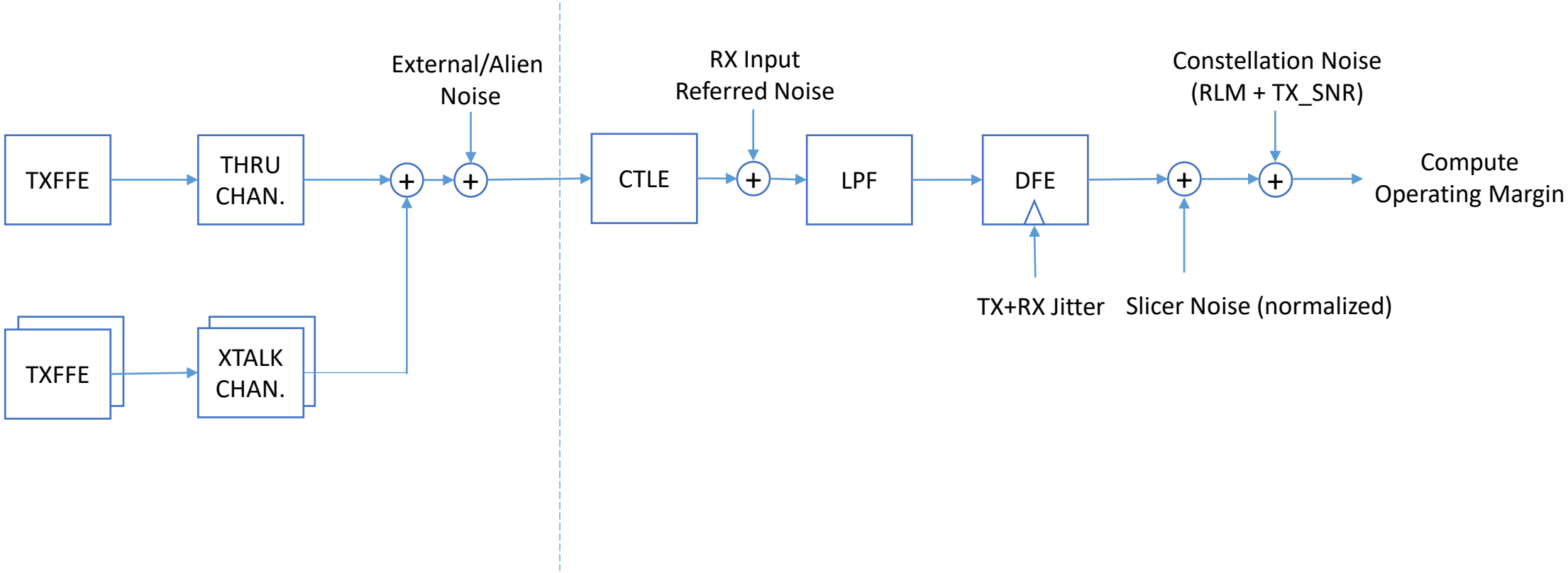
$$eCOM = 20 * log10(\frac{A_s}{A_s - eh})$$

- eCOM, or enhanced COM is developed based on the COM industry tool, which is widely used in the Ethernet segment.
- eCOM adds all Rx impairments such that the pass/fail criterion is eCOM = 0 dB
  - COM includes mostly Tx impairments.
- eCOM handles jitter more rigorously
  - COM uses the pulse response slope to approximate jitter impact, which may cause significant error when jitter is not small.
- eCOM has been correlated with TD simulations and with other statistical analysis tools.



# eCOM Reference Model



# Simulation Setup (1)

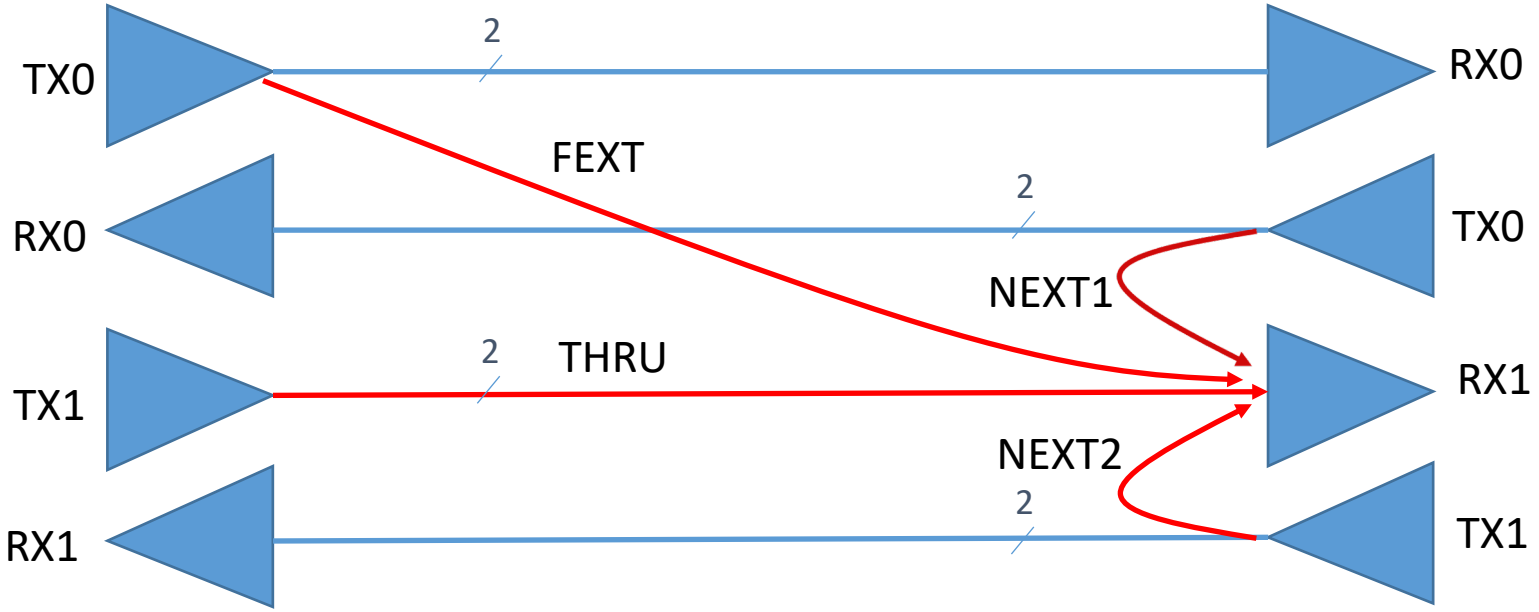
| Parameter | PAM-3 | PAM-4 |
|---|---|---|
| Baud Rate | 25.6GB | 20.0GB |
| Channel | THRU, FEXT, 2 x NEXT | THRU, FEXT, 2 x NEXT |
| TX Voltage Swing | 0.8V pk-pk | 0.8V pk-pk |
| FEXT Voltage Swing | 0.8V pk-pk | 0.8V pk-pk |
| NEXT Voltage Swing | 1V pk-pk | 1V pk-pk |
| Rise Time | 8ps | 8ps |
| TXFFE Configuration | LSB: $C_{-2}$=0.025 $C_{-1}/C_1$=0.05 | LSB: $C_{-2}$=0.025 $C_{-1}/C_1$=0.05 |
| TX Uncorrelated DJ | 0.08UI pk-pk | 0.0625UI pk-pk |
| TX RJ | 0.0075UI rms | 0.0075UI rms |
| TX Levels Mismatch | 0.975 | 0.95 |
| TX SNDR | 32.5dB | 32.5dB |
| Alien Noise (AWGN) | 1.64E-8 $V^2$/GHz | 1.64E-8 $V^2$/GHz |

# Simulation Setup (2)

| Parameter | PAM-3 | PAM-4 |
|---|---|---|
| CTLE Stage1 pole | Fbaud/2.5 | Fbaud/2.5 |
| CTLE Stage1 boost | -12:1:0 dB | -12:1:0 dB |
| CTLE Stage2 pole | Fbaud/80 | Fbaud/80 |
| CTLE Stage2 boost | -6:1:0 dB | -6:1:0 dB |
| RX BW | 0.75*Fbaud | 0.75*Fbaud |
| DFE taps | 12 | 12 |
| RX DJ (open loop) | 0.032UI pk-pk | 0.025UI pk-pk |
| RX RJ (open loop) | 0.0075UI rms | 0.0075UI rms |
| RX CDR tracking jitter | 0.01UI rms | 0.01UI rms |
| RX Amp. Input Referred Noise | 1.3E-8 $V^2$/GHz | 1.3E-8 $V^2$/GHz |
| Random Noise at RX Slicer | 2.23mV rms | 2.23mV rms |
| Deterministic Noise at RX slicer | 10.3mV pk | 8.5mV pk |

# Channel Models

- Thru differential channel
- 1 FEXT differential channel
- 2 NEXT differential channels



# Transmitter Reference Model: Baseline

- Baud Rate: 20.0GB (PAM-4), 25.6GB (PAM-3)
  - PAM-3: 1.57 bits/symbol, PAM-4: 2 bits/symbol
- TX Voltage Swing:
  - THRU: 0.8V pk-pk
  - FEXT: 0.8V pk-pk
  - NEXT: 1V pk-pk

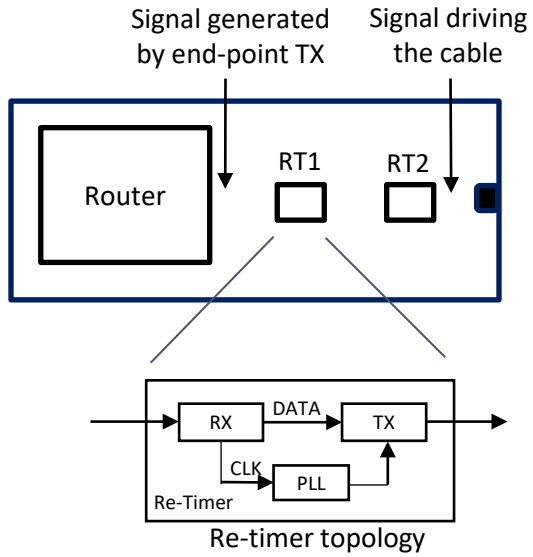
Far-side with minimum transmitter swing (THRU+FEXT)
Near side with maximum transmitter swing (NEXT)

- TX FFE:
  - 4 FIR taps (2 pre-cursor and 1 post-cursor taps)
  - 0.05 LSB step for taps C[-1], C[1]; 0.025 LSB step for tap C[-2]; $\sum|C[i]|=1$
  - Same as IEEE Ethernet standards

# Transmitter Reference Model: Jitter

- Deterministic Jitter: 3.125ps pk-pk (2.3ps UDJ, 0.8ps TX DCD)
  - 0.08UI pk-pk (PAM-3), 0.0625UI pk-pk (PAM-4)

| |
|---|
| • TX+PLL circuitry: 1.9ps pk-pk<br>• Residual SSC: 0.4ps pk-pk<br>• Re-timer's PLL noisy refclk: 0.2ps pk-pk<br>• Low frequency jitter forwarding: 2 x 0.3ps = 0.6ps pk-pk |



Re-timer topology

- Random Jitter: 0.0075UI RMS

| |
|---|
| • The phase noise scales with the rate (constant in radians) |

# Transmitter Reference Model: Voltage Noise

- Levels Mismatch (R_LM): 0.975 (PAM-3), 0.95 (PAM-4)
  - PAM-4 R_LM is the same as IEEE Ethernet standards, PAM-3 R_LM assumes the same level mismatch error as PAM-4 plus some additional benefit of its symmetrical structure:
    - The R_LM error (=1-R_LM) is the ratio between the levels differential mismatch and the ideal levels difference. Since in PAM-3 the ideal levels difference is 1.5x larger than in PAM-4, same amount of mismatch will translate into 1.5x smaller R_LM error
    - PAM-3 has symmetrical structure which decreases the levels differential mismatch compared to PAM-4 (PAM-3 inner level is generated by applying the same voltage on TXp and TXn providing better impedance matching than PAM-4 where TXp≠TXn)
- Dynamic Non-Linearity (TX_SNDR): 32.5dB
  - Same as IEEE Ethernet standards
  - It shall be noted that the USB setup is more challenging due to the tighter power and noise levels constraints

# RX Reference Model: Jitter

- RX DJ (open loop): 1.25ps pk-pk
  - 0.032UI pk-pk (PAM-3), 0.025UI pk-pk (PAM-4)
  - Not including the CDR tracking jitter

- RX RJ: 0.0125UI RMS

  - CDR loop tracking jitter modeled with 0.01UI RMS Gaussian PDF (scales with the rate)
  - Phase noise: 0.0075UI RMS (scales with the rate)

# RX Reference Model: Equalization

- CTLE:

$$H(s) = \frac{(s + 2\pi f_{LP} \cdot A_{DC\_LP})}{(s + 2\pi f_{LP})} \cdot \frac{f_{p1} \cdot (s + 2\pi f_{z1} \cdot A_{DC\_1})}{f_{z1} \cdot (s + 2\pi f_{p1})} \cdot \frac{2\pi f_{p2}}{(s + 2\pi f_{p2})}$$

Nominal setting: $f_{LP}=F_{baud}/80$

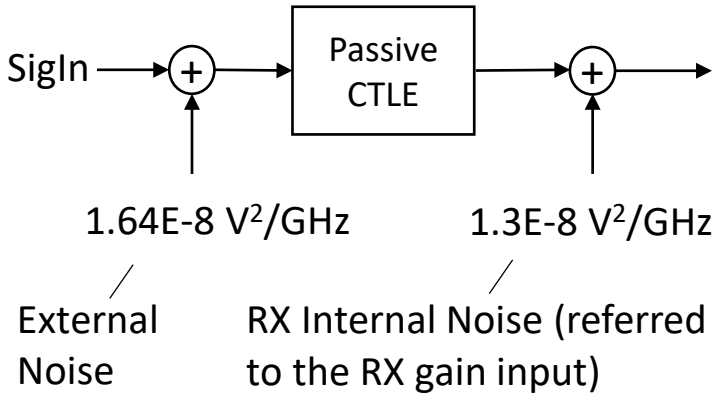
Nominal setting: $f_{p1}=f_{z1}=F_{baud}/2.5$

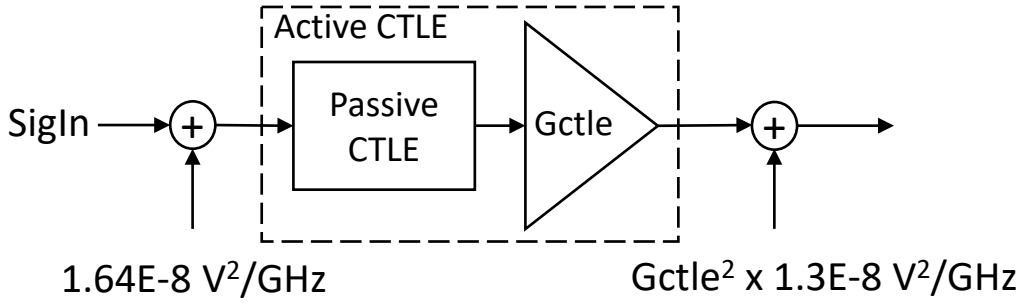
Nominal setting: $f_{p2}=F_{baud}$

- Receiver bandwidth limitation: 4 poles at $0.75*F_{baud}$
- DFE: 12 taps
  - Taps Range (normalized to the cursor): tap1: 0 – 0.75, tap2-12: -0.2 – 0.2
  - The DFE quantization error is represented by Gaussian noise with σ=1mV at the slicer input (and normalized back to the CTLE output by eCOM)
    - Assuming 1mV DFE tap resolution, the quantization error is uniformly distributed between [-0.5mV, 0.5mV]. Therefore, the RMS error per tap is of 1/sqrt(12) mV, and the total RMS error for 12 independent taps is of 1/sqrt(12) x sqrt(12) = 1mV (PDF is close to be Gaussian)

# RX Reference Model: Additive Noise

- External/Alien noise (spectral density): 1.64E-8 $V^2$/GHz
  - Same as IEEE Ethernet Standards
- RX internal noise (spectral density): 1.3E-8 $V^2$/GHz
  - Modeling the added thermal noise of the receiver gain stages
  - The input referred noise associated with the receiver gain stages is almost independent of the specific receiver design as it is mostly dominated by the noise of the first stage only



# RX Reference Model: Slicer Noise

- Slicer Sensitivity: 5mV peak (PAM-3), 4mV peak (PAM-4)
  - Assumed to be slightly lower for PAM-4 due to the larger decision time
  - Eye width (integration window) is higher in PAM-3
- Slicer Offset: 3mV peak
  - Accounted for slicer calibration inaccuracies and temperature related offsets
- Slicer AWGN: 2.2mV RMS
  - Latch noise: 2mV RMS
  - DFE finite tap resolution: 1mV RMS

# RX Reference Model: Non-Linearity

- Non-Linearity Effects: 2.3mV peak (PAM-3), 1.5mV peak (PAM-4)

  - Values are based on simulation data
  - PAM-4 is more sensitive to non-linearity effects as its constellation being impacted by both the DFE taps and the AGC gain distortion while PAM-3 constellation is impacted only by the DFE taps error
  - On the other hand, the DFE dynamic range tends to be smaller in PAM-4 compared to PAM-3 as the Nyquist insertion-loss is smaller

# eCOM Simulation Setup: PAM3

| System Level Settings | | | |
|---|---|---|---|
| **Parameter** | **Setting** | **Units** | **Information** |
| IO_interface | CIO80 | | Interface tag |
| f_b | 25.6 | GBd | Baud Rate |
| L | 3 | | Number of constallation levels |
| DER_0 | 1.00E-08 | | Target uncoded symbol error rate |
| COM Pass threshold | 0 | dB | 0 dB for CIO80. 3 dB for IEEE standards |
| **TX EQ Settings** | | | |
| ffe_preset | ).025 -0.2 -0.1;0.025 -0.2 - | | TXFFE preset configurations |
| **RX EQ Settings** | | | |
| g_DC | [-12:1:0] | dB | CTLE stage1 (high pole) DC attenuation |
| g_DC_HP | [-6:1:0] | | CTLE stage2 (low pole) DC attenuation |
| f_HP_PZ | 0.32 | GHz | CTLE stage2 pole location |
| f_z | 10.24 | GHz | CTLE stage1 zero location |
| f_p1 | 10.24 | GHz | CTLE stage1 first pole location |
| f_p2 | 25.6 | GHz | CTLE stage1 second pole location |
| N_b | 12 | UI | Number of DFE taps |
| b_max(1) | 0.75 | | Dynamic range limitation for the DFE first tap (referenced to the main cursor) |
| b_max(2..N_b) | 0.2 | | Dynamic range limitation for the DFE taps 2 and above (referenced to the main cursor) |
| **TX and RX Jitter** | | | |
| A_DDtx | 0.0128 | UI | Transmitter bimodal jitter |
| sigma_RJtx | 0.0075 | UI | Transmitter RJ RMS |
| SJtx | 0.0272 | UI | Transmitter sinusoidal jitter |
| A_DDrx | 0.016 | UI | Receiver bi-modal jitter |
| sigma_RJrx | 0.0125 | UI | Receiver RJ RMS |
| **TX and RX Noise** | | | |
| SNR_TX | 32.5 | dB | Transmitter dynamic non-linearity: same as IEEE 802.3cd (latest Ethernet spec) |
| eta_0 | 1.64E-08 | V^2/GHz | External/Alien noises: same as IEEE 802.3cd (latest Ethernet spec) |
| eta_rx | 1.30E-08 | V^2/GHz | AFE input referred AWGN (post CTLE) |
| slc_awgn | 1.86E-02 | | Rx Gaussian noise ratio (to Vref). Actual noise = X * Cursor. |
| slc_det_noise | 0.085833333 | | Receiver deterministic noise ratio (to Vref): 5mV slicer sensitivity plus 3mV slicer offset plus 2.3mV non-linearity (referenced to +/-120mV slicer dynamic range). =0.0858333 for |
| **Swing and R_LM** | | | |
| A_v | 0.4 | V | THRU transmitter peak voltage swing |
| A_fe | 0.4 | V | FEXT aggressor peak voltage swing |
| A_ne | 0.5 | V | NEXT aggressor peak voltage swing |
| R_LM | 0.975 | | Transmitter static non-linearity: based on IEEE 802.3cd (latest Ethernet spec) |
| **TX and RX Filter** | | | |
| T_r | 8.00E-03 | ns | Rise time, used to apply a Tx filter |
| f_r | 0.75 | *fb | Receiver bandwidth |
| INCLUDE_TX_RX_FILTER | 1 | logical | |

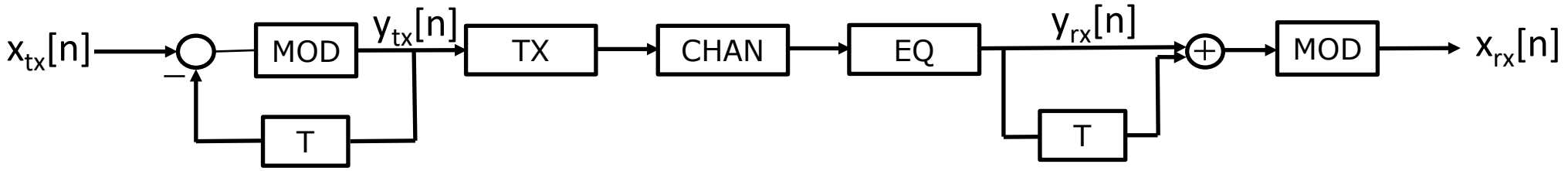
# eCOM Simulation Setup: PAM4

| System Level Settings | | | |
|---|---|---|---|
| **Parameter** | **Setting** | **Units** | **Information** |
| IO_interface | CIO80 | | Interface tag |
| f_b | 20 | GBd | Baud Rate |
| L | 4 | | Number of constallation levels |
| DER_0 | 1.00E-08 | | Target uncoded symbol error rate |
| COM Pass threshold | 0 | dB | 0 dB for CIO80. 3 dB for IEEE standards |
| **TX EQ Settings** | | | |
| ffe_preset | 0.025 -0.2 -0.1;0.025 -0.2 - | | TXFFE preset configurations |
| **RX EQ Settings** | | | |
| g_DC | [-12:1:0] | dB | CTLE stage1 (high pole) DC attenuation |
| g_DC_HP | [-6:1:0] | | CTLE stage2 (low pole) DC attenuation |
| f_HP_PZ | 0.25 | GHz | CTLE stage2 pole location |
| f_z | 8 | GHz | CTLE stage1 zero location |
| f_p1 | 8 | GHz | CTLE stage1 first pole location |
| f_p2 | 20 | GHz | CTLE stage1 second pole location |
| N_b | 12 | UI | Number of DFE taps |
| b_max(1) | 0.75 | | Dynamic range limitation for the DFE first tap (referenced to the main cursor) |
| b_max(2..N_b) | 0.2 | | Dynamic range limitation for the DFE taps 2 and above (referenced to the main cursor) |
| **TX and RX Jitter** | | | |
| A_DDtx | 0.01 | UI | Transmitter bimodal jitter |
| sigma_RJtx | 0.0075 | UI | Transmitter RJ RMS |
| SJtx | 0.02125 | UI | Transmitter sinusoidal jitter |
| A_DDrx | 0.0125 | UI | Receiver bi-modal jitter |
| sigma_RJrx | 0.0125 | UI | Receiver RJ RMS |
| **TX and RX Noise** | | | |
| SNR_TX | 32.5 | dB | Transmitter dynamic non-linearity: same as IEEE 802.3cd (latest Ethernet spec) |
| eta_0 | 1.64E-08 | V^2/GHz | External/Alien noises: same as IEEE 802.3cd (latest Ethernet spec) |
| eta_rx | 1.30E-08 | V^2/GHz | AFE input referred AWGN (post CTLE) |
| slc_awgn | 1.86E-02 | | Rx Gaussian noise ratio (to Vref). Actual noise = X * Cursor. |
| slc_det_noise | 0.070833333 | | Receiver deterministic noise ratio (to Vref): 5mV slicer sensitivity plus 3mV slicer offset plus 2.3mV non-linearity (referenced to +/-120mV slicer dynamic range). |
| **Swing and R_LM** | | | |
| A_v | 0.4 | V | THRU transmitter peak voltage swing |
| A_fe | 0.4 | V | FEXT aggressor peak voltage swing |
| A_ne | 0.5 | V | NEXT aggressor peak voltage swing |
| R_LM | 0.95 | | Transmitter static non-linearity:same as IEEE 802.3cd (latest Ethernet spec) |
| **TX and RX Filter** | | | |
| T_r | 8.00E-03 | ns | Rise time, used to apply a Tx filter |
| f_r | 0.75 | *fb | Receiver bandwidth |
| INCLUDE_TX_RX_FILTER | 1 | logical | |

# Backup

# Pre-Coding (PAM-N)

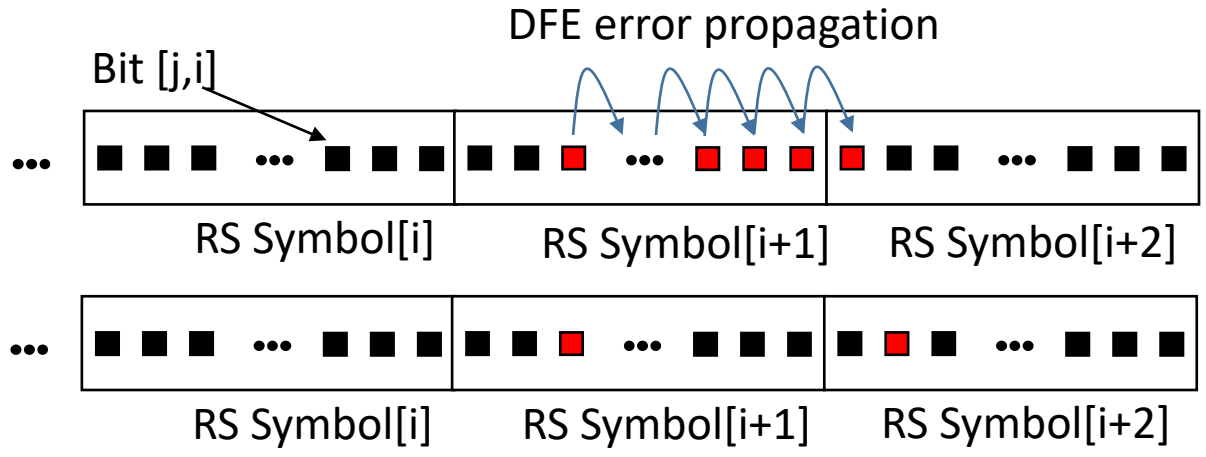
- Functionality:
  - Encoding: y[n] = MOD(-y[n-1] + x[n],N) = -y[n-1] + x[n] + a*N // x, y ∈ {0,1,..,N-1}; a ∈ Z
  - Decoding: MOD(y[n] + y[n-1], N) = MOD(-y[n-1] + x[n] + a*N + y[n-1], N) = x[n]




- Provides mitigation for DFE error propagation effects:
  - if $y_{rx}[n-1]=y_{tx}[n-1] \pm 1$ then the DFE correction for the next symbol will create error at the opposite direction such that $y_{rx}[n]=y_{tx}[n] \mp 1$ (assuming DFE tap1>0).

    Therefore: MOD(y[n]±1 + y[n-1]∓1, N) = MOD(y[n] + y[n-1], N) = x[n]

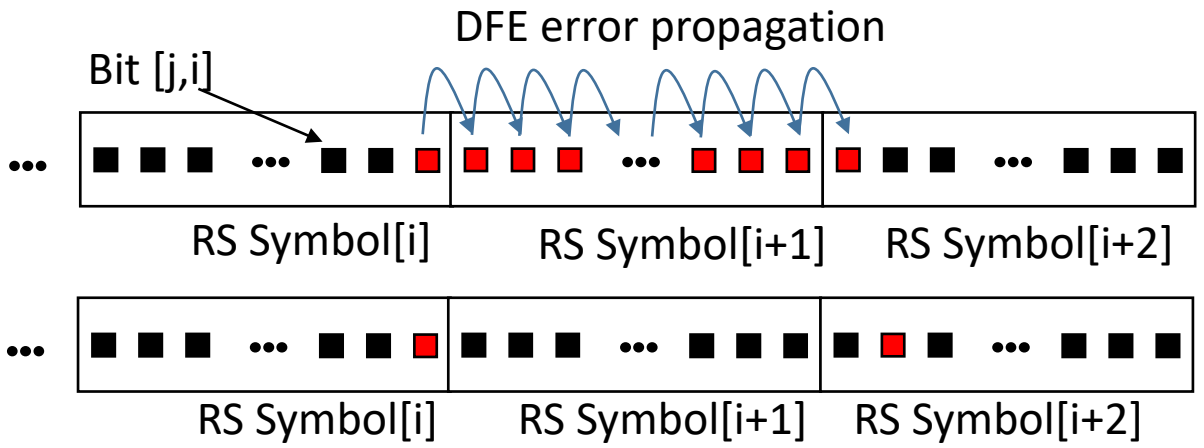
# Pre-Coding (PAM-N) (cont'd)




Without Pre-Coding (2 RS errors)




With Pre-Coding (2 RS errors)



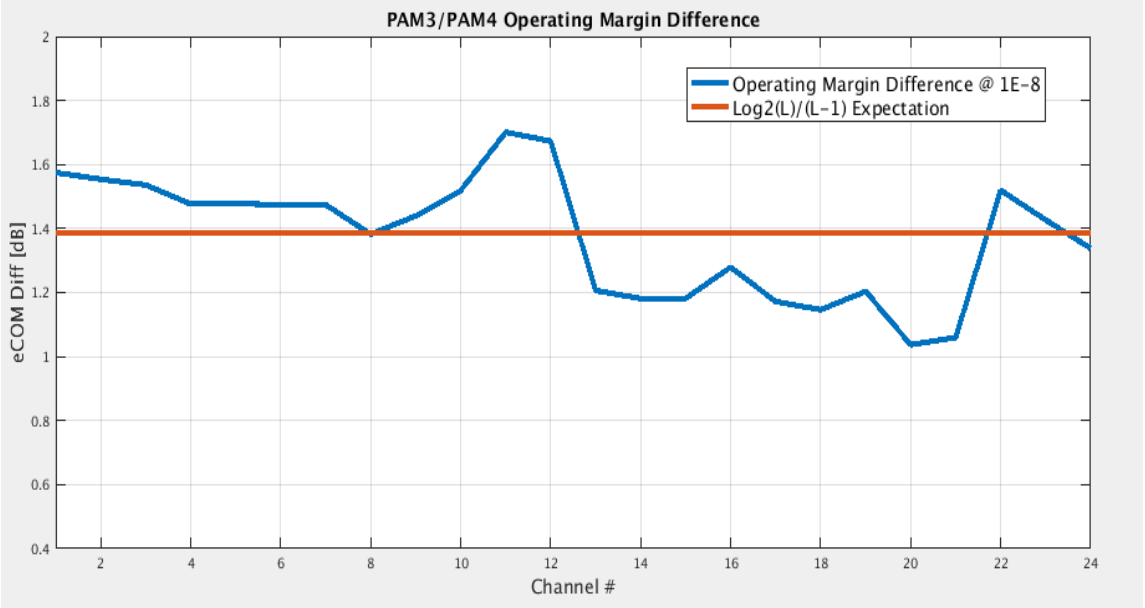

Without Pre-Coding (3 RS errors)




With Pre-Coding (2 RS errors)

# PAM-M Simulation Results: Analysis

- The signal headroom is defined by the distance between the constellation levels (proportional to 1/(L-1), where L is the number of levels)
- Empirical results indicate that the noise is approx. scaled according to the baud rate (which is proportional to 1/log2(L))
- As a result, the operating margin is proportional to the ratio between the levels distance and the rate (log2(L)/(L-1))
- Therefore, PAM-3 gains SNR Margin of 1.4dB over PAM-4:
  - (0.5/25.6G)/(0.33/20G)=1.4dB
  - Signal scaling: 0.5/0.33=1.5x
  - Noise scaling: 25.6G/20G=1.28x



# TX Circuit UDJ Background

- IEEE 50G Ethernet standard (802.3cd) reference:
  - $J_{rms}$=0.023UI (STD of the jitter PDF)
  - $J_{3u}$=0.115UI (Pk-Pk jitter including all but 1E-3 tail of the jitter PDF)
- Deriving the corresponding UDJ assuming SJ dominated model:

  $J_{rms}^2=(A_{PJ}/sqrt(2))^2+RJ^2$

  $J_{3u}=2*A_{PJ}+2*Q3*RJ$ //Q=3.29 (Q(Q3)=0.5*1E-3)

  $\rightarrow A_{PJ}$=0.03UI peak
- Deriving the corresponding UDJ assuming Dual-Dirac dominated model:

  $J_{rms}^2=A_{DD}^2+RJ^2$

  $J_{3u}=2*A_{DD}+2*Q3*RJ$ //Q=3.29 (Q(Q3)=0.5*1E-3)

  $\rightarrow A_{DD}$=0.02UI peak
- IEEE reference TX UDJ is at 0.02-0.03UI peak range (depends on the UDJ exact components), and therefore 0.025UI peak (0.05UI pk-pk) is assumed

# SSC Residual Jitter Background

- Triangular SSC modulation test-case:

$$SSC_{Jitter_{pkpk}} = \frac{1}{T} \cdot \frac{\left(16[us] \cdot \frac{T \cdot SSC_{pkpk}}{2}\right)}{2} = \frac{16[us] \cdot SSC_{pkpk}[ppm] \cdot 10^{-6}}{4} = 12ns \quad (SSC_{pkpk} = 3000ppm)$$

- Sinusoidal SSC modulation test-case:

$$SSC\_Jitter_{pkpk} = \frac{1}{T} \cdot 2 \cdot \frac{T \cdot SSC_{pkpk}[ppm] \cdot 10^{-6}}{2} \cdot \frac{1}{2 \cdot \pi \cdot 32e3[Hz]} = \frac{SSC_{pkpk[ppm]} \cdot 10^{-6}}{2 \cdot \pi \cdot 32e3[Hz]} = 15ns \quad (SSC_{pkpk} = 3000ppm)$$

Residual jitter assuming CDR jitter rejection of 91dB @ 32KHz ($\zeta$=0.71, $\omega_n$=3.8E7 r/s):

Triangle SSC profile: 12ns – 91dB = 0.34ps

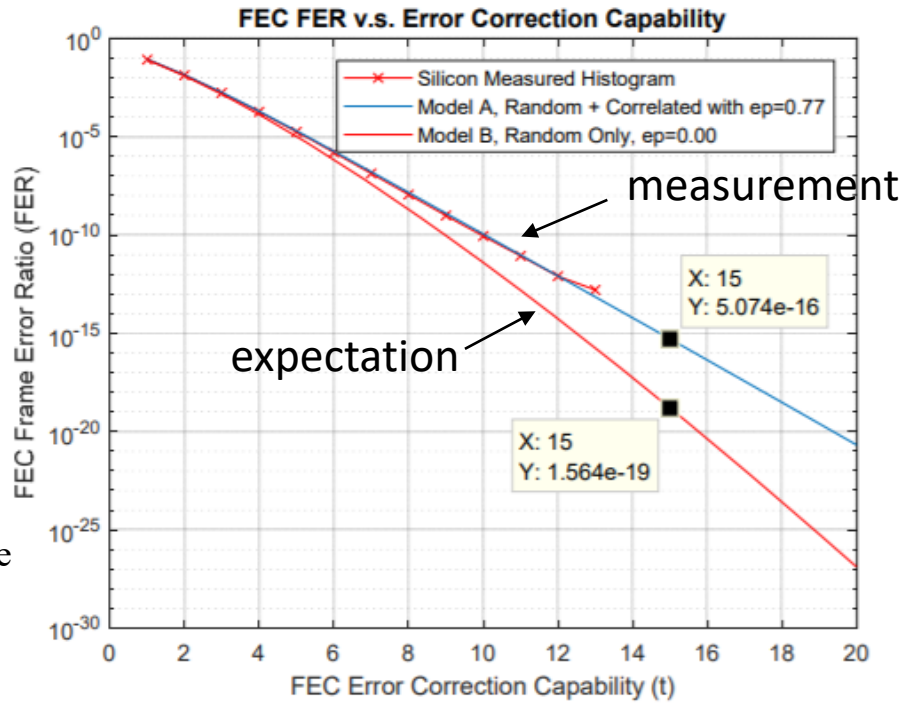
Sinusoidal SSC profile: 15ns – 91dB = 0.42ps

→ 0.4ps pk-pk (0.01UI) is assumed

# Correlated Errors: Networking Reference

- Correlated errors are observed in PAM4 optical links (based on field measurements)
- Correlated errors exist regardless of the DFE error propagation effects
- IEEE spec is defined as following:

For the 50GBASE-KR and 100GBASE-KR2 PHYs, in order to support the required frame loss ratio (see 1.4.275) of less than $6.2 \times 10^{-10}$ for 64-octet frames with minimum interpacket gap, the PMD and the adjacent PMA are expected to detect bits from a compliant input signal at a BER lower than $2.4 \times 10^{-4}$ assuming errors are sufficiently uncorrelated. This BER allocation enables a frame loss ratio lower than $10^{-10}$ after processing by the RS-FEC (Clause 134 or Clause 91) and the PCS (Clause 133 or Clause 82) if there are negligible errors due to other electrical interfaces (50GAUI-n or 100GAUI-n). If the PMD and PMA create errors that are not sufficiently uncorrelated, the BER is required to be lower as appropriate to maintain a frame loss ratio lower than $10^{-10}$.




Source: IEEE 802.3ck/cd material