

Universal Serial Bus 3.2 Link Layer Test Specification

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Revision History

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1 Introduction

This document provides the compliance criteria and test descriptions for Enhanced SuperSpeed USB 3.2 Link Layer implementations. It is relevant for anyone building an Enhanced SuperSpeed host, hub or device. The document is divided into two major sections. The first section lists the compliance criteria and the second section lists the test descriptions used to verify a port's conformance to these criteria.

Compliance criteria are provided as a list of assertions that describe specific characteristics or behaviors that must be met. Each assertion provides a reference to the USB 3.1 specification or other documents from which the assertion was derived. In addition, each assertion provides a reference to the specific test description(s) where the assertion is tested.

Each test assertion is formatted as follows:

Assertion #	Assertion Description	Test #
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Assertion#: Unique identifier for each spec requirement. The identifier is in the form USB31_SPEC_SECTION_NUMBER#X, where X is a unique integer for a requirement in that section.

Assertion Description: Specific requirement from the specification

Test #: A label for a specific test description in this specification that tests this requirement. Test # can have one of the following values:

- NT** This item is not explicitly tested in a test description. Items can be labeled NT for several reasons – including items that are not testable, not important to test for interoperability, or are indirectly tested by other operations performed by the compliance test.
- X.X** This item is covered by the test described in test description X.X in this specification.
- IOP** This assertion is verified by the USB 3.0 Interoperability Test Suite.
- BC** This assertion is applied as a background check in all test descriptions.

Test descriptions provide a high level overview of the tests that are performed to check the compliance criteria. The descriptions are provided with enough detail so that a reader can understand what the test does. The descriptions do not describe the actual step-by-step procedure to perform the test.

Host tests are performed with a Windows 8 machine with all the latest Microsoft updates. The Compliance driver is loaded for most of the Host tests. The Compliance Driver is provided with USB30CV from the usb.org website. One of the Host tests requires the vendor driver for the host controller to be loaded.

Some of the downstream port tests require USB30CV test supplements to perform the test. If a test requires USB30CV, it will be noted in the description later in this document. To run the LVS (Link Validation System) and USB30CV together, always start the USB30CV test prior to the LVS test.

For questions about this document, please contact ssusbcompliance@usb.org. For questions regarding the test matrix or equipment please contact techadmin@usb.org.

2 Terms and Abbreviations

This chapter lists and defines terms and abbreviations used throughout this specification. Terms and Abbreviations specified in the USB 3.0 specifications are not duplicated here.

Term/Abbreviation	Definition
Host Controller Test Driver	The USB30CV driver running on the host controller. This driver has a known behavior in order to run a portion of the tests described in this specification (for host downstream port testing only).
Link Validation System	The hardware aimed at running the tests on an Upstream or a Downstream Port Under Test. The Link Validation System will act as the opposite port.
LVS	See Link Validation System.
Port Under Test	The port connected to the Link Validation System on which the tests are run.
PUT	See Port Under Test.
USB30CV	USB 3.0 Command Verifier software, available for download from usb.org . The same software that runs Ch 9 and MSC tests.

3 Test Assertions

Unless otherwise noted, subsection references point to the USB 3.1 specification.

Assertion #	Assertion Description	Test #
Chapter 7 Test Assertions: Link Layer		
Subsection reference: 7.2 Link Management and Flow Control		
Subsection reference: 7.2.1 Packets and Packet Framing		
Subsection reference: 7.2.1.1 Header Packet Structure		
7.2.1.1#1	For SuperSpeed USB, all header packets shall be 20 symbols long. This includes LMPs, TPs, ITPs, and DPHs. A header packet consists of three parts: a header packet framing, a packet header, and a Link Control Word.	BC
7.2.1.1#2	For SuperSpeedPlus USB, all header packets except for non-deferred DPH shall be 20 symbols long. The non-deferred SuperSpeedPlus DPH is a header packet with its own framing ordered set, and contains a length field replica immediately after the Link Control Word.	BC
Subsection reference: 7.2.1.1.1 Header Packet Framing		
7.2.1.1.1#1	All header packets except for non-deferred SuperSpeedPlus DPH shall always begin with HPSTART ordered set.	BC
7.2.1.1.1#2	A non-deferred SuperSpeedPlus data packet header shall always begin with DPHSTART ordered set.	BC
7.2.1.1.1#2	A deferred SuperSpeedPlus data packet header shall always begin with HPSTART ordered set and it shall contain the length field replica.	BC
Subsection reference: 7.2.1.1.2 Packet Header		
7.2.1.1.2#1	A packet header shall consist of 12 bytes of header information and a 2-byte CRC-16.	BC
7.2.1.1.2#2	The CRC-16 shall be calculated as specified when transmitted.	BC
Subsection reference: 7.2.1.1.3 Link Control Word		
7.2.1.1.3#1	The Link Control Word shall contain a 3-bit Header Sequence Number, 3-bit Reserved, a 3-bit Hub Depth Index, a Delayed bit (DL), a Deferred bit (DF), and a 5-bit CRC-5.	BC
7.2.1.1.3#2	The CRC-5 shall be calculated as specified when transmitted.	BC
Subsection reference: 7.2.1.2 Data Packet Payload Structure		
Subsection reference: 7.2.1.2.1 Data Packet Payload Framing		

Assertion #	Assertion Description	Test #
7.2.1.2.1#1	A data payload packet shall always begin with DPPSTART ordered set.	IOP
7.2.1.2.1#2	A data payload packet shall always end with DPPEND ordered set to indicate normal ending.	IOP
7.2.1.2.1#3	A data payload packet shall always end with DPPABORT ordered set to indicate an abnormal ending.	NT
Subsection reference: 7.2.1.2.2 Data Packet Payload		
7.2.1.2.2#1	The DPP section shall consist of 0 to 1024 bytes of data payload followed by the 4-byte CRC-32.	IOP
7.2.1.2.2#2	The CRC-32 shall be calculated as specified when transmitted.	IOP
7.2.1.2.2#3	The CRC-32 for a 0 bytes payload shall be 0x00000000.	NT
7.2.1.2.2#4	For SuperSpeed USB, any premature termination of a DPP shall end with a DPPABORT ordered set.	NT
7.2.1.2.2#5	For SuperSpeedPlus USB, a usb port shall always preserve the DPP boundary by completing the DPP transmission meeting the length field specification defined in its associated DPH except if a downstream port is directed to issue a Warm Reset, or a port is directed to enter Recovery.	NT
7.2.1.2.2#6	In all other cases besides the exceptions specified, a port in SuperSpeedPlus operation shall append DPPEND OS upon completing the transmission of DPP, of in the case of a nullified DPP, it shall append DPPABORT OS immediately after its DPH, or in the case of a partially nullified DPP, it shall append DPPABORT OS after completing the DPP as defined by the length field in its associated DPH.	IOP partial coverage
7.2.1.2.2#7	A port shall fill with Idle Symbols in DPP if intended data for transmission are not available.	NT
Subsection reference: 7.2.1.2.3 Data Payload Structure and Spacing between DPH and DPP		
7.2.1.2.3#1	There shall be no spacing between a DPH and its corresponding DPP.	IOP
Subsection reference: 7.2.1.3 SuperSpeedPlus Packet Placement		
7.2.1.3#1	For SuperSpeedPlus USB, all packets shall be placed in data blocks and the placement of a packet may start in any symbol position within a data block, and may cross over into the next consecutive data block.	BC
Subsection reference: 7.2.2 Link Commands		
Subsection reference: 7.2.2.1 Link Command Structure		

Assertion #	Assertion Description	Test #
7.2.2.1#1	A link command shall be eight symbols long and begin with LCSTART ordered set.	BC
7.2.2.1#2	A link command shall consist of two identical consecutive Link Command Words.	BC
Subsection reference: 7.2.2.2 Link Command Word Definition		
7.2.2.2#1	A link command word shall be 16 bits long, with the 11-bit link command information protected by a 5-bit CRC-5.	BC
7.2.2.2#2	The CRC-5 shall be computed as specified when transmitted.	BC
7.2.2.2#3	Any transmitted link command shall match one of the link commands presented in table 7-4 of USB 3.0 spec.	BC
Subsection reference: 7.2.2.3 Link Command Placement		
7.2.2.3#1	Link commands shall not be placed inside header packet structures.	BC
7.2.2.3#2	Link commands shall not be placed within the DPP of a DP structure.	NT
7.2.2.3#3	Link commands shall not be placed between the DPH and the DPP.	IOP
7.2.2.3#4	Link commands may be placed before and after a header packet with the exception that they shall not be placed in between a DPH and its DPP.	BC IOP
7.2.2.3#5	Link commands shall not be sent until all scheduled SKP ordered sets have been transmitted.	NT
7.2.2.3#6	For SuperSpeedPlus USB, all link commands shall be placed in data blocks.	BC
7.2.2.3#7	For SuperSpeedPlus USB, the placement of a link command may start in any symbol position within a data block, and may cross over to the next consecutive data block.	BC
Subsection reference: 7.2.3 Logical Idle		
7.2.3#1	Idle Symbol shall be transmitted by a port at any time in U0 meeting the logical idle definition.	BC
Subsection reference: 7.2.4 Link Command Usage for Flow Control, Error Recovery, and Power Management		
Subsection reference: 7.2.4.1 Header Packet Flow Control and Error Recovery		
Subsection reference: 7.2.4.1.1 Initialization		
7.2.4.1.1#1	A port shall maintain two Tx Header Sequence Numbers, one is the Tx Header Sequence Number which will be assigned to the	BC

Assertion #	Assertion Description	Test #
	next header packet to be transmitted (not re-transmitted), and one is the ACK Tx Header Sequence Number which is expected on the next received LGOOD_n acknowledging receipt of a header packet.	
7.2.4.1.1#2	A port shall maintain an Rx Header Sequence Number, which is the expected Header Sequence Number on the next header pack received.	BC
7.2.4.1.1#3	A port in SupserSpeed operation shall maintain two Rx Header Buffer Credit Counts, one for the local available Rx Header Buffer Credits, and one for its link partners available Rx Header Buffer Credits.	BC
7.2.4.1.1#4	A port in SupserSpeedPlus operation shall maintain two Type 1 Rx Header Buffer Credit Counts, one for the local available Type 1 Rx Header Buffer Credits, and one for its link partners available Type 1 Rx Header Buffer Credits.	BC
7.2.4.1.1#5	A port in SupserSpeedPlus operation shall maintain two Type 2 Rx Header Buffer Credit Counts, one for the local available Type 2 Rx Header Buffer Credits, and one for its link partners available Type 2 Rx Header Buffer Credits.	BC
7.2.4.1.1#6	A port in SuperSpeed operation shall have enough Tx Header Buffers in its transmitter to hold up to four unacknowledged header packets.	BC
7.2.4.1.1#7	A port in SuperSpeedPlus operation shall have enough Type 1/Type 2 Tx Header Buffers in its transmitter to hold up to four unacknowledged header packets of Type 1 traffic class, and another four unacknowledged data packet headers of Type 2 traffic class.	BC
7.2.4.1.1#8	A port in SuperSpeed operation shall not transmit any header packet if its Remote Rx Header Buffer Credit Count is zero.	NT
7.2.4.1.1#9	A port in SuperSpeedPlus operation shall not transmit any Type 1 packets if its Remote Type 1 Rx Buffer Credit Count is zero, or any Type 2 packets if its Remote Type 2 Rx Buffer Credit Count is zero.	NT
7.2.4.1.1#10	A port in SuperSpeed operation shall have enough Rx Header Buffers in its receiver to receive up to four header packets.	NT
7.2.4.1.1#11	A port in SuperSpeedPlus operation shall have enough Rx Header Buffers in its receiver to receive up to four Type 1 packets of maximum DPP size, and another four Type 2 packet of maximum DPP size.	NT
7.2.4.1.1#12	Upon entry to U0, a port in SuperSpeed operation shall start the PENDING_HP_TIMER and CREDIT_HP_TIMER in expectation of the Header Sequence Number Advertisement and the Type 1 and Type 2 Rx Header Buffer Credit Advertisements.	7.26
7.2.4.1.1#13	Upon entry to U0, a port in SuperSpeedPlus operation shall start the PENDING_HP_TIMER and Type 1 and Type 2	7.26

Assertion #	Assertion Description	Test #
	CREDIT_HP_TIMERS in expectation of the Header Sequence Number Advertisement and the Rx Header Buffer Credit Advertisement.	
7.2.4.1.1#14	Upon entry to U0, after starting the PENDING_HP_TIMER and (Type 1/Type 2) CREDIT_HP_TIMER timers, a port shall initiate the Header Sequence Number Advertisement.	7.26 BC
7.2.4.1.1#15	Upon entry to U0, after the Header Sequence Number Advertisement, a port in SuperSpeed operation shall initiate the Rx Header Buffer Credit Advertisement.	5.1 7.26
7.2.4.1.1#16	Upon entry to U0, after the Header Sequence Number Advertisement, a port in SuperSpeedPlus operation shall initiate the Type 1 and Type 2 Rx Header Buffer Credit Advertisement.	5.1 7.26
7.2.4.1.1#17	A port shall set its initial Rx Header Sequence Number to zero when it enters U0 from Polling or Hot Reset.	5.1 7.27 - 29
7.2.4.1.1#18	A port shall set its initial Rx Header Sequence Number to the Header Sequence Number of the next expected header packet when it enters U0 from Recovery.	5.1 7.30
7.2.4.1.1#19	A port shall set its initial Tx Header Sequence Number to zero when it enters U0 from Polling or Hot Reset.	5.1 7.27 – 7.29
7.2.4.1.1#20	A port shall set its initial Tx Header Sequence Number to the same as the Tx Header Sequence Number before Recovery when it enters U0 from Recovery.	7.26 7.30
7.2.4.1.1#21	A header packet that is re-transmitted shall maintain its original Header Sequence Number.	7.8
7.2.4.1.1#22	A port shall initiate the Header Sequence Number Advertisement by transmitting LGOOD_n with “n” equal to the Rx Header Sequence Number minus one.	5.1
7.2.4.1.1#23	A port shall set its initial ACK Tx Header Sequence Number to the Sequence Number received during the Rx Header Sequence Number Advertisement plus one.	5.1
7.2.4.1.1#24	A port in SuperSpeed operation shall not send any header packets until the Header Sequence Number Advertisement has been received and a Remote Rx Header Buffer Credit is available.	5.1
7.2.4.1.1#25	A port in SuperSpeedPlus operation shall not send any Type 1 or Type 2 packet until the Header Sequence Number Advertisement has been received and the port’s respective Remote Type 1 or Type 2 Rx Header Buffer Credit is available.	5.1

Assertion #	Assertion Description	Test #
7.2.4.1.1#26	A port shall not request for low power link state entry before receiving and sending the Header Sequence Number Advertisement.	5.1
7.2.4.1.1#27	Upon receiving the Header Sequence Number Advertisement, a port shall flush all the header packets in its (Type 1/Type 2) Tx Header Buffers if the port entered U0 from Polling or Hot Reset.	NT
7.2.4.1.1#28	Upon entering U0 from Recovery and receiving the Header Sequence Number Advertisement, a port shall flush all the header packets in its (Type 1/Type 2) Tx Header Buffers that have been sent before Recovery except for those with the Header Sequence Number greater than (modulo 8) the Header Sequence Number received in the Header Sequence Number Advertisement.	NT
7.2.4.1.1#29	A port shall initiate the (Type 1/Type 2) Rx Header Buffer Credit Advertisement after sending LGOOD_n during Header Sequence Number Advertisement.	5.1
7.2.4.1.1#30	A port shall initialize its (Type 1/Type 2) Tx Header Buffer Credit index to A before sending the Rx Header Buffer Credit.	5.1
7.2.4.1.1#31	A port shall initialize its (Type 1/Type 2) Rx Header Buffer Credit index to A before sending the (Type 1/Type 2) Rx Header Buffer Credit.	5.1
7.2.4.1.1#32	A port shall initialize its Remote (Type 1/Type 2) Rx Header Buffer Credit Count to zero before sending the (Type 1/Type 2) Rx Header Buffer Credit.	5.1
7.2.4.1.1#33	A port shall continue to process header packets in its (Type 1/Type 2) Rx Header Buffers that have been either acknowledged with LGOOD_n prior to entry to Recovery, or validated during Recovery, and then update the Local (Type 1/Type 2) Rx Header Buffer Credit Count, before sending the (Type 1/Type 2) Rx Header Buffer Credit.	5.1
7.2.4.1.1#34	When a port enters U0 from Polling or Hot Reset, a port shall set its Local (Type 1/Type 2) Rx Header Buffer Credit Count to 4.	5.1 7.27 - 29
7.2.4.1.1#35	When a port enters U0 from Recovery, a port shall set its Local (Type 1/Type 2) Rx Header Buffer Credit Count to the number of (Type 1/Type 2) Rx Header Buffers available for incoming header packets.	NT
7.2.4.1.1#36	A port shall transmit LCRD_A when the Local (Type 1/Type 2) Rx Header Buffer Credit Count is one based on its Local (Type 1/Type 2) Rx Header Buffer Credit Count.	NT
7.2.4.1.1#37	A port shall transmit LCRD_A and LCRD_B when the Local (Type 1/Type 2) Rx Header Buffer Credit Count is two.	NT

Assertion #	Assertion Description	Test #
7.2.4.1.1#38	A port shall transmit LCRD_A, LCRD_B and LCRD_C when the Local (Type 1/Type 2) Rx Header Buffer Credit Count is three.	NT
7.2.4.1.1#39	A port shall transmit LCRD_A, LCRD_B, LCRD_C, LCRD_D, when the Local (Type 1/Type 2) Rx Header Buffer Credit Count is four.	5.1 7.27 - 29
7.2.4.1.1#40	A port receiving LCRD_x/(LCRD1_x/LCRD2_x) shall increment its Remote (Type 1/Type 2) Rx Header Buffer Credit Count by one each time an LCRD_x/(LCRD1_x/LCRD2_x) is received up to four.	NT
7.2.4.1.1#41	A port shall not transmit any header packet when its Remote (Type 1/Type 2) Rx Header Buffer Credit Count is zero.	NT
7.2.4.1.1#42	A port shall not request for a low power link state entry before receiving and sending LCRD_x/(LCRD1_x/LCRD2_x) during the (Type 1/Type 2) Rx Header Buffer Credit Advertisement.	5.1
7.2.4.1.1#43	A port sending LBAD before Recovery shall not expect to receive LRTY before a retried header packet from its link partner upon entry to U0, when a port enters U0 from Recovery.	NT
7.2.4.1.1#44	A port receiving LBAD before Recovery shall not send LRTY before a retried header packet to its link partner upon entry to U0, when a port enters U0 from Recovery.	NT
Subsection reference: 7.2.4.1.2 General Rules of LGOOD_n and LCRD_x Usage		
7.2.4.1.2#1	For SuperSpeed USB, LCRD_x received out of alphabetical order is considered a missing of a link command, and transition to Recovery shall be initiated.	7.15
7.2.4.1.2#2	For SuperSpeedPlus USB, LCRD1_x received out of alphabetical order is considered a missing of a link command, and transition to Recovery shall be initiated. The same is true for LCRD2_x.	7.15
7.2.4.1.2#3	LGOOD_n received out of numerical order is considered a missing of a link command, and transition to Recovery shall be initiated.	7.14
7.2.4.1.2#4	A hub shall set the DL bit in the Link Control Word when a header packet transmission is delayed.	NT
Subsection reference: 7.2.4.1.3 Transmitting Header Packets		
7.2.4.1.3#1	Before sending a header packet or a Type 1/Type 2 packet, a port shall add the Tx Header Sequence Number corresponding to the Header Sequence Number field in the Link Control Word.	BC
7.2.4.1.3#2	Transmission of a header packet or a Type 1/Type 2 packet shall consume a Tx Header Buffer or a Type 1/Type 2 Tx Header Buffer. The Tx Header Sequence Number shall be incremented	BC

Assertion #	Assertion Description	Test #
	by one after the transmission or roll over to zero if the maximum Header sequence number is reached.	
7.2.4.1.3#3	Transmission of a retried header packet or a Type 1/Type 2 packet shall not consume an additional Tx Header Buffer or Type 1/Type 2 Tx Header Buffer and the Tx Header Sequence Number shall remain unchanged.	7.8
7.2.4.1.3#4	Upon receiving LBAD, a port shall send LRTY followed by resending all header packets that have not been acknowledged with LGOOD_n, except for Recovery.	7.8
7.2.4.1.3#5	Prior to resending a header packet, a port shall set the Delay bit within the Link Control word and re-calculate the CRC-5.	7.8
7.2.4.1.3#6	For SuperSpeed USB, the Remote Rx Header Buffer Credit Count shall be incremented by one if a valid LCRD_x is received.	BC
7.2.4.1.3#7	For SuperSpeedPlus USB, the Remote Type 1 Rx Buffer Credit Count shall be incremented by one if a valid LCRD1_x is received. The Remote Type 2 Rx Buffer Credit Count shall be incremented by one if a valid LCRD2_x is received.	BC
7.2.4.1.3#8	For SuperSpeed USB, the Remote Rx Header Buffer Credit Count shall be decremented by one if a header packet is sent for the first time after entering U0, including when it is resent following Recovery.	NT/BC
7.2.4.1.3#9	For SuperSpeedPlus USB, Remote Type 1 Rx Buffer Credit Count shall be decremented by one if a Type 1 packet is sent for the first time after entering U0, including when it is resent following Recovery. The same operation applies to Remote Type 2 Rx Buffer Credit Count with regard to Type 2 packet.	NT/BC
7.2.4.1.3#10	The Remote Rx Header Buffer Credit Count or Remote Type 1/Type 2 Rx Header Buffer Credit Count shall not be changed when a header packet is retried following LRTY.	NT/BC
Subsection reference: 7.2.4.1.4 Deferred DPH		
7.2.4.1.4#1	The Deferred DPH shall be treated as a TP for buffering and credit purposes.	NT
Subsection reference: 7.2.4.1.5 Receiving Header Packets		
7.2.4.1.5#1	A port receiving a header packet shall send an LGOOD_n when the CRC-5 is valid, the CRC-16 is valid, the Header Sequence Number matches, and an Rx Header Buffer is available to store it.	BC
7.2.4.1.5#2	In SuperSpeed operation, a port shall consume one Rx Header Buffer until it has been processed.	BC
7.2.4.1.5#3	In SuperSpeedPlus operation, a port shall consume one Type 1 Rx Header Buffer until it has been processed.	BC

Assertion #	Assertion Description	Test #
7.2.4.1.5#4	If the header packet has one or more CRC-5 or CRC-16 errors, a port shall issue a single LBAD and ignore all subsequent header packets received until an LRTY has been received or the link has entered Recovery.	BC
7.2.4.1.5#5	If the Header Sequence Number in the received header packet does not match the Rx Header Sequence Number or a port does not have an Rx Header Buffer available to store the packet, the port shall transition to Recovery.	7.13
7.2.4.1.5#6	In SuperSpeed operation, after transmitting LBAD, a port shall continue to issue LCRD_x if an Rx Header Buffer Credit is made available.	7.7
7.2.4.1.5#7	In SuperSpeedPlus operation, after transmitting LBAD, a port shall continue to issue LCRD1_x/LCRD2_x if its respective Type 1/Type 2 Rx Buffer Credit is made available.	7.7
7.2.4.1.4#1	A port shall detect a header packet when receiving an HPSTART framing with at least three valid symbols out of four, and ignore the packet otherwise.	BC 7.5
7.2.4.1.4#2	A port receiving a header packet shall send a LGOOD_n when a valid HPSTART is detected, the CRC-5 is valid, the CRC-16 is valid, no K-symbol occurrence is detected and no 8b/10b error is detected.	BC
7.2.4.1.4#3	A port receiving a header packet shall send an LBAD when a valid HPSTART is detected and either CRC-5 or CRC-16 checks fail.	7.7
7.2.4.1.4#4	A port receiving a header packet shall send an LBAD when a valid HPSTART is detected and any K-symbol occurrence is detected or any 8b/10b error is detected.	7.7
7.2.4.1.5#8	A port shall transition directly to Recovery if it fails to receive a header packet three consecutive times. A port shall not issue the third LBAD upon the third error.	7.30
Subsection reference: 7.2.4.1.6 Receiving Data Packet Header in SuperSpeedPlus Operation		
7.2.4.1.6#1	A port shall accept a DPP and issue an LGOOD_n when the CRC-5 and CRC-16 are valid, the Header Sequence Number matches, and an Rx Buffer is available to store the packet. In this case a port shall ignore the length field replica.	BC
7.2.4.1.6#2	A port shall consume one Type 1 or Type 2 Rx Buffer Credit until it has been processed and an Rx Buffer is available.	BC
7.2.4.1.6#3	If the DPH has one or more CRC-5 or CRC-16 errors, but the two length field replica are valid and identical, a port shall issue a single LBAD and track the associated DPP that immediately follows the DPH. After issuing the LBAD, a port shall ignore all subsequent packets until an LRTY has been received or the link has entered Recovery.	NT

Assertion #	Assertion Description	Test #
7.2.4.1.6#4	If the header number in the received DPH does not match the Rx Header Sequence Number or the Rx Buffer does not have space to store the DP, or the two length field replica are not identical, the port shall enter Recovery.	NT
7.2.4.1.6#5	After transmitting LBAD, a port shall continue to issue LCRD1_x or LCRD2_x if its corresponding Type 1 or Type 2 Rx Buffer Credit is made available.	NT
7.2.4.1.6#6	A port shall transition directly to Recovery if it fails to receive a data packet header three consecutive times. A port shall not issue the third LBAD upon the third error.	NT
Subsection reference: 7.2.4.1.7 SuperSpeed Rx Header Buffer Credit		
7.2.4.1.7#1	A port shall consume one Local Rx Header Buffer Credit if a header packet is "received properly". The Local Rx Header Buffer Credit Count shall be decremented by one.	NT
7.2.4.1.7#2	Upon completion of a header packet processing, a port shall restore a Local Rx Header Buffer Credit by sending a single LCRD_x, advancing the credit index alphabetically, and incrementing the Local Rx Header Buffer Credit Count by one.	BC
Subsection reference: 7.2.4.1.8 SuperSpeedPlus Type 1/Type 2 Rx Buffer Credit		
7.2.4.1.8#1	A port shall consume one Local Type 1 or Type 2 Rx Buffer Credit if the respective Type 1 or Type 2 packet is "received properly". The Local Type 1/Type 2 Rx Buffer Credit Count shall be decremented by one.	NT
7.2.4.1.8#2	Upon completion of a Type 1 or Type 2 packet processing and the respective Type 1 or Type 2 Rx Buffer is made available, a port shall restore accordingly a Local Type 1 or Type 2 Rx Buffer Credit by sending a single LCRD1_x or LCRD2_x, advancing the credit index alphabetically, and incrementing the Local Type 1 or Type 2 Rx Buffer Credit Count by one.	BC
Subsection reference: 7.2.4.1.9 Receiving Data Packet Payload		
7.2.4.1.9#1	For SuperSpeed USB, a DPP processing shall be started if a DPH is properly received and a DPPSTART OS is received properly immediately after its DPH.	BC
7.2.4.1.9#2	For SuperSpeed USB, a DPP processing shall be completed when a valid DPPEND OS is detected.	7.6
7.2.4.1.9#3	For SuperSpeed USB, a DPP processing shall be aborted when a valid DPPABORT OS is detected, when a K-symbol that does not belong to a valid DPPEND or DPPABORT OS is detected before a valid DPPEND or DPPABORD OS -- and in this case a port shall then ignore the corresponding DPPEND or DPPABORT OS associated with the DPP, when a DPP or length exceeding sDataSymbolsBabble has been reached and no valid DPPEND or DPPABORT OS is detected.	NT

Assertion #	Assertion Description	Test #
7.2.4.1.9#4	For SuperSpeed USB, a DPP processing shall be dropped if its DPH is corrupted or when it does not immediately follow its DPH.	NT
7.2.4.1.9#5	For SuperSpeedPlus USB, a DPP processing shall be started if a DPH is received properly or is not received properly but a valid DPP length field replica is declared, and a DPPSTART OS or a DPPABORT OS is received immediately after its DPH.	7.6
7.2.4.1.9#6	For SuperSpeedPlus USB, a DPP processing shall be completed when a valid DPPEND OS or DPPABORT OS is detected at the expected end of DPP indicated by valid length field plus four.	7.6
7.2.4.1.9#7	For SuperSpeedPlus USB, a DPP processing shall be aborted if a DPPEND OS or a DPPABORT OS is not detected at the expected end of DPP indicated by valid length field plus four. In this case the port shall transition to Recovery.	NT
7.2.4.1.6#1	A port shall detect a DPP packet when receiving a DPPSTART framing with at least three valid symbols out of four, and ignore the packet otherwise.	7.6
7.2.4.1.6#2	A port shall accept a DPP when a valid DPPSTART is detected, a valid DPPEND is detected, there are four to 1028 symbols, the CRC-32 is valid, no K-symbol occurrence is detected, no 8b/10b error is detected and it is received immediately after its DPH.	7.6
7.2.4.1.6#3	A port shall ignore a DPP when valid DPPSTART and DPPEND are detected and the CRC-32 check fails, there are less than four symbols, there are more than 1028 symbols, any K-symbol occurrence is detected, any 8b/10b error is detected or it is not preceded immediately by its DPH.	NT
Subsection reference: 7.2.4.1.10 Receiving LGOOD_n		
7.2.4.1.10#1	If a port receives an LGOOD_n and this LGOOD_n is not Header Sequence Number Advertisement, is shall transition to Recovery if the received Header Sequence Number does not match the ACK Tx Header Sequence Number. The ACK Tx Header Sequence Number shall be unchanged.	7.14
Subsection reference: 7.2.4.1.11 Receiving LCRD_x/LCRD1_x/LCRD2_x		
7.2.4.1.11#1	A port shall transition to Recovery if it receives an out of order LCRD_x/LCRD1_x/LCRD2_x.	7.15
Subsection reference: 7.2.4.1.12 Receiving LBAD		
7.2.4.1.12#1	Upon receiving LBAD, a port shall send a single LRTY before retransmitting all the header packets in the (Type 1/Type 2) Tx Header Buffers that have not been acknowledged with LGOOD_n.	7.8
7.2.4.1.12#2	A hub shall set the DL bit in the Link Control Word on all resent header packets and recalculate the CRC-5.	LVS

Assertion #	Assertion Description	Test #
7.2.4.1.12#3	When retransmitting a DP in SuperSpeed operation, a hub shall drop the DPP. When retransmitting a DP in SuperSpeedPlus operation, a hub shall drop the DPP and replace it with a nullified DPP.	IOP
7.2.4.1.12#4	Upon receipt of an LBAD, a port shall send a single LRTY if there is no unacknowledged header packet in the (Type 1/Type 2) Tx Header Buffers.	7.8
Subsection reference: 7.2.4.1.13 Transmitting Timers		
7.2.4.1.13#1	The PENDING_HP_TIMER shall be started when a port enters U0 in expectation of the Header Sequence Number Advertisement.	7.26
7.2.4.1.13#2	The PENDING_HP_TIMER shall be started when the oldest header packet is retransmitted in response to LBAD.	7.8
7.2.4.1.13#3	The PENDING_HP_TIMER shall be started when a header packet is transmitted and there are no prior header packets transmitted but unacknowledged in the (Type 1/Type 2) Tx Header Buffers.	7.11
7.2.4.1.13#4	The PENDING_HP_TIMER shall be reset and restarted when a header packet is acknowledged with LGOOD_n and there are still header packets transmitted but unacknowledged in the (Type 1/Type 2) Tx Header Buffers.	7.9
7.2.4.1.13#5	The PENDING_HP_TIMER shall be reset and stopped when the Header Sequence Number Advertisement is received.	BC
7.2.4.1.13#6	The PENDING_HP_TIMER shall be reset and stopped when a header packet acknowledgement of LGOOD_n is received and all the transmitted header packets in the (Type 1/Type 2) Tx Header Buffers are acknowledged.	BC
7.2.4.1.13#7	The PENDING_HP_TIMER shall be reset and stopped when a header packet acknowledgement of LBAD is received.	7.30
7.2.4.1.13#8	A port in SuperSpeed operation shall transition to Recovery if the PENDING_HP_TIMER times out and the transmission of an outgoing header packet is completed or the transmission of an outgoing DPP is either completed with DPPEND or terminated with DPPABORT.	7.11
7.2.4.1.13#9	A port in SuperSpeedPlus operation shall transition to Recovery if the PENDING_HP_TIMER times out.	7.11
7.2.4.1.13#10	The (Type 1/Type 2) CREDIT_HP_TIMER shall be started when its respective packet or retried packet is sent, or when a port enters U0.	7.12
7.2.4.1.13#11	The (Type 1/Type 2) CREDIT_HP_TIMER shall be reset when its respective valid LCRD_x/LCRD1_x/LCRD2_x is received.	7.10

Assertion #	Assertion Description	Test #
7.2.4.1.13#1 2	The (Type 1/Type 2) CREDIT_HP_TIMER shall be restarted if its respective valid LCRD_x/LCRD1_x/LCRD2_x is received and the respective Remote (Type 1/Type 2) Rx Buffer Credit Count is less than four.	NT
7.2.4.1.13#1 3	A port in SuperSpeed operation shall transition to Recovery if the CREDIT_HP_TIMER times out and the transmission of an outgoing header packet is completed or the transmission of an outgoing DPP is either completed with DPPEND or terminated with DPPABORT.	7.12
7.2.4.1.13#1 4	A port in SuperSpeedPlus operation shall transition to Recovery if the Type 1 or Type 2 CREDIT_HP_TIMER times out.	7.12
Subsection reference: 7.2.4.2.1 Power Management Link Timers		
7.2.4.2.1#1	A port shall start the PM_LC_TIMER after the last symbol of the LGO_Ux link command is sent.	7.21
7.2.4.2.1#2	A port shall disable and reset the PM_LC_TIMER upon receipt of the LAU or LXU.	7.20
7.2.4.2.1#3	A port shall start the PM_ENTRY_TIMER after the last symbol of the LAU is sent.	7.22
7.2.4.2.1#4	A port shall disable and reset the PM_ENTRY_TIMER upon receipt of an LPMA or a TS1 ordered set.	7.23-25
7.2.4.2.1#5	A port shall start the Ux_EXIT_TIMER when it starts to send the LFPS Exit handshake signal.	NT
7.2.4.2.1#6	A port shall disable and reset the Ux_EXIT_TIMER upon entry to U0.	6.6-7
Subsection reference: 7.2.4.2.2 Low Power Link State Initiation		
7.2.4.2.2#1	<p>A port shall not send an LGO_U1, LGO_U2 or LGO_U3 unless it meets all of the following:</p> <ul style="list-style-type: none"> • It has transmitted LGOOD_n and LCRD_x or LCRD1_x/LCRD2_x for all packets received. • It has received LGOOD_n and LCRD_x or LCRD1_x/LCRD2_x for all packets transmitted. • It has no pending packets for transmission. • It has completed the Header Sequence Number Advertisement and the Rx Header Buffer Credit Advertisement or Type 1/Type 2 Rx Buffer Credit Advertisement upon entry to U0. • It is directed by a higher layer to initiate entry. • It has met higher layer conditions for initiating entry. 	7.18-19

Assertion #	Assertion Description	Test #
7.2.4.2.2#2	An upstream port shall send an LAU in response to an LGO_U1 or LGO_U2, when the Force Link PM Accept field is asserted due to having received a Set Link Functionality LMP.	7.23-24
7.2.4.2.2#3	A port shall send an LAU in response to an LGO_U1 or LGO_U2, when all of the following conditions are met: <ul style="list-style-type: none"> • It has transmitted an LGOOD_n, LCRD_x or LCRD1_x/LCRD2_x sequence for all packets received. • It has received an LGOOD_n, LCRD_x or LCRD1_x/LCRD2_x sequence for all packets transmitted. • It has no pending packets for transmission. • It is not directed by a higher layer to reject entry. 	7.23-24
7.2.4.2.2#4	A port shall send an LXU, when any of the above conditions are not met.	NT
7.2.4.2.2#5	A port shall send an LXU in response to an LGO_U1 or LGO_U2, when it has not yet transmitted an LGOOD_n, LCRD_x sequence for all packets received.	NT
7.2.4.2.2#6	A port shall send an LXU in response to an LGO_U1 or LGO_U2, when it has not received an LGOOD_n, LCRD_x sequence for all packets transmitted.	NT
7.2.4.2.2#7	A port shall send an LXU in response to an LGO_U1 or LGO_U2, when it has pending packets for transmission.	NT
7.2.4.2.2#8	A port shall send an LXU in response to an LGO_U1 or LGO_U2, when it is directed by a higher layer to reject entry.	NT
Subsection reference: 7.2.4.2.3 U1/U2 Entry Flow		
7.2.4.2.3#1	A port shall send a signal LGO_U1 or LGO_U2 to request a transition to a low power link state.	7.18-19
7.2.4.2.3#2	A port shall either accept LGO_Ux with a single LAU or shall reject LGO_U1 or LGO_U2 with a single LXU and remain in U0.	7.23-24
7.2.4.2.3#3	Upon sending LGO_U1 or LGO_U2, a port shall not send any packets until it has received LXU or re-entered U0.	7.18-19
7.2.4.2.3#4	Upon sending LGO_U1 or LGO_U2, a port shall continue receiving and processing packets and link commands.	7.18-19
7.2.4.2.3#5	Upon receiving LXU, a port shall remain in U0.	NT
7.2.4.2.3#6	A port shall initiate transition to Recovery when a single LAU or LXU is not received upon PM_LC_TIMER timeout.	7.21
7.2.4.2.3#7	Upon receiving LAU, a port shall send a single LMPA and then the requested low power link state.	7.18-19

Assertion #	Assertion Description	Test #
7.2.4.2.3#8	Upon issuing LAU or LPMA, a port shall not send any packets or link commands.	7.18-19 7.22 7.23-24
7.2.4.2.3#9	A port that sends LAU shall enter the corresponding low power link state upon receipt of LPMA before PM_ENTRY_TIMER timeout.	7.23-24
7.2.4.2.3#10	A port that sends LAU shall enter the low power link state upon PM_ENTRY_TIMER timeout and all of the following conditions are met: <ul style="list-style-type: none"> • LPMA is not received. • No TS1 ordered set is received. 	7.22
7.2.4.2.3#11	A port that sent LAU shall enter Recovery before PM_ENTRY_TIMER timeout when a TS1 ordered set is received.	NT
7.2.4.2.3#12	A port that has sent LAU shall not respond with Ux_LFPS exit handshake before PM_ENTRY_TIMER timeout.	7.22
7.2.4.2.3#13	A port in U1 shall enter U2 directly when the following two conditions are met: <ul style="list-style-type: none"> • The port's U2 inactivity timer is enabled. • The U2 inactivity timer times out and no U1 LFPS exit signal is received. 	NT
Subsection reference: 7.2.4.2.4 U3 Entry Flow		
7.2.4.2.4#1	When directed, a downstream port shall initiate U3 entry process by sending LGO_U3.	7.35 7.36
7.2.4.2.4#2	An upstream port shall send LAU in response to LGO_U3.	7.25
7.2.4.2.4#3	An upstream port shall not send any packets or link commands subsequent to sending an LAU.	7.25
7.2.4.2.4#4	Upon issuing LGO_U3, a downstream port shall ignore any packets sent by an upstream port.	7.35 7.36
7.2.4.2.4#5	A downstream port shall send a single LPMA and then transition to U3 when LAU is received.	7.35 7.36
7.2.4.2.4#6	A downstream port shall transition to Recovery and reinitiate U3 entry after re-entry to U0 when all of the following three conditions are met: <ul style="list-style-type: none"> • PM_LC_TIMER timeout • LAU is not received. 	NT

Assertion #	Assertion Description	Test #
	<ul style="list-style-type: none"> The number of consecutive U3 entry attempts is less than three. 	
7.2.4.2.4#7	An upstream port shall transition to U3 when LPMA is received.	7.25
7.2.4.2.4#8	An upstream port shall transition to U3 when PM_ENTRY TIMER times out and LPMA is not received.	NT
7.2.4.2.4#9	A downstream port shall transition to eSS.Inactive when it fails U3 entry on three consecutive attempts.	NT
Subsection reference: 7.2.4.2.5 Concurrent Low Power Link Management Flow		
7.2.4.2.5#1	When a downstream port has sent an LGO_U1, LGO_U2, LGO_U3 and also received an LGO_U1 or LGO_U2, it shall send an LXU.	NT
7.2.4.2.5#2	When an upstream port has sent an LGO_U1 or LGO_U2 and also received an LGO_U1, LGO_U2, it shall wait until receipt of an LXU and then send either an LAU or LXU.	NT
7.2.4.2.5#3	When an upstream port has sent an LGO_U1 or LGO_U2 and also received an LGO_U3, it shall wait until receipt of an LXU and then send an LAU.	NT
7.2.4.2.5#4	When a downstream port is directed by a higher layer to initiate a transition to U3, and a transition to U1 or U2 has been initiated but not yet completed, the port shall first complete the in-process transition to U1 or U2, then return to U0 and request entry to U3.	NT
Subsection reference: 7.2.4.2.6 Concurrent Low Power Link Management and Recovery Flow		
7.2.4.2.6#1	Upon issuing LGO_Ux, the port shall transition to Recovery when a TS1 ordered set is received.	NT
Subsection reference: 7.2.4.2.7 Low Power Link State Exit Flow		
7.2.4.2.7#1	When a port is initiating U3 wakeup, it shall start sending U3 LFPS wakeup handshake signal.	7.36
7.2.4.2.7#2	A port upon receiving U1/U2 EXIT or U3 wakeup LFPS handshake signal shall start U1/U2 exit or U3 wakeup by responding with U1/U2 Exit or U3 wakeup LFPS signal.	7.18-19 7.23-25
7.2.4.2.7#3	Upon a successful LFPS handshake before tNoLFPSResponse Timeout, a port shall transition to Recovery.	7.18-19 7.23-25
7.2.4.2.7#4	A port initiating U1 or U2 Exit shall transition to eSS.Inactive upon tNoLFPSResponse timeout and the condition of a successful LFPS handshake is not met.	NT
7.2.4.2.7#5	A port initiating U1 or U2 Exit shall transition to eSS.Inactive upon Ux_EXIT_TIMER timeout and the link has not transitioned to U0.	NT

Assertion #	Assertion Description	Test #
7.2.4.2.7#6	A port initiating U3 wakeup shall remain in U3 when the condition of a successful LFPS handshake is not met upon tNoLFPSResponse Timeout.	NT
Subsection reference: 7.3 Link Error Rules/Recovery		
Subsection reference: 7.3.3 Link Error Statistics		
Subsection reference: 7.3.3.1 Link Error Count		
7.3.3.1#1	Except for the upstream port in SuperSpeed operation, all ports shall implement the Link Error Count.	NT
7.3.3.1#2	A port in SuperSpeedPlus operation shall implement a Link Error Count that counts up to 65,535 error events. The Link Error Count shall saturate if it has reached its maximum count value.	NT
7.3.3.1#3	The Link Error Count shall be reset to zero during PowerOn Reset.	NT
7.3.3.1#4	The Link Error Count shall be reset to zero during entry to Polling.Idle.	NT
7.3.3.1#5	The Link Error Count shall be reset to zero when directed.	NT
7.3.3.1#6	The Link Error Count shall be reset to zero during Hot Reset.	NT
7.3.3.1#7	The Link Error Count shall be incremented by one each time a port transitions from U0 to Recovery to recover an error event.	NT
Subsection reference: 7.3.4.1 Packet Framing Errors		
7.3.4.1#1	<p>A valid HPSTART or DPHSTART OS, or a valid DPP framing ordered set shall be declared if the following two conditions are met:</p> <ul style="list-style-type: none"> At least three of the four symbols in the four consecutive symbol periods are valid packet framing symbols. The four symbols are in the order defined in Table 7-9. 	7.6 7.7
7.3.4.1#2	<p>Missing of a header packet shall result in a port transitioning to Recovery depending on which one of the following conditions becomes true first:</p> <ul style="list-style-type: none"> A port transmitting the header packet upon its PENDING_HP_TIMER timeout. A port receiving the header packet upon detection of a Rx Header Sequence Number error. 	7.6 7.7
7.3.4.1#3	Missing of a DPP framing ordered set in SuperSpeedPlus operation shall result in a port transitioning to Recovery.	7.6
7.3.4.1#4	The Link Error Count shall be incremented by one each time a transition to Recovery occurs.	NT

Assertion #	Assertion Description	Test #
Subsection reference: 7.3.5 Link Commands Errors		
7.3.5#1	A port shall detect a link command when receiving a LCSTART framing with at least three valid symbols out of four in the correct order, and ignore the link command otherwise.	7.2
7.3.5#2	For SuperSpeed USB, a valid link command is declared if both link command words are the same, they both contain valid link command information as defined in Table 7-4 and they both pass CRC-5 check.	5.1 7.2 7.3 7.4
7.3.5#2	For SuperSpeedPlus USB, a valid link command is declared if both link command words are the same, they both contain valid link command information as defined in Table 7-4 and they both pass CRC-5 check, or if one of the link command words contains valid link command information and passes the CRC-5 check, and the other link command word either contains invalid link command information or fails the CRC-5 check.	5.1 7.2 7.3 7.4
7.3.5#4	A port shall transition to Recovery upon detection of an LGOOD_n ordering error.	7.14
7.3.5#5	A port shall transition to Recovery upon detection of an LCRD_x or LCRD1_x/LCRD2_x ordering error.	7.15
7.3.5#6	A port shall transition to Recovery upon its PM_LC_TIMER timeout.	7.21
7.3.5#7	A downstream port shall transition to Recovery upon detection of a missing LUP.	7.16
7.3.5#8	An upstream port shall transition to Recovery upon detection of a missing LDN	7.16
Subsection reference: 7.3.6 ACK Tx Header Sequence Number Errors		
7.3.6#1	An ACK Tx Header Sequence Number error shall be declared when the Header Sequence Number in the received LGOOD_n does not match the ACK Tx Header Sequence Number.	7.13
Subsection reference: 7.3.7 Header Sequence Number Advertisement Error		
7.3.7#1	A port shall transition to Recovery upon its PENDING_HP_TIMER timeout before the Header Sequence Number Advertisement is received.	7.26
7.3.7#2	A port shall transition to Recovery when a header packet is received before sending the Header Sequence Number Advertisement.	NT
7.3.7#3	A port shall transition to Recovery when an LCRD_x or LCRD1_x/LCRD2_x or LGO_Ux is received before receiving the Header Sequence Number Advertisement.	NT

Assertion #	Assertion Description	Test #
Subsection reference: 7.3.8 SuperSpeed Rx Header Buffer Credit Advertisement Error		
7.3.8#1	A port shall transition to Recovery upon its CREDIT_HP_TIMER timeout before the Header Buffer Credit Advertisement is received.	NT
7.3.8#2	A port shall transition to Recovery when a header packet is received before sending the Header Buffer Credit Advertisement.	NT
7.3.8#3	A port shall transition to Recovery when a LGO_Ux is received before receiving the Header Buffer Credit Advertisement.	NT
Subsection reference: 7.3.9 SuperSpeedPlus Type 1/Type 2 Rx Buffer Credit Advertisement Error		
7.3.9#1	A port shall transition to Recovery upon a Type 1/Type 2 CREDIT_HP_TIMER timeout and its respective LCRD1_x or LCRD2_x is not received.	NT
7.3.9#2	A port shall transition to Recovery when a Type 1 packet is received before sending LCRD1_x, or a Type 2 packet is received before sending LCRD2_x.	NT
7.3.9#3	A port shall transition to Recovery when LGO_Ux is received before receiving LCRD1_x or LCRD2_x.	NT
Subsection reference: 7.3.10 Training Sequence Error		
7.3.10#1	For SuperSpeedPlus operation, upon detecting a timeout in Polling.Active or Polling.Configuration, the port shall transition to Polling.PortMatch to negotiate for SuperSpeed operation.	7.39
7.3.10#2	For SuperSpeed operation, a downstream port shall transition to Rx.Detect when a Training Sequence error occurs during Polling and cPollingTimeout is less than two.	7.40
7.3.10#3	For SuperSpeed operation, a downstream port shall transition to eSS.Inactive when a Training Sequence error occurs during Polling and cPollingTimeout is two.	7.40
7.3.10#4	For SuperSpeed operation, an upstream port of a hub shall transition to Rx.Detect when a Training Sequence error occurs during Polling.	NT
7.3.10#5	For SuperSpeed operation, an upstream port of a peripheral device shall transition to eSS.Disabled when a Training Sequence error occurs during Polling.	NT
7.3.10#6	For SuperSpeed operation, a downstream port shall transition to eSS.Inactive when a Training Sequence error occurs during Recovery and the transition to Recovery is not an attempt for Hot Reset.	NT
7.3.10#7	For SuperSpeed operation, a downstream port shall transition to Rx.Detect when a Training Sequence error occurs during	NT

Assertion #	Assertion Description	Test #
	Recovery.Active and Recovery.Configuration and the transition to Recovery is not an attempt for Hot Reset.	
7.3.10#8	For SuperSpeed operation, an upstream port shall transition to eSS.Inactive when a Training Sequence error occurs during Recovery.	NT
Subsection reference: 7.4 PowerOn Reset and Inband Reset		
Subsection reference: 7.4.1 Power On Reset		
7.4.1#1	Receiver termination shall meet the ZRX-HIGH-IMP-DC-POS when PowerOn Reset is asserted or while VBUS is OFF.	NT
7.4.1#2	Transmitters shall hold a constant DC common mode voltage (VTX-DC-CM) when PowerOnReset is asserted or while VBUS is OFF.	NT
7.4.1#3	The LTSSM of a port shall be initialized to Rx.Detect, when PowerOnReset is completed and VBUS is valid.	NT
7.4.1#4	The LTSSM and the PHY level variables shall be reset to their default values, when PowerOnReset is completed and VBUS is valid	NT
7.4.1#5	The receiver termination of a port shall meet RRX-DC, when PowerOnReset is completed and VBUS is valid.	NT
Subsection reference: 7.4.2 Inband Reset		
7.4.2#1	Upon completion of Hot Reset, a downstream port shall reset its Link Error Count.	NT
7.4.2#2	Upon completion of Hot Reset, the port shall reset its PM timers and the associated U1 and U2 timeout values to zero.	LVS
7.4.2#3	Upon completion of Hot Reset, the port configuration information of an upstream port shall remain unchanged.	7.28 7.29
7.4.2#4	Upon completion of Hot Reset, the PHY level variables shall remain unchanged.	NT
7.4.2#5	Upon completion of Hot Reset, the LTSSM of a port shall transition to U0.	7.27-29
7.4.2#6	An upstream port shall enable its LFPS receiver and Warm Reset detector in all link states except eSS.Disabled.	NT
7.4.2#7	Upon a completion of a Warm Reset, a downstream port shall reset its Link Error Count.	NT
7.4.2#8	Upon a completion of a Warm Reset, Port Configuration information of an upstream port shall be reset to default values.	7.31

Assertion #	Assertion Description	Test #
7.4.2#9	Upon a completion of a Warm Reset, the PHY level variables shall be reinitialized or retrained.	NT
7.4.2#10	Upon a completion of a Warm Reset, the LTSSM of a port shall transition to U0 through Rx.Detect and Polling.	7.31
7.4.2#11	When a PORT_RESET is directed, when the downstream port is in U3, or Loopback, or Compliance Mode, or eSS.Inactive, it shall use Warm Reset.	7.34
7.4.2#12	When a PORT_RESET is directed, when the downstream port is in U0, it shall use Hot Reset.	7.29
7.4.2#13	When a PORT_RESET is directed, when the downstream port is in U1 or U2, it shall exit U1 or U2 using the LFPS exit handshake, transition to Recovery and then transition to Hot Reset.	NT
7.4.2#14	When a PORT_RESET is directed, when a downstream port is in a transitory state of Polling or Recovery, it shall use Hot Reset.	NT
7.4.2#15	When a PORT_RESET is directed, when a Hot Reset fails due to a LFPS handshake timeout, a downstream port shall transition to eSS.Inactive.	NT
7.4.2#16	When a PORT_RESET is directed, when a Hot Reset fails due to a TS1/TS2 handshake timeout, a downstream port shall transition to Rx.Detect and attempt a Warm Reset.	7.31
7.4.2#17	When a PORT_RESET is directed, when the downstream port is in eSS.Disabled, an Inband Reset is prohibited.	NT
7.4.2#18	When BH_PORT_RESET is directed, a downstream port shall initiate a Warm Reset in all the link states except eSS.Disabled and transition to Rx.Detect.	NT
7.4.2#19	When BH_PORT_RESET is directed, an upstream port shall enable its LFPS receiver and Warm Reset detector in all the link states except eSS.Disabled.	NT
7.4.2#20	When BH_PORT_RESET is directed, an upstream port receiving Warm Reset shall transition to Rx.Detect.	NT
Subsection reference: 7.5 Link Training and Status State Machine (LTSSM)		
Subsection reference: 7.5.1 eSS.Disabled		
7.5.1#1	A downstream port shall transition to eSS.Disabled from any other state when directed.	NT
7.5.1#2	An upstream port shall transition to eSS.Disabled when VBUS is not valid.	NT
Subsection reference: 7.5.1.1 eSS.Disabled for Downstream Ports and Hub Upstream Ports		

Assertion #	Assertion Description	Test #
Subsection reference: 7.5.1.1.1 eSS.Disabled Requirements		
7.5.1.1.1#1	The port's receiver termination shall present high impedance to ground of ZRX-HIGH-IMP-DC-POS when in SS.Disabled.	NT
7.5.1.1.1#2	The port shall be disabled from transmitting and receiving LFPS and Enhanced SuperSpeed signals when in SS.Disabled.	NT
Subsection reference: 7.5.1.1.2 Exit from eSS.Disabled		
7.5.1.1.2#1	A downstream port shall transition to Rx.Detect when directed.	NT
7.5.1.1.2#2	An upstream port shall transition to Rx.Detect only when VBUS transition to valid or a USB2.0 bus reset is detected.	NT
Subsection reference: 7.5.1.2 eSS.Disabled for Upstream Ports of Peripheral Devices		
Subsection reference: 7.5.1.2.2 eSS.Disabled Requirements		
7.5.1.2.2#1	The requirements from section 7.5.1.1.1 apply.	NT
7.5.1.2.2#2	A peripheral upstream port shall implement a tDisabledCount counter that shall be reset to zero upon invalid Vbus or a successful port configuration exchange.	NT
7.5.1.2.2#3	The tDisabledCount counter shall be incremented upon entry to eSS.Disabled.Default	NT
Subsection reference: 7.5.1.2.3 Exit from eSS.Disabled.Default		
7.5.1.2.3#1	A peripheral upstream port shall transition to Rx.Detect when Vbus transitions to valid.	NT
7.5.1.2.3#2	A peripheral upstream port shall transition to Rx.Detect when a USB 2.0 bus reset is detected and tDisabledCount is less than three.	NT
7.5.1.2.3#3	A peripheral upstream port shall transition to eSS.Disabled.Error if tDisabledCount is three.	NT
Subsection reference: 7.5.1.2.4 Exit from eSS.Disabled.Error		
7.5.1.2.4#1	A peripheral upstream port shall transition to Rx.Detect upon PowerOn reset.	NT
7.5.1.2.4#2	A self-powered peripheral upstream port shall transition to eSS.Disabled.Default upon detection of invalid Vbus.	NT
7.5.1.2.4#3	A self-powered peripheral upstream port shall remain in eSS.Disabled.Error upon detection of USB 2.0 bus reset.	NT
Subsection reference: 7.5.2 eSS.Inactive		
Subsection reference: 7.5.2.3 eSS.Inactive.Quiet		

Assertion #	Assertion Description	Test #
Subsection reference: 7.5.2.3.1 eSS.Inactive.Quiet Requirement		
7.5.2.3.1#1	The function of the far-end receiver termination detection shall be disabled.	NT
Subsection reference: 7.5.2.3.2 Exit from eSS.Inactive.Quiet		
7.5.2.3.2#1	The port shall transition to eSS.Inactive.Disconnect.Detect upon the eSSInactiveQuietTimeout timer timeout.	NT
7.5.2.3.2#2	A downstream port shall transition to Rx.Detect when Warm Reset is issued.	NT
7.5.2.3.2#3	An upstream port shall transition to Rx.Detect upon detection of Warm Reset.	NT
Subsection reference: 7.5.2.4 eSS.Inactive.Disconnect.Detect		
Subsection reference: 7.5.2.4.1 eSS.Inactive.Disconnect.Detect Requirements		
7.5.2.4.1#1	The transmitter shall perform the far-end receiver termination detection when in eSS.Inactive.Disconnect.Detect.	NT
Subsection reference: 7.5.2.4.2 Exit from eSS.Inactive.Disconnect.Detect		
7.5.2.4.2#1	The port shall transition to Rx.Detect when a far-end low-impedance receiver termination (RRX-DC) is not detected.	NT
7.5.2.4.2#2	The port shall transition to eSS.Inactive.Quiet when a far-end low-impedance receiver termination (RRX-DC) is detected.	NT
Subsection reference: 7.5.3 Rx.Detect		
Subsection reference: 7.5.3.3 Rx.Detect.Reset		
Subsection reference: 7.5.3.3.1 Rx.Detect.Reset Requirements		
7.5.3.3.1#1	A downstream port shall transmit Warm Reset for the duration of tReset.	7.31
7.5.3.3.1#2	An upstream port shall remain in this state until it detects the completion of Warm Reset.	NT
Subsection reference: 7.5.3.3.2 Exit from Rx.Detect.Reset		
7.5.3.3.2#1	The port shall transition directly to Rx.Detect.Active when the entry to Rx.Detect is not due to a Warm Reset.	NT
7.5.3.3.2#2	A downstream port shall transition to Rx.Detect.Active after it transmits Warm Reset for the duration of tReset.	NT
7.5.3.3.2#3	An upstream port shall transition to Rx.Detect.Active when it receives no more LFPS Warm Reset signaling.	NT

Assertion #	Assertion Description	Test #
Subsection reference: 7.5.3.4 Rx.Detect.Active		
Subsection reference: 7.5.3.5 Rx.Detect.Active Requirement		
7.5.3.5#1	The transmitter shall initiate a far-end receiver termination detection when in Rx.Detect.Active.	NT
7.5.3.5#2	The number of far-end receiver termination detection events shall be counted by an upstream port when in Rx.Detect.Active.	NT
Subsection reference: 7.5.3.6 Exit from Rx.Detect.Active		
7.5.3.6#1	The port shall transition from Rx.Detect.Active to Polling upon detection of a far-end low-impedance receiver termination (RRX-DC).	NT
7.5.3.6#2	A downstream port shall transition from Rx.Detect.Active to Rx.Detect.Quiet when a far-end low-impedance receiver termination (RRX-DC) is not detected.	NT
7.5.3.6#3	An upstream port of a hub shall transition from Rx.Detect.Active to Rx.Detect.Quiet when a far-end low-impedance receiver termination (RRX-DC) is not detected.	NT
7.5.3.6#4	An upstream port of a peripheral device shall transition from Rx.Detect.Active to Rx.Detect.Quiet when the following two conditions are met: <ul style="list-style-type: none"> A far-end low-impedance receiver termination (RRX-DC) is not detected. The number of far-end receiver termination detection events is less than eight. 	NT
7.5.3.6#5	An upstream port of a peripheral device shall transition from Rx.Detect.Active to eSS.Disabled when the following two conditions are met: <ul style="list-style-type: none"> A far-end low-impedance receiver termination (RRX-DC) is not detected. The number of far-end receiver termination (RRX-DC) detection events has reached eight. 	NT
Subsection reference: 7.5.3.7 Rx.Detect.Quiet		
Subsection reference: 7.5.3.7.1 Rx.Detect.Quiet Requirements		
7.5.3.7.1#1	The far-end receiver termination detection shall be disabled when in Rx.Detect.Quiet.	NT
Subsection reference: 7.5.3.7.2 Exit from Rx.Detect.Quiet		
7.5.3.7.2#1	A downstream port shall transition from Rx.Detect.Quiet to Rx.Detect.Active upon the timeout of the tRxDetectQuietTimeoutDFP timer (12ms to 120ms).	NT

Assertion #	Assertion Description	Test #
7.5.3.7.2#2	An upstream port shall transition from Rx.Detect.Quiet to Rx.Detect.Active upon the timeout of the tRxDetectQuietTimeoutUFP timer (12ms).	NT
Subsection reference: 7.5.4 Polling		
Subsection reference: 7.5.4.2 Polling Requirements		
7.5.4.2#1	A downstream port shall implement a counter, cPollingTimeout, which shall be reset to zero upon PowerOn Reset, Warm Reset on the upstream port, exit to eSS.Disabled or eSS.Inactive or U0, and detection of the removal of far-end terminations.	BC
7.5.4.2#2	A downstream port shall implement a counter, cPollingTimeout, which shall be incremented by one or saturated at two if a transition to Rx.Detect is due to timeout in any of the Polling substates.	7.40
Subsection reference: 7.5.4.3 Polling.LFPS		
Subsection reference: 7.5.4.3.1 Polling.LFPS Requirements		
7.5.4.3.1#1	Upon entry to Polling.LFPS, an LFPS receiver shall be enabled.	BC
7.5.4.3.1#2	Upon entry to Polling.LFPS, a port shall establish its LFPS operating condition within 80 μ s.	NT
7.5.4.3.1#3	A downstream port shall disable its transition path to Compliance Mode upon PowerOn Reset or Warm Reset.	NT
7.5.4.3.1#4	A downstream port shall enabled its transition path to Compliance Mode, if directed.	7.34
7.5.4.3.1#5	An upstream port always has its transition path to Compliance Mode enabled upon PowerOn Reset.	7.33
7.5.4.3.1#6	A port in SuperSpeed operation shall transmit Polling.LFPS.	BC
7.5.4.3.1#7	An upstream port in SuperSpeedPlus operation shall transmit SCD1. If no signature of SCD1 is found in sixteen consecutive Polling.LFPS received, the port shall switch to SuperSpeed operation and transmit Polling.LFPS instead of SCD1.	7.1
7.5.4.3.1#8	A downstream port in SuperSpeedPlus operation shall transmit SCD1 if Compliance Mode is disabled. If no signature of SCD1 is found in sixteen consecutive Polling.LFPS received, the port shall switch to SuperSpeed operation and transmit Polling.LFPS instead of SCD1.	7.1
7.5.4.3.1#8	A downstream port in SuperSpeedPlus operation shall transmit SCD2 if Compliance Mode is enabled.	NT
7.5.4.3.1#9	A port in SuperSpeedPlus operation shall implement a 60us timer (tPollingSCDLFPSTimeout) to monitor the absence of	7.1

Assertion #	Assertion Description	Test #
	LFPS signal after the completion of SuperSpeed Polling.LFPS handshake.	
7.5.4.3.1#10	A port in SuperSpeedPlus operation shall be ready for SuperSpeed operation if it has detected that its link partner operates at SuperSpeed.	7.1
7.5.4.3.1#11	A port shall disabled its transition path to Compliance Mode when it has successfully completed Polling.LFPS handshake or has entered Compliance Mode.	NT
Subsection reference: 7.5.4.3.2 Exit from Polling.LFPS		
7.5.4.3.2#1	The port in SuperSpeed operation shall transition from Polling.LFPS to Polling.RxEQ when the following three conditions are met: <ul style="list-style-type: none"> At least 16 consecutive Polling.LFPS bursts are sent. Two consecutive Polling.LFPS bursts are received. Four consecutive Polling.LFPS bursts are sent after receiving one Polling.LFPS burst. 	BC
7.5.4.3.2#2	A port in SuperSpeedPlus operation shall transition to Polling.LFSPPlus if two SCD1 are transmitted after one SCD1 or SCD2 is received.	BC
7.5.4.3.2#3	A port in SuperSpeedPlus operation shall transition to Polling.RxEQ and switch to SuperSpeed operation if the following conditions are met: <ul style="list-style-type: none"> At least two consecutive Polling.LFPS bursts are received. Twenty Polling.LFPS bursts are transmitted and no SCD1 is detected. No LFPS signal for more than tPollingSCDLFPSTimeout is observed. 	7.1
7.5.4.3.2#4	An upstream port shall transition to from Polling.LFPS to Compliance Mode upon 360-ms timer timeout if the following two conditions are met: <ul style="list-style-type: none"> The port has never successfully completed Polling.LFPS after PowerOn Reset. The condition to transition to Polling.RxEQ is not met. 	7.33 7.34
7.5.4.3.2#5	A downstream port shall transition from Polling.LFPS to Compliance Mode upon the 360ms timer timeout (tPollingLFPSTimeout) if the following three conditions are met: <ul style="list-style-type: none"> The Compliance Mode is enabled. The port has never successfully completed Polling.LFPS handshake after Compliance Mode is enabled. 	7.34

Assertion #	Assertion Description	Test #
	<ul style="list-style-type: none"> The condition to transition to Polling.RxEQ or Polling.LFPSPlus is not met. 	
7.5.4.3.2#6	A downstream port shall transition from Polling.LFPS to Rx.Detect upon the 360-ms timer timeout if cPollingTimeout is less than two and Compliance Mode is disabled.	7.40
7.5.4.3.2#7	A downstream port shall transition from Polling.LFPS to eSS.Inactive upon the 360-ms timer timeout and cPollingTimeout is two.	7.40
7.5.4.3.2#8	An upstream port of a hub shall transition from Polling.LFPS to Rx.Detect upon the 360-ms timer timeout after having trained once since PowerOn Reset if the conditions to transition to Polling.RxEQ are not met.	NT
7.5.4.3.2#9	A peripheral device shall transition from Polling.LFPS to eSS.Disabled upon the 360-ms timeout after having trained once since PowerOn Reset if the conditions to transition to Polling.ExEQ are not met.	NT
7.5.4.3.2#10	A downstream port shall transition from Polling.LFPS to Rx.Detect when directed to issue Warm Reset.	NT
7.5.4.3.2#11	An upstream port shall transition from Polling.LFPS to Rx.Detect when Warm Reset is detected.	NT
Subsection reference: 7.5.4.4 Polling.LFPSPlus		
Subsection reference: 7.5.4.4.1 Polling.LFPSPlus Requirements		
7.5.4.4.1#1	A port in SuperSpeedPlus operation shall transmit SCD2. If SCD2 cannot be found in sixteen consecutive Polling.LFPS received, the port shall transmit Polling.LFPS instead of SCD2.	NT
7.5.4.4.1#2	The operation of the 360ms timer (tPollingLFPSTimeout) shall continue without reset upon entry to this substate from Polling.LFPS.	NT
7.5.4.4.1#3	A port in SuperSpeedPlus operation shall be ready for SuperSpeed operation if it has detected that its link partner operates at SuperSpeed.	7.1
7.5.4.4.1#4	A port in SuperSpeedPlus operation shall implement a 60us timer (tPollingSCDLFPSTimeout) to monitor the absence of LFPS signal after the completion of SuperSpeed Polling.LFPS handshake.	7.1
Subsection reference: 7.5.4.4.2 Exit from Polling.LFPSPlus		
7.5.4.4.2#1	A port in SuperSpeedPlus operation shall transition to Polling.PortMatch if two SCD2 are transmitted after one SCD2 is received.	BC

Assertion #	Assertion Description	Test #
7.5.4.4.2#2	A port in SuperSpeedPlus operation shall transition to Polling.RxEQ and switch to SuperSpeed operation if the following two conditions are met: <ul style="list-style-type: none"> No LFPS signal for more than tPollingSCDLFPSTimeout is observed. Twenty Polling.LFPS bursts are transmitted, after finding no SCD2 is detected. 	NT
7.5.4.4.2#3	A downstream port shall transition to Rx.Detect upon the 360ms timeout detected and cPollingTimeout is less than two.	NT
7.5.4.4.2#4	A downstream port shall transition to eSS.Inactive upon the 360ms timeout detected and cPollingTimeout is two.	NT
7.5.4.4.2#5	An upstream port of a hub shall transition to Rx.Detect upon the 360ms timeout.	NT
7.5.4.4.2#6	An peripheral device shall transition to eSS.Disabled upon the 360ms timeout.	NT
7.5.4.4.2#7	A downstream port shall transition to Rx.Detect when directed to issue Warm Reset.	BC
7.5.4.4.2#8	An upstream port shall transition to Rx.Detect when a Warm Reset is detected.	BC
Subsection reference: 7.5.4.5 Polling.PortMatch		
Subsection reference: 7.5.4.5.2 Polling.PortMatch Requirements		
7.5.4.5.2#1	Upon entry to this substate from Polling.LFSPPlus, the port shall transmit continuous PHY Capability LBPMs to announce its highest PHY capability.	BC
7.5.4.5.2#2	Upon entry to this substate from Polling.Active or Polling.Configuration or Polling.Idle, the port shall transmit continuous PHY Capability LBPMs to announce its next highest PHY capability from its previous PHY Capability.	7.39
7.5.4.5.2#3	A port shall decode received PHY Capability LBPM or PHY Ready LBPM and compare to its own PHY Capability.	BC
7.5.4.5.2#4	The port with higher PHY capability shall adjust its PHY capability by transmitting PHY Capability LBPM that matches its link partner's.	NT
7.5.4.5.2#5	The port with lower PHY capability shall continue transmitting its own PHY Capability LBPMs and monitoring the PHY Capability LBPMs from its link partner.	NT
Subsection reference: 7.5.4.5.3 Exit from Polling.PortMatch		
7.5.4.5.3#1	The port shall transition to Polling.PortConfig when four consecutive and matched PHY Capability LBPMs are sent after	BC

Assertion #	Assertion Description	Test #
	two consecutive and matched PHY Capability LBPMs or PHY Ready LBPMs are received.	
7.5.4.5.3#2	A downstream port shall transition to Rx.Detect upon the tPollingLBPM LFPSTimeout and cPollingTimeout is less than two.	NT
7.5.4.5.3#3	A downstream port shall transition to eSS.Inactive upon the tPollingLBPM LFPSTimeout and cPollingTimeout is two.	NT
7.5.4.5.3#4	An upstream port of a hub shall transition to Rx.Detect upon the tPollingLBPM LFPSTimeout and the conditions to transition to Polling.PortConfig are not met.	NT
7.5.4.5.3#5	A peripheral device shall transition to eSS.Disabled upon the tPollingLBPM LFPSTimeout and the conditions to transition to Polling.PortConfig are not met.	NT
7.5.4.5.3#6	A downstream port shall transition to Rx.Detect when directed to issue Warm Reset.	BC
7.5.4.5.3#7	An upstream port shall transition to Rx.Detect when a Warm Reset is detected.	BC
Subsection reference: 7.5.4.6 Polling.PortConfig		
Subsection reference: 7.5.4.6.1 Polling.PortConfig Requirements		
7.5.4.6.1#1	The operation of the tPollingLBPM LFPSTimeout shall continue without reset upon entry to this substate from Polling.PortMatch.	BC
7.5.4.6.1#2	Upon entry to this state, the port shall place its transmitter in electrical idle if it is preparing its PHY re-configuration according to PHY Capability LBPM negotiated in Polling.PortMatch.	BC
7.5.4.6.1#3	The port shall perform the following PHY re-configuration: <ul style="list-style-type: none"> • The transmitter DC voltage shall be within specification. • The port shall maintain its low-impedance receiver terminations. • The port shall be ready to transmit TSEQ OS. • The port shall be ready to receive TSEQ OS for receiver equalization training. 	BC
7.5.4.6.1#4	Upon completion of PHY re-configuration, the port shall transmit consecutive PHY Ready LBPMs to notify its link partner.	7.1
Subsection reference: 7.5.4.6.2 Exit from Polling.PortConfig		
7.5.4.6.2#1	The port shall transition to Polling.RxEQ when four consecutive and matched PHY Ready LBPMs are sent after two consecutive and matched PHY Ready LBPMs are received.	7.1

Assertion #	Assertion Description	Test #
7.5.4.6.2#2	A downstream port shall transition to Rx.Detect upon the tPollingLBPMLFPSTimeout and cPollingTimeout is less than two.	NT
7.5.4.6.2#3	A downstream port shall transition to eSS.Inactive upon the tPollingLBPMLFPSTimeout and cPollingTimeout is two.	NT
7.5.4.6.2#4	An upstream port of a hub shall transition to Rx.Detect upon the tPollingLBPMLFPSTimeout and the conditions to transition to Polling.PortConfig are not met.	NT
7.5.4.6.2#5	A peripheral device shall transition to eSS.Disabled upon the tPollingLBPMLFPSTimeout and the conditions to transition to Polling.PortConfig are not met.	NT
7.5.4.6.2#6	A downstream port shall transition to Rx.Detect when directed to issue Warm Reset.	NT
7.5.4.6.2#7	An upstream port shall transition to Rx.Detect when a Warm Reset is detected.	NT
Subsection reference: 7.5.4.7 Polling.RxEQ		
Subsection reference: 7.5.4.7.1 Polling.RxEQ Requirements		
7.5.4.7.1#1	The detection and correction of the lane polarity inversion in SuperSpeed operation shall be enabled in Polling.RxEQ.	6.1
7.5.4.7.1#2	The port shall transmit the corresponding TSEQ ordered sets in Polling.RxEQ.	BC
7.5.4.7.1#3	The port shall complete receiver equalizer training upon exit from Polling.RxEQ .	BC
Subsection reference: 7.5.4.7.2 Exit from Polling.RxEQ		
7.5.4.7.2#1	The port in SuperSpeed operation shall transition from Polling.RxEQ to Polling.Active after 65,536 consecutive TSEQ ordered sets are transmitted.	BC
7.5.4.7.2#1	The port in SuperSpeedPlus operation shall transition from Polling.RxEQ to Polling.Active after 262,143 TSEQ ordered sets are transmitted.	BC
7.5.4.7.2#2	A downstream port shall transition from Polling.RxEQ to Rx.Detect when directed to issue Warm Reset.	NT
7.5.4.7.2#3	An upstream port shall transition from Polling.RxEQ to Rx.Detect when Warm Reset is detected.	NT
Subsection reference: 7.5.4.8 Polling.Active		
Subsection reference: 7.5.4.8.1 Polling.Active Requirements		
7.5.4.8.1#1	The port shall transmit TS1 ordered sets in Polling.Active.	BC

Assertion #	Assertion Description	Test #
7.5.4.8.1#2	The port in SuperSpeedPlus operation shall insert a SYNC ordered set every 32 TS1 ordered sets.	BC
7.5.4.8.1#3	The port in SuperSpeedPlus operation shall perform block alignment and scrambler synchronization.	BC
7.5.4.8.1#4	Lane polarity detection and correction shall be completed.	BC
7.5.4.8.1#5	The receiver is training using TS1 or TS2 ordered sets in Polling.Active.	BC
Subsection reference: 7.5.4.8.2 Exit from Polling.Active		
7.5.4.8.2#1	The port in SuperSpeed operation shall transition from Polling.Active to Polling.Configuration upon receiving eight consecutive and identical TS1 or TS2 ordered sets.	BC
7.5.4.8.2#2	The port in SuperSpeedPlus operation shall transition from Polling.Active to Polling.Configuration upon receiving eight consecutive and identical TS1 or TS2 ordered sets, excluding symbols 14 and 15 of TS1 or TS2 ordered sets.	BC
7.5.4.8.2#3	A downstream port in SuperSpeed operation shall transition from Polling.Active to Rx.Detect upon the 12-ms timer timeout if the conditions to transition to Polling.Configuration are not met and cPollingTimeout is less than two.	7.40
7.5.4.8.2#4	A downstream port in SuperSpeed operation shall transition from Polling.Active to eSS.Inactive upon the 12-ms timer timeout if the conditions to transition to Polling.Configuration are not met and cPollingTimeout is two.	7.40
7.5.4.8.2#5	An upstream port of a hub shall transition from Polling.Active to Rx.Detect upon the 12-ms timer timeout if the conditions to transition to Polling.Configuration are not met.	NT
7.5.4.8.2#6	An upstream port of a peripheral device shall transition from Polling.Active to eSS.Disabled upon the 12-ms timer timeout if the conditions to transition to Polling.Configuration are not met.	NT
7.5.4.8.2#7	A downstream port in SuperSpeedPlus operation shall transition to Polling.PortMatch to negotiate for alternative operation upon the 12ms timeout and the conditions to transition to Polling.Configuration are not met.	NT
7.5.4.8.2#8	An upstream port of a hub in SuperSpeedPlus operation shall transition to Polling.PortMatch to negotiate for alternative operation upon the 12ms timeout and the conditions to transition to Polling.Configuration are not met.	NT
7.5.4.8.2#9	An upstream port of a peripheral device in SuperSpeedPlus operation shall transition to Polling.PortMatch to negotiate for alternative operation upon the 12ms timeout and the conditions to transition to Polling.Configuration are not met.	NT

Assertion #	Assertion Description	Test #
7.5.4.8.2#10	A downstream port shall transition to from Polling.Active to Rx.Detect when directed to issue Warm Reset.	NT
7.5.4.8.2#11	An upstream port shall transition to from Polling.Active to Rx.Detect when Warm Reset is detected.	NT
Subsection reference: 7.5.4.9 Polling.Configuration		
Subsection reference: 7.5.4.9.1 Polling.Configuration Requirements		
7.5.4.9.1#1	The downstream port shall transmit identical TS2 ordered sets upon entry to Polling.Configuration and set the Reset bit, when directed.	BC 7.29
7.5.4.9.1#2	A port that has Loopback Master capability and has been directed to enter Loopback shall transmit identical TS2 ordered sets with the Loopback bit set upon entry to Polling.Configuration.	NT
7.5.4.9.1#3	A port that has Disabling Scrambling capability and has been directed to disable scrambling shall transmit identical TS2 ordered sets with the Disabling Scrambling bit set upon entry to Polling.Configuration.	NT
7.5.4.9.1#4	The port in SuperSpeedPlus operation shall insert a SYNC ordered set every 32 TS2 ordered sets.	NT
7.5.4.9.1#5	The port in SuperSpeedPlus operation shall perform block alignment and scrambler synchronization.	NT
Subsection reference: 7.5.4.9.2 Exit from Polling.Configuration		
7.5.4.9.2#1	The port in SuperSpeed operation shall transition from Polling.Configuration to Polling.Idle when the following two conditions are met: <ul style="list-style-type: none"> Eight consecutive and identical TS2 ordered sets are received. Sixteen TS2 ordered sets are sent after receiving the first of the eight consecutive and identical TS2 ordered sets. 	BC
7.5.4.9.2#2	The port in SuperSpeedPlus operation shall transition from Polling.Configuration to Polling.Idle when the following two conditions are met: <ul style="list-style-type: none"> Eight consecutive and identical TS2 ordered sets, excluding symbols 14 and 15, are received. Sixteen TS2 ordered sets are sent after receiving the first of the eight consecutive and identical TS2 ordered sets, excluding symbols 14 and 15. 	BC
7.5.4.9.2#3	A downstream port in SuperSpeed operation shall transition from Polling.Configuration to Rx.Detect upon the 12-ms timer timeout	7.40

Assertion #	Assertion Description	Test #
	if the conditions to transition to Polling.Idle are not met and cPollingTimeout is less than two.	
7.5.4.9.2#4	A downstream port in SuperSpeed operation shall transition from Polling.Configuration to eSS.Inactive upon the 12-ms timer timeout if the conditions to transition to Polling.Idle are not met and cPollingTimeout is two.	NT
7.5.4.9.2#5	An upstream port of a hub in SuperSpeed operation shall transition from Polling.Configuration to Rx.Detect upon the 12-ms timer timeout if the conditions to transitions to Polling.Idle are not met.	NT
7.5.4.9.2#6	An upstream port of a peripheral device in SuperSpeed operation shall transition from Polling.Configuration to SS.Disabled upon the 12-ms timer timeout if the conditions to transition to Polling.Idle are not met.	NT
7.5.4.9.2#7	A downstream port in SuperSpeedPlus operation shall transition to Polling.PortMatch to negotiate for alternative operation upon the 12ms timeout and the conditions to transition to Polling.Configuration are not met.	NT
7.5.4.9.2#8	An upstream port of a hub in SuperSpeedPlus operation shall transition to Polling.PortMatch to negotiate for alternative operation upon the 12ms timeout and the conditions to transition to Polling.Configuration are not met.	NT
7.5.4.9.2#9	An upstream port of a peripheral device in SuperSpeedPlus operation shall transition to Polling.PortMatch to negotiate for alternative operation upon the 12ms timeout and the conditions to transition to Polling.Configuration are not met.	NT
7.5.4.9.2#10	A downstream port shall transition from Polling.Configuration to Rx.Detect when directed to issue Warm Reset.	NT
7.5.4.9.2#11	An upstream port shall transition from Polling.Configuration to Rx.Detect when Warm Reset is detected.	NT
Subsection reference: 7.5.4.10 Polling.Idle		
Subsection reference: 7.5.4.10.1 Polling.Idle Requirements		
7.5.4.10.1#1	A downstream port shall reset its Link Error Count when it enters Polling.Idle.	NT
7.5.4.10.1#2	An upstream port shall reset its port configuration information to default values when it enters Polling.Idle.	NT
7.5.4.10.1#3	A port in SuperSpeed operation shall enable scrambling if the Disabling Scrambling bit is not asserted in the TS2 ordered set received in Polling.Configuration.	NT

Assertion #	Assertion Description	Test #
7.5.4.10.1#4	A port in SuperSpeed operation shall disable the scrambling when directed, or when the Disabling Scrambling bit is asserted in the TS2 ordered set received in Polling.Configuration.	NT
7.5.4.10.1#5	A port in SuperSpeed operation shall transmit Idle Symbols in Polling.Idle if the next state is U0.	NT
7.5.4.10.1#6	A port in SuperSpeedPlus operation shall transmit a single SDS ordered set before the start of the data blocks with Idle Symbols if the next state is U0.	NT
7.5.4.10.1#7	A port in SuperSpeedPlus operation shall disable the scrambling upon completion of SDS ordered set transmission if directed, or if the Disabling Scrambling bit is asserted in the TS2 ordered set received in Polling.Configuration.	NT
7.5.4.10.1#8	The port shall be able to receive the Header Sequence Number Advertisement from its link partner in Polling.Idle.	NT
Subsection reference: 7.5.4.10.2 Exit form Polling.Idle		
7.5.4.10.2#1	A port having Loopback Master capability shall transition to Loopback when directed.	NT
7.5.4.10.2#2	A port shall transition to Loopback as a loopback slave when the Loopback bit is asserted in the TS2 ordered set received in Polling.Configuration.	NT
7.5.4.10.2#3	A downstream port shall transition to Hot Reset when directed.	7.29
7.5.4.10.2#4	An upstream port shall transition to Hot Reset when the Reset bit is asserted in the TS2 ordered set received in Polling.Configuration.	7.27
7.5.4.10.2#5	The port shall transition from Polling.Idle to U0 when the following two conditions are met: <ul style="list-style-type: none"> Eight consecutive Idle Symbols are received. Sixteen Idle Symbols are sent after receiving one Idle Symbol. 	NT
7.5.4.10.2#6	A downstream port in SuperSpeed operation shall transition from Polling.Idle to Rx.Detect upon the 2-ms timer timeout if the conditions to transition to U0 are not met and cPollingTimeout is less than two.	NT
7.5.4.10.2#7	A downstream port in SuperSpeed operation shall transition from Polling.Idle to eSS.Inactive upon the 2-ms timer timeout if the conditions to transition to U0 are not met and cPollingTimeout is two.	NT
7.5.4.10.2#8	An upstream port of a hub in SuperSpeed operation shall transition from Polling.Idle to Rx.Detect upon the 2-ms timer timeout if the conditions to transition to U0 are not met.	NT

Assertion #	Assertion Description	Test #
7.5.4.10.2#9	An upstream port of a peripheral device in SuperSpeed operation shall transition from Polling.Idle to eSS.Disabled upon the 2-ms timer timeout if the conditions to transition to U0 are not met.	NT
7.5.4.10.2#10	A downstream port in SuperSpeedPlus operation shall transition to Polling.PortMatch to negotiate for alternative operation upon the 12ms timeout and the conditions to transition to Polling.Configuration are not met.	NT
7.5.4.10.2#11	An upstream port of a hub in SuperSpeedPlus operation shall transition to Polling.PortMatch to negotiate for alternative operation upon the 12ms timeout and the conditions to transition to Polling.Configuration are not met.	NT
7.5.4.10.2#12	An upstream port of a peripheral device in SuperSpeedPlus operation shall transition to Polling.PortMatch to negotiate for alternative operation upon the 12ms timeout and the conditions to transition to Polling.Configuration are not met.	NT
7.5.4.10.2#13	A downstream port shall transition from Polling.Idle to Rx.Detect when Reset is directed.	NT
7.5.4.10.2#14	An upstream port shall transition from Polling.Idle to Rx.Detect when Warm Reset is detected.	NT
Subsection reference: 7.5.5 Compliance Mode		
Subsection reference: 7.5.5.1 Compliance Mode Requirements		
7.5.5.1#1	The port shall maintain the low-impedance receiver termination (RRX-DC) when it is in Compliance Mode.	NT
7.5.5.1#2	Upon entry to Compliance Mode, the port shall wait until its SS Tx DC common mode voltage meets specification in Table 6-18 before it starts to send the first compliance test pattern.	NT
7.5.5.1#3	The port shall transmit the next compliance test pattern continuously upon detection of a Ping.LFPS when in Compliance Mode.	7.33 7.34
7.5.5.1#4	The port shall transmit the first compliance test pattern continuously upon detection of a Ping.LFPS and the test pattern has reached the final test pattern.	NT
Subsection reference: 7.5.5.2 Exit from Compliance Mode		
7.5.5.2#1	A downstream port shall transition from Compliance Mode to Rx.Detect when directed to issue Warm Reset.	7.34
7.5.5.2#2	An upstream port shall transition from Compliance Mode to Rx.Detect upon detection of Warm Reset.	7.33
Subsection reference: 7.5.6 U0		

Assertion #	Assertion Description	Test #
Subsection reference: 7.5.6.1 U0 Requirements		
7.5.6.1#1	The port shall maintain the low-impedance receiver termination (RRX-DC) in U0.	NT
7.5.6.1#2	The LFPS receiver shall be enabled in U0.	IOP
7.5.6.1#3	A port shall enable a 1-ms timer to measure the time interval between two consecutive link commands in U0.	7.16
7.5.6.1#4	A port shall enable a 10- μ s timer in U0. It shall be reset when the first symbol of any link command or packet is sent and restarted after the last symbol of any link command or packet is sent. This timer shall be active when the link is in logical idle.	NT
7.5.6.1#5	An upstream port shall transmit a single LUP when the 10- μ s timer expires in U0.	5.1
7.5.6.1#6	A downstream port shall transmit a single LDN when the 10- μ s timer expires in U0.	5.1
Subsection reference: 7.5.6.2 Exit from U0		
7.5.6.2#1	The port shall transition from U0 to Recovery upon detection of a TS1 ordered set.	NT
7.5.6.2#2	The port shall transition from U0 to Recovery when directed.	NT
7.5.6.2#3	The port shall transition from U0 to eSS.Inactive when PENDING_HP_TIMER times out for the fourth consecutive time.	NT
7.5.6.2#4	A downstream port shall transition from U0 to eSS.Inactive when directed.	NT
7.5.6.2#5	An upstream port shall transition from U0 to eSS.Disabled when directed.	NT
7.5.6.2#6	A downstream port shall transition from U0 to Recovery upon not receiving any link commands within 1 ms.	7.16
7.5.6.2#7	A downstream port shall transition from U0 to Rx.Detect when directed to issue Warm Reset.	NT
7.5.6.2#8	An upstream port shall transition from U0 to Rx.Detect when Warm Reset is detected.	NT
7.5.6.2#9	An upstream port shall transition from U0 to eSS.Disabled upon detection of VBUS off.	NT
7.5.6.2#10	A downstream port shall transition from U0 to eSS.Inactive upon tPortConfiguration timeout.	7.17
7.5.6.2#11	An upstream port shall transition from U0 to eSS.Disabled upon tPortConfiguration timeout.	7.17

Assertion #	Assertion Description	Test #
Subsection reference: 7.5.7 U1		
Subsection reference : 7.5.7.1 U1 Requirements		
7.5.7.1#1	The port shall maintain its low-impedance receiver termination (RRX-DC) in U1.	NT
7.5.7.1#2	The port shall enable U1 exit detect functionality in U1.	7.18 7.23
7.5.7.1#3	The port shall enable LFPS transmitter when it initiates the exit from U1.	IOP
7.5.7.1#4	The port shall enable its U2 inactivity timer upon entry to U1 when the U2 inactivity timer has a non-zero timeout value.	NT
7.5.7.1#5	A downstream port shall enable its Ping.LFPS detection in U1.	NT
7.5.7.1#6	A downstream port shall enable a 300-ms timer in U1. This timer will be reset and restarted when a Ping.LFPS is received.	NT
7.5.7.1#7	An upstream port shall transmit Ping.LFPS in U1.	NT
Subsection reference: 7.5.7.2 Exit from U1		
7.5.7.2#1	A downstream port shall transition from U1 to Rx.Detect when the 300-ms timer expires.	NT
7.5.7.2#2	A downstream port shall transition from U1 to RxDetect when directed to issue Warm Reset.	NT
7.5.7.2#3	An upstream port shall transition from U1 to Rx.Detect when Warm Reset is detected.	NT
7.5.7.2#4	A self-powered upstream port shall transition from U1 to eSS.Disabled upon not detecting valid VBUS.	NT
7.5.7.2#5	A port shall transition from U1 to U2 upon the timeout of the U2 inactivity timer.	NT
7.5.7.2#6	A port shall transition from U1 to Recovery upon completion of an LFPS handshake (U1 LFPS exit).	7.18 7.23
7.5.7.2#7	A port shall transition from U1 to eSS.Inactive upon the 2-ms LFPS handshake timer timeout if a successful LFPS handshake is not achieved.	NT
Subsection reference: 7.5.8 U2		
Subsection reference: 7.5.8.1 U2 Requirements		
7.5.8.1#1	A port shall maintain its low-impedance receiver termination (RRX-DC) in U2.	NT

Assertion #	Assertion Description	Test #
7.5.8.1#2	A port shall enable its U2 exit detect functionality when in U2.	7.19 7.24
7.5.8.1#3	A port shall enable its LFPS transmitter when it initiates the exit from U2.	NT
7.5.8.1#4	A downstream port shall perform a far-end receiver termination detection every 100 ms in U2.	NT
Subsection reference: 7.5.8.2 Exit from U2		
7.5.8.2#1	A downstream port shall transition from U2 to Rx.Detect upon detection of a far-end high-impedance receiver termination (ZRX-HIGH-IMP-DC-POS).	NT
7.5.8.2#2	A downstream port shall transition from U2 to Rx.Detect when directed to issue Warm Reset.	NT
7.5.8.2#3	An upstream port shall transition from U2 to Rx.Detect when Warm Reset is detected.	NT
7.5.8.2#4	A self-powered upstream port shall transition from U2 to eSS.Disabled upon not detecting valid VBUS.	NT
7.5.8.2#5	A port shall transition from U2 to Recovery upon successful completion of a LFPS handshake (U2 LFPS exit).	7.19 7.24
7.5.8.2#6	The port shall transition from U2 to eSS.Inactive upon the 2-ms LFPS handshake timer timeout if a successful LFPS handshake is not achieved.	NT
Subsection reference: 7.5.9 U3		
Subsection reference: 7.5.9.1 U3 Requirements		
7.5.9.1#1	The port shall maintain its low-impedance receiver termination (RRX-DC) in U3.	NT
7.5.9.1#2	LFPS Ping detection shall be disabled in U3. (Downstream port Only.)	NT
7.5.9.1#3	The port shall enable its U3 wakeup detect functionality in U3.	7.25
7.5.9.1#4	The port shall enable its LFPS transmitter when it initiates the exit from U3.	7.36
7.5.9.1#5	A downstream port shall perform a far-end receiver termination detection every 100 ms in U3.	NT
Subsection reference: 7.5.9.2 Exit from U3		

Assertion #	Assertion Description	Test #
7.5.9.2#1	A downstream port shall transition from U3 to Rx.Detect upon detection of a far-end high-impedance receiver termination (ZRX-HIGH-IMP-DC-POS).	NT
7.5.9.2#2	A downstream port shall transition from U3 to Rx.Detect when directed to issue Warm Reset.	7.35
7.5.9.2#3	An upstream port shall transition from U3 to Rx.Detect when Warm Reset is detected.	NT
7.5.9.2#4	A self-powered upstream port shall transition from U3 to eSS.Disabled upon not detecting valid VBUS.	NT
7.5.9.2#5	A port shall transition from U3 to Recovery upon successful completion of a LFPS handshake (U3 wakeup).	7.36 7.25
7.5.9.2#6	A port shall remain in U3 when the 10-ms LFPS handshake timer times out if a successful LFPS handshake is not achieved.	NT
7.5.9.2#7	A port in U3 100ms after an unsuccessful LFPS exit handshake and the requirement to exit U3 still exists shall initiate the U3 wakeup LFPS handshake to wake up the host.	NT
Subsection reference: 7.5.10 Recovery		
Subsection reference: 7.5.10.3 Recovery.Active		
Subsection reference: 7.5.10.3.1 Recovery.Active Requirements		
7.5.10.3.1#1	A port shall transmit the TS1 ordered sets upon entry to Recovery.Active.	7.26 7.30
7.5.10.3.1#2	A port shall train its receiver with TS1 or TS2 ordered sets in Recover.Active.	7.26 7.30
7.5.10.3.1#3	The port in SuperSpeedPlus operation shall insert a SYNC ordered set every 32 TS1 ordered sets.	BC
7.5.10.3.1#4	The port in SuperSpeedPlus operation shall perform block alignment and scrambler synchronization.	BC
Subsection reference: 7.5.10.3.2 Exit from Recovery.Active		
7.5.10.3.2#1	A port in SuperSpeed operation shall transition from Recovery.Active to Recovery.Configuration after eight consecutive and identical TS1 or TS2 ordered sets are received.	7.26 7.30
7.5.10.3.2#2	A port in SuperSpeedPlus operation shall transition from Recovery.Active to Recovery.Configuration after eight consecutive and identical TS1 or TS2 ordered sets are received, excluding symbols 14 and 15 of TS1 or TS2 ordered sets.	7.26 7.30

Assertion #	Assertion Description	Test #
7.5.10.3.2#3	A port shall transition from Recovery.Active to eSS.Inactive when either the Ux_EXIT TIMER or the 12-ms timer times out.	NT
7.5.10.3.2#4	A downstream port shall transition from Recovery.Active to eSS.Inactive when the transition to Recovery is not to attempt a Hot Reset AND the 12ms timer or Ux_EXIT_TIMER times out.	NT
7.5.10.3.2#5	A downstream port shall transition from Recovery.Active to Rx.Detect when the transition to Recovery is to attempt a Hot Reset AND the 12ms timer or the Ux_EXIT_TIMER times out.	7.31
7.5.10.3.2#6	A downstream port shall transition from Recovery.Active to Rx.Detect when directed to issue Warm Reset.	NT
7.2.10.3.2#7	An upstream port shall transition from Recovery.Active to Rx.Detect when Warm Reset is detected.	NT
Subsection reference: 7.5.10.4 Recovery.Configuration		
Subsection reference: 7.5.10.4.1 Recovery.Configuration Requirements		
7.5.10.4.1#1	The port shall transmit identical TS2 ordered sets upon entry to Recovery.Configuration and set the Reset bit, when directed.	7.28 7.29
7.5.10.4.1#2	If port that has Loopback Master Capability and is directed to go to Loopback, it shall transmit identical TS2 ordered sets with the Loopback bit set upon entry to Recovery.Configuration.	NT
7.5.10.4.1#3	If directed to disable scrambling, a port shall transmit identical TS2 ordered sets upon entry to this Recovery.Configuration with the Disabling Scrambling bit set.	NT
7.5.10.4.1#4	The port in SuperSpeedPlus operation shall insert a SYNC ordered set every 32 TS2 ordered sets.	BC
7.5.10.4.1#5	The port in SuperSpeedPlus operation shall perform block alignment and scrambler synchronization.	BC
Subsection reference: 7.5.10.4.2 Exit from Recovery.Configuration		
7.5.10.4.2#1	The port in SuperSpeed operation shall transition from Recovery.Configuration to Recovery.Idle after the following two conditions are met: <ul style="list-style-type: none"> Eight consecutive and identical TS2 ordered sets are received. Sixteen TS2 ordered sets are sent after receiving the first of the eight consecutive and identical TS2 ordered sets. 	7.26 7.30
7.5.10.4.2#2	The port in SuperSpeedPlus operation shall transition from Recovery.Configuration to Recovery.Idle after the following two conditions are met:	7.26 7.30

Assertion #	Assertion Description	Test #
	<ul style="list-style-type: none"> Eight consecutive and identical TS2 ordered sets, excluding symbols 14 and 15, are received. Sixteen TS2 ordered sets are sent after receiving the first of the eight consecutive and identical TS2 ordered sets, excluding symbols 14 and 15. 	
7.5.10.4.2#3	A port shall transition from Recovery.Active to eSS.Inactive when either the Ux_EXIT TIMER or the 6-ms timer times out.	NT
7.5.10.4.2#4	A downstream port shall transition from Recovery.Active to eSS.Inactive when the transition to Recovery is not to attempt a Hot Reset AND the 6ms timer or Ux_EXIT_TIMER times out.	NT
7.5.10.3.2#5	A downstream port shall transition from Recovery.Active to Rx.Detect when the transition to Recovery is to attempt a Hot Reset AND the 6ms timer or the Ux_EXIT_TIMER times out.	7.31
7.5.10.4.2#6	A downstream port shall transition from Recovery.Configuration to Rx.Detect when directed to issue Warm Reset.	NT
7.5.10.4.2#7	An upstream port shall transition from Recovery.Configuration to Rx.Detect when Warm Reset is detected.	NT
Subsection reference: 7.5.10.5 Recovery.Idle		
Subsection reference: 7.5.10.5.1 Recovery.Idle Requirements		
7.5.10.5.1#1	A port in SuperSpeed operation shall transmit Idle Symbols in Recovery.Idle if the next state is U0.	7.26 7.30
7.5.10.5.1#2	A port in SuperSpeed operation shall enable scrambling by default in Recovery.Idle.	7.26 7.30
7.5.10.5.1#3	A port in SuperSpeed operation shall disable the scrambling when directed, or when the Disabling Scrambling bit is asserted in the TS2 ordered set received in Recovery.configuration.	NT
7.5.10.5.1#4	A port in SuperSpeedPlus operation shall transmit a single SDS ordered set before the start of the data blocks with Idle Symbols if the next state is U0.	BC
7.5.10.5.1#5	A port in SuperSpeedPlus operation shall disable the scrambling upon completion of SDS ordered set transmission if directed or if the Disabling Scrambling bit is asserted in the TS2 ordered set received in Recovery.Configuration.	NT
7.5.10.5.1#6	A port shall be able to receive the Header Sequence Number Advertisement from its link partner in Recovery.Idle.	NT
Subsection reference: 7.5.10.5.2 Exit from Recovery.Idle		
7.5.10.5.2#1	A port shall transition from Recovery.Idle to Loopback when directed as a loopback master if the port is capable of being a loopback master.	NT

Assertion #	Assertion Description	Test #
7.5.10.5.2#2	A port shall transition from Recovery.Idle to Loopback as a loopback slave when the Loopback bit is asserted in TS2 ordered sets.	NT
7.5.10.5.2#3	A port shall transition from Recovery.Idle to U0 when the following two conditions are met: <ul style="list-style-type: none"> Eight consecutive Idle Symbols are received. Sixteen Idle Symbols are sent after receiving one Idle Symbol. 	7.26 7.30
7.5.10.5.2#4	A port shall transition from Recovery.Idle to eSS.Inactive when Ux_EXIT_TIMER or the 2-ms timer times out if the conditions to transition to U0 are not met.	NT
7.5.10.5.2#5	A downstream port shall transition from Recovery.Idle to Hot Reset when directed.	NT
7.5.10.5.2#6	A downstream port shall transition from Recovery.Idle to Rx.Detect when directed to issue Warm Reset.	NT
7.5.10.5.2#7	An upstream port shall transition from Recovery.Idle to Rx.Detect when Warm Reset is detected.	NT
7.5.10.5.2#8	An upstream port shall transition from Recovery.Idle to Hot Reset when the Reset bit is asserted in TS2 ordered sets.	NT
Subsection reference: 7.5.11 Loopback		
Subsection reference: 7.5.11.3.1 Loopback.Active Requirements		
7.5.11.3.1#1	A loopback master shall send valid 8b/10b data with SKPs as necessary when in Loopback.Active.	NT
7.5.11.3.1#2	A loopback slave shall retransmit the received 10-bit symbols when in Loopback.Active.	NT
7.5.11.3.1#3	A loopback slave shall not modify the received 10-bit symbols in Loopback.Active. (Other than SKP ordered set, which may be added or dropped.)	NT
7.5.11.3.1#4	The loopback slave shall process the BERT commands in Loopback.Active.	NT
7.5.11.3.1#5	The LFPS receiver shall be enabled in Loopback.Active.	NT
Subsection reference: 7.5.11.3.2 Exit from Loopback.Active		
7.5.11.3.2#1	A downstream port shall transition from Loopback.Active to Rx.Detect when directed to issue Warm Reset.	NT
7.5.11.3.2#2	An upstream port shall transition from Loopback.Active to Rx.Detect when Warm Reset is detected.	NT

Assertion #	Assertion Description	Test #
7.5.11.3.2#3	When directed, loopback master shall transition from Loopback.Active to Loopback.Exit.	NT
7.5.11.3.2#4	A loopback slave shall transition from Loopback.Active to Loopback.Exit upon detection of Loopback LFPS exit handshake.	NT
Subsection reference: 7.5.11.4 Loopback.Exit		
Subsection reference: 7.5.11.4.1 Loopback.Exit Requirements		
7.5.11.4.1#1	A LFPS transmitter and the LFPS receiver shall be enabled in Loopback.Exit.	NT
7.5.11.4.1#2	A port shall transmit and receive Loopback LFPS exit handshake in Loopback.Exit.	NT
Subsection reference: 7.5.11.4.2 Exit from Loopback.Exit		
7.5.11.4.2#1	A port shall transition from Loopback.Exit to Rx.Detect upon a successful Loopback LFPS exit handshake.	NT
7.5.11.4.2#2	A port shall transition from Loopback.Exit to eSS.Inactive upon the 2-ms timer timeout if the condition to transition to Rx.Detect is not met	NT
7.5.11.4.2#3	A downstream port shall transition from Loopback.Exit to Rx.Detect when directed to issue Warm Reset.	NT
7.5.11.4.2#4	An upstream port shall transition from Loopback.Exit to Rx.Detect when Warm Reset is detected.	NT
Subsection reference: 7.5.12 Hot Reset		
Subsection reference: 7.5.12.2 Hot Reset Requirements		
7.5.12.2#1	A downstream port shall reset its PM timers and the U1 and U2 timeout value to zero in Hot Reset.	NT
Subsection reference: 7.5.12.3 Hot Reset.Active		
Subsection reference: 7.5.12.3.1 Hot Reset.Active Requirements		
7.5.12.3.1#1	Upon entry to this Hot Reset.Active, the port shall first transmit at least 16 TS2 ordered sets continuously with the Reset bit asserted.	7.27-29
7.5.12.3.1#2	In Hot Reset.Active a downstream port shall continue to transmit TS2 ordered sets with the Reset bit asserted until the upstream port transitions from sending TS2 ordered sets with the Reset bit asserted to sending the TS2 ordered sets with the Reset bit de-asserted.	7.29
7.5.12.3.1#3	An upstream port shall transmit TS2 ordered sets with the Reset bit asserted while performing the Hot Reset.	7.27-28

Assertion #	Assertion Description	Test #
7.5.12.3.1#4	An upstream port shall transmit TS2 ordered sets with the Reset bit de-asserted after completing the Hot Reset.	7.27-28
Subsection reference: 7.5.12.3.2 Exit from Hot Reset.Active		
7.5.12.3.2#1	The port shall transition to Hot Reset.Exit when the following three conditions are met: <ul style="list-style-type: none"> At least 16 TS2 ordered sets with the Reset bit asserted are transmitted. Two consecutive TS2 ordered sets are received with the Reset bit de-asserted. Four consecutive TS2 ordered set with the Reset bit de-asserted are sent after receiving one TS2 ordered set with the Reset bit de-asserted. 	7.27-29
7.5.12.3.2#2	The port shall transition from Hot Reset.Active to eSS.Inactive upon the 12-ms timer timeout if the conditions to transition to Hot Reset.Exit are not met.	NT
7.5.12.3.2#3	A downstream port shall transition from Hot Reset.Active to Rx.Detect when directed to issue Warm Reset.	NT
7.5.12.3.2#4	An upstream port shall transition from Hot Reset.Active to Rx.Detect when Warm Reset is detected.	NT
Subsection reference: 7.5.12.4 Hot Reset.Exit		
Subsection reference: 7.5.12.4.1 Hot Reset.Exit Requirements		
7.5.12.4.1#1	A port in SuperSpeed operation shall transmit idle symbols in Hot Reset.Exit.	7.27-29
7.5.12.4.1#2	A port in SuperSpeedPlus operation shall transmit a single SDS ordered set before the start of the data block with Idle Symbols.	7.27-29
7.5.12.4.1#3	The port shall be able to receive the Header Sequence Number Advertisement from its link partner in Hot Reset.Exit.	NT
Subsection reference: 7.5.12.4.2 Exit from Hot Reset.Exit		
7.5.12.4.2#1	The port shall transition from Hot Reset.Exit to U0 when the following two conditions are met: <ul style="list-style-type: none"> Eight consecutive Idle Symbols are received. Sixteen Idle Symbols are sent after receiving one Idle Symbol. 	7.27-29
7.5.12.4.2#2	The port shall transition from Hot Reset.Exit to eSS.Inactive upon the 2-ms timer timeout if the conditions to transition to U0 are not met.	NT
7.5.12.4.2#3	A downstream port shall transition from Hot Reset.Exit to Rx.Detect when directed to issue Warm Reset.	NT

Assertion #	Assertion Description	Test #
7.5.12.4.2#4	An upstream port shall transition from Hot Reset.Exit to Rx.Detect when Warm Reset is detected.	NT
Chapter 8 Test Assertions: Protocol Layer		
Subsection reference: 8.3 Packet Formats		
Subsection reference: 8.3.1 Fields Common to all Headers		
Subsection reference: 8.3.1.1 Reserved Values and Reserved Field Handling		
8.3.1.1#1	A receiver shall ignore any Reserved field.	PT 7.6
8.3.1.1#2	A receiver shall ignore any packet that has any of its defined fields set to a reserved value, but it shall acknowledge the packet and return credit for the same.	NT
Subsection reference: 8.4 Link Management Packet (LMP)		
Subsection reference: 8.4.2 Set Link Function		
8.4.2#1	Upon receipt of an LMP with the Force_LinkPM_Accept bit asserted, the upstream port shall accept all LGO_U1 and LGO_U2 Link Commands until the port receives an LMP with Force_LinkPM_Accept bit is de-asserted.	7.23-24
Subsection reference: 8.4.4 Vendor Device Test		
8.4.4#1	The Vendor Device Test LMP shall not be used during normal operation of the link.	NT
Subsection reference: 8.4.5 Port Capabilities		
8.4.5#1	The port shall send the Port Capability LMP within tPortConfiguration time after completion of link initialization.	5.1 7.17
8.4.5#2	When the link partner that has downstream capability does not receive the Port Capability LMP within tPortConfiguration time, it shall signal an error.	NT
8.4.5#3	When the link partner that only supports upstream capability does not receive Port Capability LMP within tPortConfiguration time, it shall transition to SS.Disabled and try to connect at the other speeds this device supports.	7.17
8.4.5#4	After exchanging Port Capability LMPs, the link partners shall determine which of the link partners shall be configured as the downstream facing port.	7.38
Subsection reference: 8.4.6 Port Configuration		

Assertion #	Assertion Description	Test #
8.4.6#1	All Enhanced SuperSpeed ports that supports downstream port capability shall be capable of sending the Port Configuration LMP.	5.1
8.4.6#2	When the port that was to be configured in the upstream facing mode does not receive the Port Configuration LMP within tPortConfiguration time after link initialization, the upstream port shall transition to eSS.Disabled and try and connect at the other speeds this device supports.	7.17
8.4.6#3	A port configured in the downstream mode shall send the Port Configuration LMP to the upstream port.	7.17
8.4.6#4	The port sending the Port Configuration LMP shall select only one bit for the Link Speed field.	NT
8.4.6#5	The Link Speed field shall only be used when the port is operating at Gen 1 speed.	TBD
8.4.6#6	When a downstream capable port cannot work with its link partner, it shall signal an error as described in Section 10.14.2.6.	NT
Subsection reference: 8.4.7 Port Configuration Response		
8.4.7#1	All Enhanced SuperSpeed ports that supports upstream port capability shall be capable of sending the Port Configuration Response LMP.	5.1
8.4.7#2	When the downstream port does not receive the Port Configuration Response LMP within tPortConfiguration time, it shall signal an error as described in Section 10.14.2.6.	NT
8.4.7#3	When the Response Code indicates that the Link Speed was rejected by the upstream port, the downstream port shall signal an error as described in Section 10.14.2.6.	NT
Subsection reference: 8.4.8 Precision Time Measurement		
Subsection reference: 8.4.8.1 PTM Bus Interval Boundary Counters		
8.4.8.1#1	The PTM Delta Counter shall be incremented by the PTM Clock to measure the delay from present time to the previous bus interval boundary.	NT
8.4.8.1#2	The PTM Bus Interval Counter shall be incremented when the PTM Delta Counter wraps.	NT
8.4.8.1#3	Hosts shall implement a set of PTM Bus Interval Boundary Counters.	NT
8.4.8.1#4	PTM capable devices shall implement PTM Bus Interval Boundary Counters.	NT
Subsection reference: 8.4.8.2 LDM Protocol		

Assertion #	Assertion Description	Test #
8.4.8.2#1	If an LDM Message is received by a port that does not support PTM, then the packet shall be dropped. Note that the port shall acknowledge the packet and return credit for the same as per the requirement specified in Section 7.2.4.1.	NT
8.4.8.2#2	LDM timestamps shall reference the first framing symbol of a received or transmitted LDM LMP.	NT
Subsection reference: 8.4.8.3 LDM State Machines		
Subsection reference: 8.4.8.3.1 Requester Operation		
8.4.8.3.1#1	The LDM Requester State Machine shall maintain the local variable Init Response Timeout Counter.	NT
8.4.8.3.1#2	The LDM Requester State Machine shall maintain the local timer Response Timer.	NT
Subsection reference: 8.4.8.3.1.1 Init Request		
8.4.8.3.1.1#1	Upon entering this state, the Requester shall set the LDM Enabled flag to 1.	NT
8.4.8.3.1.1#2	The Init Response Timeout Counter shall be initialized to 0 at power up, or if the Init Request state is entered from the LDM Disabled or Timestamp Response states.	NT
8.4.8.3.1.1#3	If the Init Request state is entered from the Init Response state, then the Init Response Timeout Counter shall not be changed.	NT
8.4.8.3.1.1#4	When a trigger event occurs, the Requester shall transmit a LDM TS Request LMP to the Responder, save timestamp t1 from the Local Time Source in the LDM Context to record the time that the LDM Request was transmitted, and transition to the Init Response state.	NT
Subsection reference: 8.4.8.3.1.2 Init Response		
8.4.8.3.1.2#1	Upon entering this state, the Requester shall increment the Init Response Timeout Counter, start the Response Timer and wait for a TS Response LMP or a timeout.	NT
8.4.8.3.1.2#2	If a LDM TS Response LMP and LCW Delayed (DL)=0 is received, the Requester shall save timestamp t4 from the Local Time Source in the LDM Context to record the time that the LDM Response was received, then calculate the LDM Link Delay and set the LDM Valid flag to 1, and transition to the Timestamp Request state.	NT
8.4.8.3.1.2#3	If a LDM TS Response LMP and LCW Delayed (DL)=1 is received, the Requester shall consider the Response Delay field of the LDM TS Response LMP invalid, invalidate the LDM Context t1, t2, and t3 timestamps, immediately generate a Trigger Event to initiate another Exchange, and transition to the Timestamp Request state.	NT

Assertion #	Assertion Description	Test #
8.4.8.3.1.2# 4	If an Init Response Timeout occurs and the Init Response Timeout Counter is less than 3, then the Requester shall increment the Init Response Timeout Counter and transition to the Init Request state.	NT
8.4.8.3.1.2# 5	If an Init Response Timeout occurs and the Init Response Timeout Counter is equal to 3, then the Requester shall transition to the LDM Disabled state.	NT
Subsection reference: 8.4.8.3.1.3 Timestamp Request		
8.4.8.3.1.3# 1	Upon entering this state, the Requester shall wait for a Trigger Event.	NT
8.4.8.3.1.3# 2	When a trigger event occurs, the Requester shall transmit a LDM Timestamp (TS) Request LMP to the Responder, save timestamp t1 from the Local Time Source in the LDM Context to record the time that the LDM Request was transmitted, and transition to the Timestamp Response state.	NT
8.4.8.3.1.3# 3	Timestamp t1 shall be adjusted for the TS Delay.	NT
Subsection reference: 8.4.8.3.1.4 Timestamp Response		
8.4.8.3.1.4# 1	Upon entering this state, the Requester shall start the Response Timer and wait for a LDM TS Response LMP or a timeout.	NT
8.4.8.3.1.4# 2	If a LDM TS Response LMP is received and the LCW Delayed (DL) flag is zero, the Requester shall save timestamp t4 from the Local Time Source in the LDM Context to record the time that the LDM Response was received, then calculate the LDM Link Delay, set the LDM Valid flag to 1, and transition to the Timestamp Request state.	NT
8.4.8.3.1.4# 3	If a LDM TS Response LMP is received and the LCW Delayed (DL) flag is one, the Requester shall consider the Response Delay field of the LDM TS Response LMP invalid, invalidate the LDM Context t1, t2, and t3 timestamps, immediately generate a Trigger Event to initiate another Timestamp Exchange, and transition to the Timestamp Request state.	NT
8.4.8.3.1.4# 4	If a Response Timeout occurs the Requester shall transition to the Init Request state, where the LDM state machine will attempt to retry the Timestamp Exchange with the Responder.	NT
8.4.8.3.1.4# 5	Timestamp t4 shall be adjusted for the TS Delay.	NT
Subsection reference: 8.4.8.3.1.5 LDM Disabled		
8.4.8.3.1.5# 1	Upon entering this state, the Requester shall clear the LDM_ENABLE flag and terminate all LDM protocol activity.	NT

Assertion #	Assertion Description	Test #
8.4.8.3.1.5# 2	When the device receives a CLEAR_FEATURE(LDM_ENABLE) request it shall transition from any other LDM state to the LDM Disabled state.	NT
8.4.8.3.1.5# 3	When the device receives a SET_FEATURE(LDM_ENABLE) request it shall transition to the Init Request state.	NT
Subsection reference: 8.4.8.3.2 Responder Operation		
8.4.8.3.2#1	The LDM Responder State Machine shall maintain the local variable Responder Response Delay Overflow.	NT
Subsection reference: 8.4.8.3.2.1 Responder Disabled		
8.4.8.3.2.1# 1	Upon entering this state the Responder shall terminate all LDM protocol activity.	NT
8.4.8.3.2.1# 2	If LDM Enabled equals 0, then the Responder shall transition from any other LDM state to the Responder Disabled state.	NT
8.4.8.3.2.1# 2	If LDM Enabled equals 1, then the Responder shall transition to the Timestamp Request state.	NT
Subsection reference: 8.4.8.3.2.2 Timestamp Request		
8.4.8.3.2.2# 1	Upon entering this state the Responder shall wait for a LDM TS Request LMP.	NT
8.4.8.3.2.2# 2	If a LDM TS Request LMP is received, the Responder shall capture timestamp t2 from the PTM Local Time Source to record the time that the LDM TS Request was received and transition to the Timestamp Response state.	NT
8.4.8.3.2.2# 3	Timestamp t2 shall be adjusted for the TS Delay.	NT
Subsection reference: 8.4.8.3.2.3 Timestamp Response		
8.4.8.3.2.3# 1	Upon entering this state the Responder shall wait for a Trigger Event.	NT
8.4.8.3.2.3# 2	When a Trigger Event occurs, the Responder shall capture timestamp t3 from the PTM Local Time Source to record the time that the LDM Response was transmitted.	NT
8.4.8.3.2.3# 3	If the value $t3 - t2$ is less than $tLDMResponseDelay$, the Responder shall form a LDM TS Response LMP by initializing the Response Delay field with the value $t3 - t2$, transmit the LDM TS Response LMP to the Requester, and transition to the Timestamp Request state.	NT
8.4.8.3.2.3# 4	If the value $t3 - t2$ is equal to or greater than $tLDMResponseDelay$, then the Responder shall transition to the Timestamp Request state.	NT

Assertion #	Assertion Description	Test #
8.4.8.3.2.3#5	The timestamp t3 shall be adjusted for the TS Delay.	NT
8.4.8.3.2.3#6	A Responder shall set the LCW Delayed (DL) flag and re-calculate CRC-5 if a LDM TS Response LMP is delayed if its adjusted Response Delay value exceeds tLDMRequestTimeout.	NT
Subsection reference: 8.4.8.5 PTM Bus Interval Boundary Device Calculation		
8.4.8.5#1	If Delta(RxITP) is greater than or equal to 7500, the device shall ignore the ITP.	NT
8.4.8.5#2	If Delta(RxITP) is less than 7500, the device shall apply Delta(RxITP) and Correction(RxITP) values and the LDM Link Delay to set the value of the PTM Delta Counter at the time an ITP is received (tITUFP) using the formula shown (see section 8.4.8.5).	NT
8.4.8.5#3	If Delta(RxITP) is less than 7500, a device shall use the values of Bus Interval Counter(RxITP) and Delta(RxITP) subfields received in the ITP to set the value of the PTM But Interval Counter at the time an ITP is received (tITUFP) using the formula shown (see section 8.4.8.5).	NT
Subsection reference: 8.4.8.6 PTM Bus Interval Boundary Host Calculation		
8.4.8.6#1	A host shall maintain an ITP Delay Counter that is incremented by the PTM Clock.	NT
8.4.8.6#2	The host shall transmit downstream ITPs using these current values for the ITP Isochronous Timestamp Bus Interval Counter(TxITP) and Delay(TxITP) fields, and set the Correction(TxITP) field to zero.	NT
Subsection reference: 8.4.8.7 PTM Hub ITP Regeneration		
8.4.8.7#1	A hub shall maintain an ITP Delay Counter that is incremented by the PTM Clock.	NT
8.4.8.7#2	If an ITP is received by a PTM capable hub and the Delayed(DL) bit is not set, then the hub shall set the ITP Delay Counter to zero and for each downstream port in U0, the hub shall queue the ITP for transmission.	NT
8.4.8.7#3	When a PTM capable hub transmits an ITP, it shall copy the value of Bus Interval Boundary(RxITP) to the BUS Interval Boundary(TxITP) subfield of the Isochronous Timestamp field in the downstream ITP.	NT
8.4.8.7#4	When a PTM capable hub transmits an ITP, it shall calculate the value of Delta(TxITP) subfield using the formula shown (see section 8.4.8.7).	NT
8.4.8.7#5	When a PTM capable hub transmits an ITP, it shall re-calculate the CRC-16 for the modified ITP.	NT

Assertion #	Assertion Description	Test #
8.4.8.7#6	If an ITP is received by a PTM capable hub and the Delayed (DL) bit is set, then the hub shall forward the received ITP without modification.	NT
8.4.8.7#7	The Isochronous Timestamp values used in the ITP being transmitted shall be the values present at the time of transmission (not time queued for transmission but actual transmission, see section 8.4.8.6).	NT
Subsection reference: 8.4.8.9 LDM Rules		
8.4.8.9#1	A Responder shall not send a LDM Response without first receiving a LDM Request LMP.	NT
8.4.8.9#2	A Responder shall capture the PTM Local Clock Source timestamps (t2 and t3) when transmitting LDM Response and when receiving LDM request LMPs.	NT
8.4.8.9#3	A Responder shall issue LDM Response LMP when it possesses the timing values required to populate the LDM Response LMP: timestamps (t2-t3 in Figure 8-11).	NT
8.4.8.9#4	A Requester shall capture t1 timestamps upon transmitting the last symbol of a LDM Request.	NT
8.4.8.9#5	A Responder shall capture t2 timestamps upon receiving the last symbol of a LDM Request.	NT
8.4.8.9#6	A Responder shall capture t3 timestamps upon transmitting the last symbol of a LDM Response.	NT
8.4.8.9#7	A Requester shall capture t4 timestamps upon receiving the last symbol of a LDM Response.	NT
Subsection reference: 8.4.8.10 LDM and Hubs		
8.4.8.10#1	On a hub, when both LDM Enabled and LDM Valid in the Requester State Machine transition to 1, then all of the hub's Responder State Machine shall transition to the Init Request state.	NT
Subsection reference: 8.6 Data Packet (DP)		
8.6#1	If no endpoints on this device have packets pending, then the device can use this information to aggressively manage its upstream link, e.g., set the link to a lower power U1 or U2 state.	7.37
Chapter 10 Test Assertions: Hub, Host Downstream Port, and Device Upstream Port Specification		
Subsection reference: 10.2 Hub Power Management		
Subsection reference: 10.2.2 Hub Downstream Port U1/U2 Timers		

Assertion #	Assertion Description	Test #
10.2.2#6	If a hub has received a valid packet on its upstream port that is routed to a downstream port, it shall reject U1 or U2 link entry attempts on the downstream port until the packet has been successfully transmitted.	NT
10.2.2#7	Hub implementation ensures no race condition when a header packet that has not been deferred is queued for transmission on a downstream port with a link that is in U1, U2, or is in the process of entering U1, U2	NT
Subsection reference: 10.3: Hub Downstream Facing Ports		
Subsection reference: 10.3.1: Hub Downstream Facing Port State Descriptions		
Subsection reference: 10.3.1.6: DSPORT.Resetting		
10.3.1.6#6	If the port initiates a hot reset on the link and the hot reset TS1/TS2 handshake fails, a warm reset is automatically tried.	7.31
10.3.1.6#7	When the downstream port link enters Rx.Detect.Active during a warm reset, the hub shall start a timer to count the time it is in Rx.Detect.Active. If this timer exceeds tTimeForResetError while the link remains in Rx.Detect.Active, the port shall transition to the DSPORT.Disconnected state.	7.32
Subsection reference: 10.4 Hub Downstream Facing Port Power Management		
Subsection reference: 10.4.2 Hub Downstream Facing Port State Descriptions		
Subsection reference: 10.4.2.1 Enabled U0 States		
10.4.2.1#14	Hub shall ensure that there is no race condition between a link partner initiating a U1/U2 request and transitioning to U0 based on SetPortFeature(PORT_LINK_STATE) request.	NT
XHCl Specification Chapter 5 Test Assertions: Register Interface		
Subsection reference: xHCl 5.4 Host Controller Operational Registers		
Subsection reference: xHCl 5.4.8 Port Status and Control Register (PORTSC)		
5.4.8	The xHC shall set the PLC bit of the PORTSC register of a USB3 port to '1' when an Error occurs (the link transitions from any state -> Inactive).	NT

4 Timing Definitions

The USB 3.1 Specification defines the timers used in the Link Layer. To accurately test timer implementations, there are several considerations beyond the simple timer definition that factor into this document's timing scheme. Section 7.5 of the USB 3.1 Specification defines the link layer timers to have an implementation tolerance of +50%. Chapter 6 details an SSC Tolerance of -5300/+300ppm, the lower limit of which could add 0.5% time to any interval. Consideration for Physical Layer and Link Layer processing time (Tx and Rx latency time) is also applied.

The following expression is used for determining each timer's high-end value used in this specification:

$$\text{Spec Defined Timer value} \times \text{Additional50pctTolerance} \times \text{SSCFactor} + \text{tLinkTurnAround}$$

Spec Defined Timer value = the timer value defined in USB 3.1 specification.

Additional50pctTolerance = +50% tolerance defined in the Section 7.5 of the USB 3.1 specification.

SSCFactor = delay induced by SSC influenced clock with a maximum SSC of 5000ppm applied, equating to +0.5%.

tLinkTurnAround = tDHPResponse – tDPacket.

This is understood to be the maximum delay induced by the PHY and Link layers when a link event occurs, until the respective action is made, when there is no other packet processing occurring on the port. This is measured from the time a packet is received, until the time a response is generated on the transmit side.

For a PUT operating at Gen 1:

$$\text{tLinkTurnaround} = \text{tDHPResponse} - \text{tDPacket} = 2540\text{ns} - 2140\text{ns} = 400\text{ns}$$

For a PUT operating at Gen 2:

$$\text{tLinkTurnaround} = \text{tDHPResponse} - \text{tDPacket} = 1610\text{ns} - 910\text{ns} = 700\text{ns}$$

Note: Since captive re-timer delay is included in tDHPResponse and not factored out for tLinkTurnaround, a PUT that does not contain a captive re-timer can use the extra time for its Tx and Rx Data Paths.

Using their respective numerical values, the expression is presented again below:

$$\text{Spec Defined Timer value} \times 1.5 \times 1.005 + \text{tLinkTurnaround}$$

The expression above is applicable for Link Layer timers.

$$\text{Spec Defined Timer value} \times 1.005 + \text{tLinkTurnaround}$$

The expression above is applicable for PHY and protocol layer timers.

The following table lists the timers used in the Link Layer compliance tests and the window of compliant durations between the initial event that started the timer, and the expected response when the timer expires.

PORT_U2_TIMEOUT is not listed in the table because its value is programmable using the U2 Inactivity Timeout LMP. A calculation is needed as per the value programmed.

tPollingLFPSEstablishedTimeout was created from USB 3.1 Specification section 7.5.4.3.1: A Port shall establish its LFPS operating condition within 80us.

tRecoveryTimeout was created as a replacement for tLinkTurnaround when an error occurs that should result in a quick transition to Recovery. This mechanism may be implemented separately from tLinkTurnaround logic. Both Gen 1 and Gen 2 PUTs are given 1us to enter recovery for TDs 7.13, 7.14, 7.15, and 7.30.

Timer definition	Deadline (USB 3.1 specification defined value)	Expiration (Calculated test time) (Gen 1)	Expiration (Calculated test time) (Gen 2)
tDHPResponse (Gen 1)	2540ns		
tDHPResponse (Gen 2)	1610ns		
tDPacket (Gen 1)	2150ns		
tDPacket (Gen 2)	910ns		
tLinkTurnAround		400ns	700ns
tRxDetectQuietTimeoutUFP	12ms	18.0904ms	18.0907ms
tRxDetectQuietTimeoutDFP	12ms	120ms	120ms
tPollingLFPSTimeout	360ms	542.7004ms	542.7007ms
tPollingLFPSEstablishedTimeout		80us	80us
tPollingSCDLFPSTimeout	60us	90.850us	91.150us
tPollingLBPMLFPSTimeout	12ms	18.0904ms	18.0907ms
tPollingActiveTimeout	12ms	18.0904ms	18.0907ms
tPollingConfigurationTimeout	12ms	18.0904ms	18.0907ms
tRecoveryActiveTimeout	12ms	18.0904ms	18.0907ms
tRecoveryConfigurationTimeout	6ms	9.0454ms	9.0457ms
tRecoveryTransition		1us	1us
tU0RecoveryTimeout	1ms	1.5079ms	1.5082ms
tHotResetActiveTimeout	12ms	18.0904ms	18.0907ms
[Type 1/Type 2] CREDIT_HP_TIMER	5ms	7.5379ms	7.5382ms
PENDING_HP_TIMER	10μs	15.475μs	15.775μs
PM_LC_TIMER	4μs	6.43μs	6.73μs
PM_ENTRY_TIMER	8μs	12.46μs	12.76μs
Ux_EXIT_TIMER	6ms	9.0454ms	9.0457ms
tPortConfiguration	20μs	30μs	30μs
tNoLFPSTimeout for U1/2	2ms	2.0104ms	2.0107ms
tNoLFPSTimeout for U3	10ms	10.0504ms	10.0507ms
tU3WakeupRetryDelay	100ms	150.7504ms	150.7507ms

Table 4-1

Note +/- 100ns applies to Timer Expiration Times in Table 4-1 above.

5 Test Descriptions

5.1 Link Initialization Sequence

Most of the following test descriptions (TDs) refer to the Link Initialization Sequence, described here. The purpose of the Link Initialization Sequence is to establish the link between the LVS and the PUT and check that link establishment and initialization is followed properly by the PUT.

Some tests are designed to follow the Link Initialization Sequence up to a certain point and then introduce different test steps. This is reflected in each specific TD.

Link training is different for Gen 1 and Gen 2 capable PUTs during Polling substates. The verification checks on these substates are performed during TD 7.1.

Covered Assertions

7.2.4.1.1#6,8,10-17,22

7.2.4.1.4#2

7.3.4#2

7.5.6.1#5,6

8.4.5#1

8.4.6#1,3 (downstream)

8.4.7#1 (upstream)

Link Initialization Sequence

1. The LVS and the PUT go through the initial steps of the LTSSM (eSS.Disabled, Rx.Detect, Polling) to reach U0.
2. Once in U0, the LVS will transmit the Header Sequence Number Advertisement and
 - a. In Gen 1 speed, the Rx Header Buffer Credit Advertisement.
 - b. In Gen 2 speeds, the Type 1 and Type 2 Rx Header Buffer Credit Advertisements.
3. The LVS verifies that:
 - a. The Header Sequence Number Advertisement transmitted by the PUT is LGOOD_7
 - b. A Gen 2 PUT transmits the following Type 1 and Type 2 Rx Header Buffer Credit Advertisements: LCRD1_A, LCRD1_B, LCRD1_C, LCRD1_D, LCRD2_A, LCRD2_B, LCRD2_C, LCRD2_D.
 - c. A Gen 1 PUT transmits the following Rx Header Buffer Credit Advertisements: LCRD_A, LCRD_B, LCRD_C and LCRD_D.
4. The LVS and the PUT will exchange Port Configuration transactions.
 - If the LVS is configured as a Downstream Port:
 - a. LVS waits for the PUT's Port Capability LMP.
 - b. LVS verifies that the Port Capability LMP is valid.
 - c. LVS transmits its Port Capability LMP.
 - d. LVS transmits a valid Port Configuration LMP to the PUT.

- e. LVS waits for the PUT Port Configuration Response LMP.
- f. LVS verifies that the Port Configuration Response LMP is valid.
- If the LVS is configured as an Upstream Port:
 - a. LVS waits for the PUT's Port Capability LMP.
 - b. LVS verifies that the Port Capability LMP is valid.
 - c. LVS transmits its Port Capability LMP.
 - d. LVS waits for the PUT to transmit the Port Configuration LMP.
 - e. LVS verifies that the Port Configuration LMP is valid.
 - f. LVS transmits a Port Configuration Response LMP to the device.
- 5. The test fails if the Port Configuration transaction is not completed before tPortConfiguration expires.
- 6. The LVS will keep the link active by sending Link Pollings (LUP when it is configured as an Upstream Port or LDN when it is configured as a Downstream Port) for 50ms.
- 7. The Link Initialization Sequence passes if the exchanges are successful, no timeout is detected, no recovery is entered, all packets are successfully received, all credits are restored and the link stays in U0 for at least 50ms.

5.2 Physical Layer

TD.6.1 Lane Polarity Inversion Test

This test verifies that the PUT can successfully handle reception of lane polarity inversion.

Covered Assertions

(No Physical Layer assertions defined)

7.5.4.4.1#1

Overview of Test Steps

1. Invert the LVS TX lane polarity.
2. Bring the link to U0 using the Link Initialization Sequence.
3. The test passes if the Link Initialization Sequence passes.

TD.6.2 SKP Test

This test verifies that the PUT supports all possible skip (SKP) combinations.

Combinations to be tested for Gen 1 PUT:

- A. Repetition of one skip ordered set followed by 354 symbols (word aligned)
- B. Repetition of one skip ordered set followed by 353 symbols (word misaligned)
- C. Repetition of two skip ordered sets followed by 708 symbols (word aligned)
- D. Repetition of two skip ordered sets followed by 707 symbols (word misaligned)
- E. Repetition of three skip ordered sets followed by 1,062 symbols (word aligned)
- F. Repetition of three skip ordered sets followed by 1,061 symbols (word misaligned)

- G. Repetition of four skip ordered sets followed by 1,416 symbols (word aligned)
- H. Repetition of four skip ordered sets followed by 1,415 symbols (word misaligned)

Combinations to be tested for Gen 2 PUT:

For Each SKP Symbol count x in X :

- A. Repeat Sequence 01 with all SKP OSs containing x SKP symbols.
- B. Repeat Sequence 01 with all SKP OSs containing x SKP symbols, with one SKP symbol including a bit error. Before starting the sequences, let $n = -1$. At each sequence repetition, CVS will include the bit error in symbol $(n + 1) \% x$.
- C. Repeat Sequence 02 with all SKP OSs containing x SKP symbols.
- D. Repeat Sequence 02 with all SKP OSs containing x SKP symbols, with one SKP symbol including a bit error. Before starting the sequences, let $n = -1$. At each sequence repetition, CVS will include the bit error in symbol $(n + 1) \% (x * 3)$ (because Sequence 02 contains 3 SKP OSs with x symbols in them).

Received SKP symbol counts in Gen 2 PUT:

- $X = \{4, 8, 12, 16, 20, 24, 28, 32, 36\}$ if PUT includes no captive re-timer
- $X = \{8, 12, 16, 20, 24, 28, 32\}$ if PUT includes one captive re-timer

Sequences of Repetition for Gen 2 PUT:

Sequence 01:

- a. Forty (40) blocks
- b. One SKP OS

Sequence 02:

- a. One hundred and nine (109) blocks
- b. Two SKP OS
- c. One block
- d. One SKP OS

Covered Assertions

(No Physical Layer assertions defined)

Overview of Test Steps

1. Do steps 1 to 4 of the Link Initialization Sequence.
2. The LVS will keep the link active by sending Link Pollings (LUP when it is configured as an Upstream Port or LDN when it is configured as a Downstream Port) for 50ms. Skips will be generated according to Combination A described above.
3. The test passes if the exchanges are successful, no timeout is detected, no recovery is entered, all packets are successfully received, all credits are restored and the link stays in U0 for at least 50ms.
4. Repeat the steps with the next combination listed above.

TD.6.3 Elasticity Buffer Test

This test verifies that the PUT's elasticity buffer supports the required frequency range, from -5,300 to 300ppm.

Covered Assertions

(No Physical Layer assertions defined)

Overview of Test Steps

1. Configure the LVS with an SSC clock of -5300ppm.
2. Bring the link to U0 using the Link Initialization Sequence.
3. The test passes if the Link Initialization Sequence passes.
4. Repeat the above steps with an SSC clock of +300ppm.

TD.6.4 LFPS Frequency Test

This test verifies that the PUT's LFPS detector supports the required frequency range. The periods to be tested are:

- A. SS: tPeriod = 10 MHz, SSP: tPeriod = 12.5 MHz (min)
- B. tPeriod = 50 MHz (max)

Covered Assertions

(No Physical Layer assertions defined)

Overview of Test Steps

1. The LVS and the PUT go through the initial steps of the LTSSM (eSS.Disabled, Rx.Detect) to reach Polling.LFPS.
2. The LVS will start generating a Polling.LFPS signal having durations of tBurst = 1 us and tRepeat = 10 us. The burst period will be set to the first period listed above.
3. The test passes if the PUT moves successfully to Polling.RxEQ according to section 7.5.4.3.2 of the USB 3.1 specification.
4. Repeat the steps with the other period listed above.

TD.6.5 Polling.LFPS Duration Test

This test verifies that the PUT's Polling.LFPS detector supports the required duration range. Here are the durations to be tested:

- A. tBurst = 0.6 us and tRepeat = 6 us
- B. tBurst = 0.6 us and tRepeat = 14 us
- C. tBurst = 1.4 us and tRepeat = 6 us
- D. tBurst = 1.4 us and tRepeat = 14 us

Covered Assertions

(No Physical Layer assertions defined)

Overview of Test Steps

1. The LVS and the PUT go through the initial steps of the LTSSM (eSS.Disabled, Rx.Detect) to reach Polling.LFPS.

2. The LVS will start generating a Polling.LFPS signal having the first duration specified in the list above.
3. The test passes if the PUT moves successfully to Polling.RxEQ according to section 7.5.4.3.2, and if the Polling.LFPS tPeriod, tBurst and tRepeat from the PUT are within the ranges specified in section 6.9.1.
4. Repeat the steps with the other durations listed above.

TD.6.6 SCD Duration Test (Gen 2 Capable Only)

This test verifies that the PUT's Polling.LFPS detector supports the required duration range for SCD signals. Here are the durations to be tested:

- A. tBurst = 0.6 us and '0' tRepeat = 6 us and '1' tRepeat = 11 us
- B. tBurst = 0.6 us and '0' tRepeat = 6 us and '1' tRepeat = 14 us
- C. tBurst = 0.6 us and '0' tRepeat = 9 us and '1' tRepeat = 11 us
- D. tBurst = 0.6 us and '0' tRepeat = 9 us and '1' tRepeat = 14 us
- E. tBurst = 1.4 us and '0' tRepeat = 6 us and '1' tRepeat = 11 us
- F. tBurst = 1.4 us and '0' tRepeat = 6 us and '1' tRepeat = 14 us
- G. tBurst = 1.4 us and '0' tRepeat = 9 us and '1' tRepeat = 11 us
- H. tBurst = 1.4 us and '0' tRepeat = 9 us and '1' tRepeat = 14 us

Covered Assertions

(No Physical Layer assertions defined)

Overview of Test Steps

1. The LVS and the PUT go through the initial steps of the LTSSM (eSS.Disabled, Rx.Detect) to reach Polling.LFPS.
2. The LVS will start generating a Polling.LFPS SCD1 signal having the A parameters specified in the list above.
3. The LVS verifies that:
 - a. The PUT moves successfully to Polling.LFPSPlus according to section 7.5.4.3.2.
 - b. The SCD1 Polling.LFPSs transmitted from the PUT have tPeriod, tBurst, and tRepeat within the ranges specified in spec sections 6.9.1 and 6.9.4.1.
4. The LVS will generate Polling.LFPS SCD2 signals having the A parameters specified in the list above.
5. The test passes if the PUT moves successfully to Polling.PortMatch according to section 7.5.4.4.2, and if the SCD2 Polling.LFPSs transmitted from the PUT have tPeriod, tBurst and tRepeat within the ranges specified in section 6.9.1 and 6.9.4.1.
6. Repeat the steps with the other parameters listed above.

TD.6.7 PWM Duration Test (Gen 2 Capable Only)

This test verifies that the PUT's Polling.LFPS detector supports the required duration range for PWM signals. Here are the durations to be tested:

- A. tPWM = 2 us and tLFPS-0 = 0.5 us and tLFPS-1 = 1.33 us
- B. tPWM = 2 us and tLFPS-0 = 0.5 us and tLFPS-1 = 1.8 us
- C. tPWM = 2 us and tLFPS-0 = 0.8 us and tLFPS-1 = 1.33 us
- D. tPWM = 2 us and tLFPS-0 = 0.8 us and tLFPS-1 = 1.8 us
- E. tPWM = 2.4 us and tLFPS-0 = 0.5 us and tLFPS-1 = 1.33 us

- F. $t_{\text{PWM}} = 2.4 \text{ us}$ and $t_{\text{LFPS-0}} = 0.5 \text{ us}$ and $t_{\text{LFPS-1}} = 1.8 \text{ us}$
- G. $t_{\text{PWM}} = 2.4 \text{ us}$ and $t_{\text{LFPS-0}} = 0.8 \text{ us}$ and $t_{\text{LFPS-1}} = 1.33 \text{ us}$
- H. $t_{\text{PWM}} = 2.4 \text{ us}$ and $t_{\text{LFPS-0}} = 0.8 \text{ us}$ and $t_{\text{LFPS-1}} = 1.8 \text{ us}$

Covered Assertions

(No Physical Layer assertions defined)

Overview of Test Steps

1. The LVS and the PUT go through the initial steps of the LTSSM (eSS.Disabled, Rx.Detect) to reach Polling.PortMatch.
2. The LVS will generate LBPM signals having the A parameters specified in the list above.
3. The LVS verifies that:
 - a. The PUT moves successfully to Polling.PortConfig according to section 7.5.4.5.2.
 - b. The PWM LFPSs transmitted from the PUT have t_{PWM} , $t_{\text{LFPS-0}}$, and $t_{\text{LFPS-1}}$ within the ranges specified in spec sections 6.9.1 and 6.9.5.1.
4. The LVS will generate LBPM signals having the A parameters specified in the list above.
5. The test passes if the PUT moves successfully to Polling.RxEQ according to section 7.5.4.6.2, and if the PWM LFPSs transmitted from the PUT have t_{PWM} , $t_{\text{LFPS-0}}$ and $t_{\text{LFPS-1}}$ within the ranges specified in section 6.9.1 and 6.9.4.1.
6. Repeat the steps with the other parameters listed above.

5.3 Link Layer

TD.7.1 Link Bring-up Test

This test verifies that the Link Verification System (LVS) and the Port under Test (PUT) can reach U0 successfully.

As the test progresses it is divided into four subtests. Ports with Gen 1 capability and not Gen 2 capability must be tested with subtests 1 and 2. Ports with Gen 2 capability must be tested with subtests 3, 4 and 5.

Covered Assertions

Refer to the list of covered assertions for the Link Initialization Sequence

Overview of Test Steps

1. The LVS starts the link process.
 - If the LVS is configured as a Downstream Port, the LVS asserts VBUS. The PUT should move from eSS.Disabled to Rx.Detect.
 - If the LVS is configured as an Upstream Port, the LVS asserts Terminations. The PUT should already be in Rx.Detect.
2. The test fails if the PUT does not transmit Polling.LFPS bursts before $t_{\text{RxDetectQuietTimeout}} + t_{\text{PollingLFPSEstablishedTimeout}}$ expires.

Continue to Required Subtest

Subtest 1 (TD 7.1.1):

1. The LVS waits to receive Polling.LFPS bursts.
2. The LVS transmits four Polling.LFPS bursts.
3. The test fails if any of the following occur:
 - a. If the PUT does not contain a captive re-timer, it does not transmit at least sixteen consecutive Polling.LFPS bursts.
 - b. If the PUT contains a captive re-timer, it does not transmit at least four consecutive Polling.LFPS bursts.
 - c. The PUT does not transmit at least four consecutive Polling.LFPS bursts after receiving one Polling.LFPS bursts.
 - d. The PUT transitions away from Polling.LFPS before the LVS sends at least two consecutive Polling.LFPS bursts.
 - e. The PUT does not transition from Polling.LFPS before `tPollingLFPSTimeout` expires.
4. The test fails if the PUT has transmitted more than 6 LFPS after receiving 1 LFPS and the Number of LFPS tx'd before receiving 1 > 18 – the Number of LFPS tx'd after receiving 1.
5. The LVS transmits 65,536 TSEQ ordered sets.
6. The test fails if any of the following occur:
 - a. The PUT does not transmit TSEQ ordered sets.
 - b. The PUT transmits SKP Ordered Sets, Idle Symbols, or any other Packet, Symbol or Ordered Set during TSEQ transmission or between training ordered sets.
7. The LVS transmits TS1 ordered sets and waits to receive eight consecutive and identical TS1 or TS2 ordered sets from the PUT.
8. The test fails if any of the following occur:
 - a. The PUT does not transmit TS1 ordered sets.
 - b. The PUT transmits TS2s before the LVS sends eight consecutive and identical TS1s or TS2s.
 - c. The PUT interrupts a TS1 ordered set to transmit a SKP ordered set (between TS1 ordered sets is OK).
 - d. The PUT transmits Idle Symbols or any other Packet.
 - e. The PUT continues to transmit TS1 ordered sets after `tPollingActiveTimeout` expires.
9. The LVS transmits TS2 ordered sets and readies to complete the Polling.Configuration handshake.
10. The test fails if any of the following occur:
 - a. The PUT does not transmit at least sixteen consecutive TS2 ordered sets after receiving one TS2 ordered set.
 - b. The PUT sends Idle symbols before the LVS sends at least eight consecutive TS2 ordered sets.
 - c. The PUT interrupts transmission of a TS2 ordered set to transmit a SKP ordered set (between TS2 ordered sets is OK).
 - d. The PUT continues to transmit TS2 ordered sets after `tPollingConfigurationTimeout` expires.
11. The LVS transmits Idle symbols.

12. The test fails if upon entering U0, the PUT does not transmit the Header Sequence Number Advertisement and the Rx Header Buffer Credit Advertisement before their respective timeouts, PENDING_HP_TIMER and CREDIT_HP_TIMER, expire.
13. The LVS and PUT continue the test with the Link Initialization Sequence starting at step two.

Subtest 2 (TD 7.1.2):

1. The LVS transmits Polling.LFPS bursts with an SCD1 signature.
2. The test fails if a PUT that does not contain a captive re-timer does not transmit at least 16 Polling.LFPS bursts.
3. The LVS switches to regular Polling.LFPS bursts after transmitting 4 SCD1 and receiving 16 Polling.LFPS bursts, or after receiving 4 Polling.LFPS and tPollingSCDLFPSTimeout has expired – whichever comes first.
4. The test fails if any of the following occur:
 - a. The PUT does not transmit at least four consecutive Polling.LFPS bursts after receiving one Polling.LFPS burst (Note: The received Polling.LFPS burst may be part of an SCD1 from the LVS, or may be from a regular Polling.LFPS burst after the LVS transitions)
 - b. The PUT transitions away from Polling.LFPS before the LVS sends at least two consecutive Polling.LFPS bursts.
 - c. The PUT does not transition from Polling.LFPS before tPollingLFPSTimeout expires.
5. The test fails if the PUT has transmitted more than 6 LFPS after receiving 1 regular (non-SCD) Polling.LFPS burst and the Number of LFPS tx'd before receiving 1 > 18 – the Number of LFPS tx'd after receiving 1.
6. Continue to Subtest 1 (TD 7.1.1) step 5.

Subtest 3 (TD 7.1.3)

1. The LVS transmits Polling.LFPS bursts.
2. The test fails if any of the following occur:
 - a. The PUT does not switch to SuperSpeed operation after transmitting 4 SCD1 and receiving 16 Polling.LFPS.
 - b. For a PUT with no captive re-timer, the PUT does not transmit 16 regular Polling.LFPS
 - c. The PUT does not transmit at least four consecutive regular Polling.LFPS bursts after receiving one Polling.LFPS burst.
 - d. For a PUT with no captive re-timer, the PUT does not transition to Polling.RxEQ after transmitting 16 regular Polling.LFPS.
 - e. For a PUT with a captive re-timer, the PUT does not transition to Polling.RxEQ after transmitting 4 regular Polling.LFPS on both transmitters and tPollingSCDLFPSTimeout has expired at both receivers.
3. Continue to Subtest 1 (TD 7.1.1) step 5.

Subtest 4 (TD 7.1.4)

1. The LVS transmits Polling.LFPS bursts with an SCD1 signature.
2. The test fails if the PUT does not transmit two SCD1 after one SCD1 or SCD2 is received.
3. The LVS transitions to transmitting Polling.LFPS bursts with an SCD2 signature after transmitting two SCD1 after receiving 1 SCD1 or SCD2 from the PUT
4. The test fails if the PUT does not transmit two SCD2 after one SCD2 is received.
5. The LVS transmits continuous PHY Capability LBPMs to announce its 10Gbps capability.
6. The test fails if the PUT does not continuously transmit its PHY Capability LBPMs.
7. If the LVS has a PHY Capability greater than the PUT, then:
 - a. The LVS adjusts its PHY Capability by transmitting PHY Capability LBPMs that match the PUT.
 - b. The test fails if the PUT does not continuously transmit its PHY Capability LBPMs.
8. The test fails if the PUT does not transmit three consecutive and matched PHY Capability LBPMs after receiving two consecutive and matched PHY Capability LBPMs or PHY Ready LBPMs.
9. The LVS transmits 524,288 TSEQ Ordered Sets, inserting a SYNC Ordered Set every 16,384 Ordered Sets.
10. The test fails if any of the following occur:
 - a. The PUT does not transmit TSEQ Ordered Sets.
 - b. The PUT does not transmit a SYNC Ordered Set for every 16,384 TSEQ Ordered Sets.
 - c. The PUT transmits Idle Symbols, or any other Packet, Symbol or Ordered Set besides SYNC or SKP Ordered Sets, during TSEQ transmission or between TSEQ Ordered Sets.
11. The LVS transmits TS1 Ordered Sets, inserting a SYNC Ordered Set every 32 Ordered Sets, and inserting SKP Ordered Sets periodically when necessary.
12. The LVS waits to receive eight consecutive and identical TS1 or TS2 Ordered Sets from the PUT. Note: SYNC and SKP Ordered Sets do not disqualify consecutive TS1s / TS2s. Symbols 14-15 of the TS1 / TS2 Ordered Sets do not need to be identical.
13. The test fails if any of the following occur:
 - a. The PUT does not transmit TS1 ordered sets.
 - b. The PUT transmits TS2s before the LVS transmits eight consecutive and identical TS1s or TS2s.
 - c. The PUT interrupts a TS1 Ordered Set to transmit a SKP or SYNC Ordered Set (between TS1 ordered sets is OK).
 - d. The PUT transmits Idle Symbols or any other Packet.
 - e. The PUT continues to transmit TS1 Ordered Sets after tPollingActiveTimeout expires.
14. The LVS transmits TS2 Ordered Sets, inserting a SYNC Ordered Set every 32 Ordered Sets, and inserting SKP Ordered Sets periodically when necessary.
15. The test fails if any of the following occur:

- a. The PUT does not transmit at least 16 consecutive TS2 ordered sets after receiving one TS2 ordered set.
 - b. The PUT transmits Idle symbols before the LVS transmits eight consecutive and identical TS2s.
 - c. The PUT interrupts a TS1 Ordered Set to transmit a SKP or SYNC Ordered Set (between TS2 Ordered Sets is OK).
 - d. The PUT continues to transmit TS2 Ordered Sets after tPollingConfigurationTimeout expires.
16. The LVS transmits a single SDS Ordered Set and then data blocks with Idle Symbols.
 17. The test fails if upon entering U0, the PUT does not transmit the Header Sequence Number Advertisement and the Type 1 and Type 2 Rx Header Buffer Credit Advertisements before their respective timeouts, PENDING_HP_TIMER and Type 1 and Type 2 CREDIT_HP_TIMERS, expire.
 18. The LVS and PUT continue the Link Initialization Sequence starting at step two.

Subtest 5 (TD 7.1.5)

1. The LVS waits to receive Polling.LFPS bursts (as components of the SCD1)
2. The LVS transmits four regular Polling.LFPS bursts and transitions to Polling.RxEQ
3. The test fails if any of the following occur:
 - a. The PUT does not switch to SuperSpeed operation and Polling.RxEQ state after tPollingSCDLFPSTimeout deadline and before tPollingSCDLFPSTimeout expires.
 - b. The PUT does not continue to send Polling.LFPS up until tPollingSCDLFPSTimeout.
4. Continue to Subtest 1 (TD 7.01.1) step 5.

TD.7.2 Link Commands Framings Robustness Test

This test verifies that the PUT can tolerate link commands having one symbol error in the LCSTART framing. Here are the combinations to be tested:

- A. ERR SLC SLC EPF
- B. SLC ERR SLC EPF
- C. SLC SLC ERR EPF
- D. SLC SLC SLC ERR

The Port Configuration transaction will be used for this purpose.

Covered Assertions

7.3.4#1,2

Overview of Test Steps

1. Perform the Link Initialization Sequence, but transmit all LCRD_X or LCRD1_X with an error in the first LCSTART symbol.
2. The test passes if the Link Initialization Sequence passes.
3. Repeat the above steps with an error in the second, third, and fourth LCSTART symbols as shown above.

TD.7.3 Link Commands CRC-5 Robustness Test

This test verifies that a Gen 1 PUT will ignore link commands with a CRC-5 error, even if only one of the Link Command Words has a CRC-5 error. The test verifies that a Gen 2 device will accept link commands with one CRC-5 error and ignore link commands with both LCWs containing a CRC-5 error. The Port Configuration transaction will be used for this purpose.

The tested CRC-5 error robustness conditions are:

- A. Incorrect CRC-5 in first Link Command Word
- B. Incorrect CRC-5 in second Link Command Word
- C. Both Link Command Words have an incorrect CRC-5.

Covered Assertions

7.3.4#2

Overview of Test Steps

1. Perform the Link Initialization Sequence but transmit all LCRD_X or LCRD1_X with condition A above.
2. The test passes if:
 - a. A SuperSpeed PUT enters recovery when CREDIT_HP_TIMER expires.
 - b. A SuperSpeedPlus PUT stays in U0 for 50ms.
3. Repeat the above steps for condition B listed above.
4. Perform the Link Initialization Sequence but transmit all LCRD_X or LCRD1_X with condition C above.
5. The test passes if the PUT enters recovery when the CREDIT_HP_TIMER or the Type 1 CREDIT_HP_TIMER expires.

TD.7.4 Invalid Link Commands Test

This test verifies that the PUT will ignore Link Commands with link command information in the first LCW not the same as link command information in the second LCW, and both pass the CRC5 check.

Covered Assertions

7.3.4#2

Overview of Test Steps

1. Do steps 1 to 5 of the Link Initialization Sequence.
2. The LVS sends a link command with LGO_U1 in the first LCW and LGO_U2 in the second LCW, with good CRC-5 calculations on both.
3. The test fails if the PUT responds with an LAU or LXU.
4. The LVS will keep the link active by sending Link Pollings (LUP when it is configured as an Upstream Port or LDN when it is configured as a Downstream Port) for 50ms.

5. The test passes if the link command is ignored, all exchanges are successful, no timeout is detected, no recovery is entered, all packets are successfully received by the PUT, all credits are restored and the link stays in U0 for at least 50ms.

TD.7.5 Header Packet Framing Robustness Test

This test verifies that the PUT does not invalidate header packets having one symbol error in the HPSTART framing. The combinations to be tested:

- A. **ERR** SHP SHP EPF
- B. SHP **ERR** SHP EPF
- C. SHP SHP **ERR** EPF
- D. SHP SHP SHP **ERR**

The Port Configuration transaction will be used for this purpose.

Covered Assertions

7.2.4.1.4#1

Overview of Test Steps

1. Perform the Link Initialization Sequence, but transmit all Header Packets with an error in the first HPSTART symbol.
2. The test passes if the Link Initialization Sequence passes.
3. Repeat the above steps with an error in the second, third, and fourth HPSTART symbols, as shown above.

TD.7.6 Data Payload Packet Framing Robustness Test

This test verifies that the PUT does not invalidate data payload packets having a single character framing error in DPPSTART and DPPEND. The combinations to be tested:

- A. **ERR** SDP SDP EPF
- B. SDP **ERR** SDP EPF
- C. SDP SDP **ERR** EPF
- D. SDP SDP SDP **ERR**
- E. **ERR** END END EPF
- F. END **ERR** END EPF
- G. END END **ERR** EPF
- H. END END END **ERR**

When the LVS is a Downstream Port, it will place framing errors on Setup DP Packets.

When the LVS is an Upstream Port, it will reply to the GetDeviceDescriptor request with a DPP containing framing errors.

If the DUT is a Gen 1 device, the LVS also verifies that the PUT can handle Gen2 Transaction Packets in which several Gen1 Reserved bits are in use. The verification includes various configurations in the TPS and TT fields of the Gen2 Transaction Packet.

Covered Assertions

7.2.4.1.6#1,2

7.3.4.1#3

Overview of Test Steps

1. Perform the Link Initialization Sequence.
2. At this stage the Downstream Port is expected to issue a GetDeviceDescriptor request.
 - If the LVS is configured as an Upstream Port:
 - a. The LVS prompts the test operator to have the PUT send a GetDeviceDescriptor request through USB30CV and then press “OK”.
 - b. The test fails if no GetDeviceDescriptor request is received and the test operator has pressed “OK”.
 - c. When the LVS receives a GetDeviceDescriptor request, it closes the prompt. The LVS will respond to the request with a DPP containing the Device Descriptor data which includes the first framing error listed above.
 - If the LVS is configured as a Downstream Port, it will issue a GetDeviceDescriptor request, but will send the SETUP DP with the first framing error listed above.
3. The LVS will keep the link active by sending Link Pollings (LUP when it is configured as an Upstream Port or LDN when it is configured as a Downstream Port) for 50ms.
4. The test fails if the data exchange fails on the protocol level.
5. The test passes if the exchanges are successful, no timeout is detected, no recovery is entered, all packets are successfully received by the PUT, all credits are restored and the link stays in U0 for at least 50ms.
6. Repeat for each condition listed above.

TD.7.7 RX Header Packet Retransmission Test

This test verifies that the PUT will send an LBAD if an invalid header packet is received, and that the retransmission will be correctly handled.

The tested conditions invalidating a header packet are:

- A. Incorrect CRC-16
- B. Incorrect CRC-5
- C. K28.2 SDP symbol in HP data
- D. K28.3 EDB symbol in HP data
- E. K28.4 SUB symbol in HP data
- F. K28.6 Reserved K-symbol in HP data
- G. K27.7 SHP symbol in HP data
- H. K29.7 END symbol in HP data
- I. K30.7 SLC symbol in HP data
- J. K23.7 EPF symbol in HP data

Conditions C – J are tested for Gen 1 PUTs only. Each of the conditions C – J in the following positions, one case at a time:

1. Position 2: SHP SHP SHP EPF DX.X KX.X DX.X DX.X
2. Position 5: SHP SHP SHP EPF DX.X DX.X DX.X DX.X KX.X

Covered Assertions

7.2.4.1.4#3, 4

Overview of Test Steps

1. Do steps 1 to 3 of the Link Initialization Sequence.
2. The LVS and the PUT will exchange Port Configuration transactions, but the first packet sent by the LVS will be invalid.
 - If the LVS is configured as a Downstream Port:
 - a. The LVS waits for the PUT's Port Capability LMP.
 - b. LVS verifies that the Port Capability LMP is valid.
 - c. LVS transmits its Port Capability LMP with the first invalid condition listed above.
 - d. LVS verifies that the PUT replies with an LBAD.
 - e. LVS transmits a LRTY and then retransmits the packet.
 - f. LVS transmits the Port Configuration LMP.
 - g. LVS waits for the PUT's Port Configuration Response LMP.
 - h. LVS verifies the PUT's Port Configuration Response LMP.
 - If the LVS is configured as an Upstream Port:
 - a. LVS waits for the PUT's Port Capability LMP.
 - b. LVS verifies that the Port Capability LMP is valid.
 - c. LVS transmits its Port Capability LMP with the first invalid condition listed above.
 - d. LVS verifies the PUT replies with an LBAD.
 - e. LVS transmits a LRTY and then retransmits the packet.
 - f. LVS waits for the PUT's Port Configuration LMP.
 - g. LVS verifies the PUT's Port Configuration LMP.
 - h. LVS transmits its Port Configuration Response LMP.
3. The LVS will keep the link active by sending Link Pollings (LUP when the LVS is configured as Upstream Port, or LDN when the LVS is configured as a Downstream Port) for 50ms.
4. The test passes if the exchanges are successful, no timeout is detected, no recovery is entered, the PUT responds to the invalid packets with an LBAD, all other packets are successfully received, all credits are restored and the link stays in U0 for at least 50ms.
5. Repeat the above steps for each of the invalid conditions listed above.
6. For a Gen 1 device, skip the remaining steps.
7. The LVS and PUT complete the Link Initialization Sequence.
 - If the LVS is configured as a Downstream Port:
 - a. LVS issues a GetDeviceDescriptor() request for the PUT, but transmits the SETUP packet with Condition A listed above.
 - If the LVS is configured as an Upstream Port:
 - a. The LVS prompts the test operator to have the PUT send a GetDeviceDescriptor request through USB30CV and then press "OK".

- b. The test fails if no GetDeviceDescriptor request is received and the test operator has pressed “OK”.
 - c. LVS will transmit the IN DP with Condition A listed above.
8. The LVs will keep the link active by sending Link Pollings (LUP when it is configured as an Upstream Port, LDN when it is configured as a Downstream Port).
 9. The test passes if the exchanges are successful, no timeout is detected, no recovery is entered, the PUT responds to the invalid packets with an LBAD, all other packets are successfully received, all credits are restored and the link stays in U0 for at least 50ms.
 10. Repeat steps 7 through 9 for Condition B listed above.

TD.7.8 TX Header Packet Retransmission Test

This test verifies that the PUT will correctly retransmit a header packet on receipt of an LBAD.

Covered Assertions

7.2.4.1.3#1, 2

Overview of Test Steps

1. Do steps 1 to 3 of the Link Initialization Sequence.
2. The LVS and the PUT will exchange the Port Configuration transaction, but in this case the LVS will respond to the first packet sent by the PUT with an LBAD.
 - If the LVS is configured as a Downstream Port:
 - a. LVS waits for the PUT’s Port Capability LMP.
 - b. LVS verifies that the Port Capability LMP is valid.
 - c. LVS responds to the PUT with an LBAD.
 - d. LVS waits for the PUT to transmit an LRTY.
 - e. LVS waits for the retransmitted packet.
 - f. LVS verifies that the retransmitted packet is the same as the first packet sent by the device.
 - g. LVS transmits its Port Capability LMP and Port Configuration LMP.
 - h. LVS waits for the PUT Port Configuration Response LMP.
 - i. LVS verifies the PUT’s Port Configuration Response LMP.
 - If the LVS is configured as an Upstream Port:
 - a. LVS waits for the PUT’s Port Capability LMP.
 - b. LVS verifies that the Port Capability LMP is valid.
 - c. LVS transmits its Port Capability LMP.
 - d. LVS responds to the PUT with an LBAD.
 - e. LVS waits for the PUT to transmit an LRTY.
 - f. LVS waits for the retransmitted packet.
 - g. LVS verifies that the retransmitted packet is the same as the first packet sent by the device.
 - h. LVS waits for the PUT’s Port Configuration LMP.

- i. LVS verifies that the Port Configuration LMP is valid.
 - j. LVS transmits its Port Configuration Response LMP.
3. The LVS will keep the link active by sending Link Pollings (LUP when it was configured as an Upstream Port, LDN when it was configured as a Downstream Port) for 50ms.
 4. The test passes if the exchanges are successful, no timeout is detected, no recovery is entered, the packet that the LVS responded to with an LBAD is retransmitted correctly, all other packets are received successfully, all credits are restored and the link stays in U0 for at least 50ms.

TD.7.9 PENDING_HP_TIMER Deadline Test

This test verifies that:

- 1) The PUT will accept an LGOOD_N sent at the maximum link delay budget before PENDING_HP_TIMER deadline. The Port Configuration transaction will be used for this purpose.
- 2) The PUT adheres to tLinkTurnaround as defined in Ch 7 and Appendix E.

Covered Assertions

7.2.4.1.10#2

Overview of Test Steps

1. Perform the Link Initialization Sequence, but transmit LGOOD_N responses for Port Capability LMP 200ns prior to the PENDING_HP_TIMER deadline.
2. The LVS verifies that for each LGOOD_n received from the PUT, the first symbol of the LGOOD_n is received within tLinkTurnaround of the last symbol of the Header Packet that is acknowledged by the LGOOD_n.
3. The LVS will keep the link active by sending Link Pollings (LUP when it is configured as an Upstream Port or LDN when it is configured as a Downstream Port) for 50ms.
4. The test passes if the exchanges are successful, no timeout is detected, no recovery is entered, all packets are successfully received, all credits are restored and the link stays in U0 for at least 50ms.

TD.7.10 CREDIT_HP_TIMER Deadline Test

This test verifies that the PUT will accept an LCRD_X, LCRD1_X or LCRD2_X sent at the CREDIT_HP_TIMER deadline. The Port Configuration transaction will be used for this purpose.

Covered Assertions

7.2.4.1.10#7

Overview of Test Steps

1. Perform the Link Initialization Sequence but transmit all LCRD_X or LCRD1_X responses tLinkTurnAround prior to the CREDIT_HP_TIMER or type 1 CREDIT_HP_TIMER deadline.
2. The LVS will keep the link active by sending Link Pollings (LUP when it is configured as an Upstream Port or LDN when it is configured as a Downstream Port) for 50ms.
3. For a Gen 1 PUT continue to step 6.
4. For a Gen 2 PUT:

- If the LVS is configured as a Downstream Port:
 - a. LVS issues a GetDeviceDescriptor() request for the PUT.
 - b. LVS transmits all LCRD2_X responses 200ns prior to the CREDIT_HP_TIMER deadline.
 - If the LVS is configured as an Upstream Port:
 - a. The LVS prompts the test operator to have the PUT send a GetDeviceDescriptor request through USB30CV and then press “OK”.
 - b. The test fails if no GetDeviceDescriptor request is received and the test operator has pressed “OK”.
 - c. LVS transmits all LCRD2_X responses associated with the GetDeviceDescriptor request 200ns prior to the type 2 CREDIT_HP_TIMER deadline.
5. The LVS will keep the link active by sending Link Pollings (LUP when it is configured as an Upstream Port or LDN when it is configured as a Downstream Port) for 50ms.
 6. The test passes if the exchanges are successful, no timeout is detected, no recovery is entered, all packets are successfully received, all credits are restored and the link stays in U0 for at least 50ms.

TD.7.11 PENDING_HP_TIMER Timeout Test

This test verifies that the PUT will go to recovery when the PENDING_HP_TIMER expires.

Covered Assertions

7.2.4.1.10#1

Overview of Test Steps

1. Do steps 1 to 3 of the Link Initialization Sequence.
2. The LVS and the PUT will exchange the Port Configuration transaction, but the LVS will respond (with an LGOOD) to the first LMP packet sent by the PUT after expiration of the PENDING_HP_TIMER.
 - If the LVS is configured as a Downstream Port:
 - a. LVS waits for the PUT’s Port Capability LMP.
 - b. LVS verifies that the Port Capability LMP is valid.
 - c. LVS will not respond to the PUT with an LGOOD.
 - d. LVS transmits its Port Capability LMP and Port Configuration LMP.
 - If the LVS is configured as an Upstream Port:
 - a. LVS waits for the PUT to transmit its Port Capability LMP.
 - b. LVS verifies that the Port Capability LMP is valid.
 - c. LVS transmits its PUT Port Capability LMP.
 - d. LVS will not respond to the PUT with an LGOOD.
3. The LVS will keep the link active by sending Link Pollings (LUP when it is configured as an Upstream Port, LDN when it is configured as a Downstream Port).
4. The test passes if the PUT goes to recovery after the PENDING_HP_TIMER deadline and before the PENDING_HP_TIMER expires.

TD.7.12 CREDIT_HP_TIMER Timeout Test

This test verifies that the PUT will go to recovery when the CREDIT_HP_TIMER expires.

Covered Assertions

7.2.4.1.10#6

Overview of Test Steps

1. Do steps 1 to 4 of the Link Initialization Sequence with the exception that the LVS will not send any LCRD_X or LCRD1_X.
2. The LVS will keep the link active by sending Link Pollings (LUP when it is configured as an Upstream Port, LDN when it is configured as a Downstream Port).
3. The test passes if the PUT goes to recovery after the CREDIT_HP_TIMER deadline and before the CREDIT_HP_TIMER expires. For a Gen 2 PUT, this refers to the Type 1 CREDIT_HP_TIMER.
4. For a Gen 1 device, skip the remaining steps.
5. The LVS and PUT complete the Link Initialization Sequence.
 - If the LVS is configured as a Downstream Port:
 - a. LVS issues a GetDeviceDescriptor() request for the PUT.
 - b. LVS will not send any LCRD2_X.
 - If the LVS is configured as an Upstream Port:
 - a. The LVS prompts the test operator to have the PUT send a GetDeviceDescriptor request through USB30CV and then press “OK”.
 - b. The test fails if no GetDeviceDescriptor request is received and the test operator has pressed “OK”.
 - c. LVS will not send any LCRD2_X.
6. The LVS will keep the link active by sending Link Pollings (LUP when it is configured as an Upstream Port, LDN when it is configured as a Downstream Port).
7. The test passes if the PUT goes to recovery after the type 2 CREDIT_HP_TIMER deadline and before the type 2 CREDIT_HP_TIMER expires.

TD.7.13 Wrong Header Sequence Test

This test verifies that the PUT will go to recovery when it receives a wrong header sequence.

Covered Assertions

7.3.5#1

Overview of Test Steps

1. Do steps 1 to 4 of the Link Initialization Sequence, with the exception that the LVS will send two LMP packets with Header Sequence Numbers that are not sequential.
2. The test passes if the PUT goes to recovery within tRecoveryTransition after reception of the LMP packet with a Header Sequence Number that is not sequential.

TD.7.14 Wrong LGOOD_N Sequence Test

This test verifies that the PUT will go to recovery when it receives an incorrect LGOOD_N sequence.

Covered Assertions

7.3.4#4

Overview of Test Steps

1. Do steps 1 to 4 of the Link Initialization Sequence, with the exception that the LVS will send an LGOOD_0 for the first LMP packet as expected, but will send an LGOOD_n with $n \neq 1$ for the second LMP packet.
2. The test passes if the PUT goes to recovery within tRecoveryTransition after reception of the incorrect LGOOD_n.

TD.7.15 Wrong LCRD_X Sequence Test

This test verifies that the PUT will go to recovery when it receives an incorrect LCRD_X or LCRD1_X sequence.

Covered Assertions

7.3.4#5

Overview of Test Steps

1. Do steps 1 to 4 of the Link Initialization Sequence, with the exception that the LVS will send an LCRD_A or LCRD1_A for the first LMP packet as expected, but will send an LCRD_X or LCRD1_X with $X \neq B$ for the second LMP packet.
2. The test passes if the PUT goes to recovery within tRecoveryTransition after reception of the incorrect LCRD_X or LCRD1_X.
3. For a Gen 1 device, skip the remaining steps.
4. The LVS and PUT complete the Link Initialization Sequence.
 - If the LVS is configured as a Downstream Port:
 - a. LVS issues a GetDeviceDescriptor() request for the PUT.
 - b. LVS transmits an LCRD2_A in response to the IN DP.
 - c. LVS issues a GetDeviceDescriptor() request for the PUT.
 - d. LVS transmits an LCRD2_X with $X \neq B$ for the IN DP.
 - If the LVS is configured as an Upstream Port:
 - a. The LVS prompts the test operator to have the PUT send two GetDeviceDescriptor requests through USB30CV and then press “OK”.
 - b. The test fails if two GetDeviceDescriptor requests have not been received and the test operator has pressed “OK”.
 - c. LVS transmits an LCRD2_A in response to the first SETUP DP.
 - d. LVS transmits an LCRD2_X with $X \neq B$ for the second SETUP DP.

5. The test passes if the PUT goes to Recovery within tRecoveryTransition after reception of the incorrect LCRD2_X.

TD.7.16 Link Command Missing Test (Upstream Port Only)

This test verifies that the PUT will go to Recovery if no Link Commands are received for more than tU0RecoveryTimeout.

Please note that the downstream LVS port shall disable transmission of ITPs.

Covered Assertions

- 7.3.4#7, 8
- 7.5.6.1#3
- 7.5.6.2#6

Overview of Test Steps

1. Do steps 1 to 4 of the Link Initialization Sequence.
2. The LVS will not send LDNs or any other link commands.
3. The test fails if the PUT goes to Recovery before the tU0RecoveryTimeout deadline, or if it does not go to Recovery after tU0RecoveryTimeout expires.

TD.7.17 tPortConfiguration Time Timeout Test

This test verifies that a downstream PUT will go to SS.Inactive if tPortConfiguration expires, and an upstream PUT will go to SS.Disabled if tPortConfiguration expires.

Covered Assertions

- 7.5.6.2#10,11
- 8.4.5#1,3
- 8.4.6#2

Overview of Test Steps

Note: For a PUT with captive re-timer, once LVS enters U0, LVS times out to Recovery after tPortConfiguration max + tU0RecoveryActive max.

1. Do steps 1 to 3 of the Link Initialization Sequence.
2. The LVS does not transmit both the Port Capability LMP and Port Configuration LMP.
3. The test fails if any of the following occur:
 - a. The PUT transitions to eSS.Inactive (downstream PUT) or eSS.Disabled (upstream PUT) before tPortConfiguration deadline.

- b. The PUT does not transition to eSS.Inactive (downstream PUT) or eSS.Disabled (upstream PUT) before tPortConfiguration expires.
 - i. For a PUT with a captive re-timer, the PUT does not transition to eSS.Inactive (downstream PUT) or eSS.Disabled (upstream PUT) before tU0RecoveryTimeout + tRecoveryActiveTimeout expires.
 - c. An Upstream Facing PUT sends any other packets or LFPS signals.
 - d. A Downstream Facing PUT sends any other packets or LFPS signals besides a Warm Reset.
 - e. For a PUT without a captive re-timer, the PUT enters recovery.
4. Do steps 1 to 3 of the Link Initialization Sequence.
5. The LVS waits for the Port Capability LMP from the PUT.
6. LVS verifies that the Port Capability LMP is valid.
7. The LVS transmits the Port Capability LMP, but does not transmit the Port Configuration LMP (downstream LVS port) or Port Configuration Response LMP (upstream LVS port).
8. The test fails if any of the following occur:
 - a. The PUT does not transmit the Port Capability LMP.
 - b. The PUT transitions to eSS.Inactive (downstream PUT) or eSS.Disabled (upstream PUT) before tPortConfiguration deadline.
 - c. The PUT does not transition to eSS.Inactive (downstream PUT) or eSS.Disabled (upstream PUT) before tPortConfiguration expires.
 - i. For a PUT with a captive re-timer, the PUT does not transition to eSS.Inactive (downstream PUT) or eSS.Disabled (upstream PUT) before tU0RecoveryTimeout + tRecoveryActiveTimeout expires.
 - d. An Upstream Facing PUT sends any other packets or LFPS signals.
 - e. A Downstream Facing PUT sends any other packets or LFPS signals besides a Warm Reset.
 - f. For a PUT without a captive re-timer, the PUT enters recovery.
9. Do steps 1 to 3 of the Link Initialization Sequence
10. The LVS does not transmit the Port Capability LMP, but does send the Port Configuration LMP (downstream LVS port) or Port Configuration Response LMP if a Port Configuration LMP is received (upstream LVS port).
11. The test fails if any of the following occur:
 - a. The PUT does not transmit the Port Capability LMP.
 - b. The PUT transitions to eSS.Inactive (downstream PUT) or eSS.Disabled (upstream PUT) before tPortConfiguration deadline.
 - c. The PUT does not transition to eSS.Inactive (downstream PUT) or eSS.Disabled (upstream PUT) before tPortConfiguration expires.
 - i. For a PUT with a captive re-timer, the PUT does not transition to eSS.Inactive (downstream PUT) or eSS.Disabled (upstream PUT) before tU0RecoveryTimeout + tRecoveryActiveTimeout expires.
 - d. An Upstream Facing PUT sends any other packets or LFPS signals.
 - e. A Downstream Facing PUT sends any other packets or LFPS signals besides a Warm Reset.
 - f. For a PUT without a captive re-timer, the PUT enters recovery.

TD.7.18 Low Power initiation for U1 test (Downstream Port Only)

This test verifies that the PUT initiates U1 state.

Covered Assertions

7.2.4.2.2#1

7.2.4.2.3#1,3,4,5,7,8

7.2.4.2.7#2,3

7.5.7.1#2

7.5.7.2#6

Overview of Test Steps

1. Do steps 1 to 4 of the Link Initialization Sequence.
2. The LVS application prompts the test operator to enable and configure the U1 and U2 inactivity timers through USB30CV. CV will set the U1 Timeout field to 7Fh and the U2 Timeout field to 00h.
3. The LVS waits to receive an LGO_U1 from the PUT. The LVS transmits an LXU, when it receives the LGO_U1.
4. The test fails if the PUT sends an LPMA, or if recovery is entered.
5. The LVS waits to receive an LGO_U1 from the PUT again.
6. The LVS transmits an LAU when it receives the LGO_U1.
7. The test fails if any of the following conditions occur:
 - a. The PUT does not transmit an LPMA before PM_ENTRY_TIMER deadline
 - b. The PUT enters recovery
 - c. The PUT does not transition to U1
8. The LVS transmits the U1 Exit LFPS to transition to U0 and waits to receive U1 Exit LFPS to complete the U1 Exit LFPS handshake.
9. The test fails if the LFPS handshake does not conform to the following specifications from section 6.9.2:
 - a. Between 300ns – 2us elapses between the start of the LVS U1 Exit LFPS and the start of the PUT U1 Exit LFPS.
 - b. The PUT U1 Exit LFPS duration is within 0.9us – 1.2us.
 - c. The PUT enters U0 before Ux_EXIT_TIMER deadline.
 - d. The PUT enters Recovery before tNoLFPSResponseTimeout deadline after the start of its U1 exit LFPS.
10. The test passes if all packets are successful, recovery is entered once, no extra packets or LFPS signals are received, and the PUT returns to U0.
11. After the LVS completes this test case, clear the U1/U2 registers through the CV prompt.

TD.7.19 Low Power initiation for U2 test (Downstream Port Only)

This test verifies that the PUT initiates U2 state.

Covered Assertions

- 7.2.4.2.2#1,
- 7.2.4.2.3#1,3,4,5,7,8
- 7.2.4.2.7#2,3
- 7.5.8.1#2
- 7.5.8.2#5

Overview of Test Steps

1. Do steps 1 to 4 of the Link Initialization Sequence.

The LVS application prompts the test operator to enable and configure the U1 and U2 inactivity timers through USB30CV. CV will set the U1 Timeout field to 00h and the U2 Timeout field to 7Fh.
2. The LVS waits to receive an LGO_U2 from the PUT.
3. The LVS transmits an LXU when it receives the LGO_U2.
4. The test fails if the PUT sends an LPMA, or if recovery is entered.
5. The LVS waits to receive an LGO_U2 from the PUT again.
6. The LVS transmits an LAU when it receives the LGO_U2.
7. The test fails if any of the following occur:
 - a. The PUT does not transmit an LPMA before PM_ENTRY_TIMER deadline.
 - b. The PUT enters recovery
 - c. The PUT does transition to U2.
8. The test fails if the PUT does not transition to U2.
9. The LVS transmits the U2 Exit LFPS to transition to U0 and waits to receive U2 Exit LFPS to complete the U2 Exit LFPS handshake.
10. The test fails if the LFPS handshake does not conform to the following specifications from section 6.9.2:
 - a. Between 300ns – 2ms elapses between the start of the LVS U2 Exit LFPS and the start of the PUT U2 Exit LFPS.
 - b. The PUT U2 Exit LFPS duration is within 80us – 2ms.
 - c. The PUT enters U0 before Ux_EXIT_TIMER deadline.
 - d. The PUT enters Recovery before tNoLFPSResponseTimeout deadline after the start of its U2 exit LFPS.
11. The test passes if all packets are successful, recovery is entered once, no extra packets or LFPS signals are received, and the PUT returns to U0.
12. After the LVS completes this test case, clear the U1/U2 registers through the CV prompt.

TD.7.20 PM_LC_TIMER Deadline Test (Downstream Port Only)

This test verifies that the PUT accepts an LGO_U1 sent at the PM_LC_TIMER deadline.

Covered Assertions

- 7.2.4.2.1#1, 2

Overview of Test Steps

1. Do steps 1 to 4 of the Link Initialization Sequence.
2. The LVS application prompts the test operator to enable and configure the U1 and U2 inactivity timers through USB30CV. CV will set the U1 Timeout field to 7Fh and the U2 Timeout field to 00h.
3. The LVS waits to receive an LGO_U1 from the PUT.
4. The LVS transmits an LAU tLinkTurnAround before the PM_LC_TIMER deadline.
5. The test fails if the PUT does not transmit an LPMA after receiving the LAU.
6. After the LVS completes this test case, clear the U1/U2 registers through the CV prompt.

TD.7.21 PM_LC_TIMER Timeout Test (Downstream Port Only)

This test verifies that the PUT transitions to Recovery when the PM_LC_TIMER expires.

Covered Assertions

- 7.2.4.2.1#1
- 7.2.4.2.3#6
- 7.3.4#6

Overview of Test Steps

1. Do steps 1 to 3 of TD.7.18.
2. The LVS does not transmit LAU when it receives the LGO_U1.
3. The test fails if the PUT does not transition to Recovery when the PM_LC_TIMER expires.
4. After the LVS completes this test case, clear the U1/U2 registers through the CV prompt.

TD.7.22 PM_ENTRY_TIMER Timeout Test (Upstream Port Only)

This test verifies that the PUT transitions to a low power state when the PM_ENTRY_TIMER expires.

Covered Assertions

- 7.2.4.2.1#37.2.4.2.3#8,10,12

Overview of Test Steps

1. Do steps 1 to 4 of TD.7.23.
2. The LVS does not transmit LPMA when it receives LAU.
3. The test fails if the PUT does not transition to U1 when the PM_ENTRY_TIMER expires, the PUT does not transmit LAU, or if the PUT sends any packet or LFPS.

TD.7.23 Accepted Power Management Transaction for U1 Test (Upstream Port Only)

This test verifies that the PUT transitions to U1 if it receives LGO_U1.

Covered Assertions

7.2.4.1.1#7,9
 7.2.4.2.1#4
 7.2.4.2.2#2,3
 7.2.4.2.3#2,8,9
 7.2.4.2.7#2,3
 7.5.5.1#2
 7.5.5.2#2
 7.5.7.1#2
 7.5.7.2#2
 8.4.2#1

Overview of Test Steps

1. Do steps 1 to 4 of the Link Initialization Sequence.
2. The LVS transmits the Set Link Function LMP with the Force_LinkPM_Accept bit asserted.
3. The LVS transmits an LGO_U1 and waits to receive an LAU from the PUT.
4. The test fails if the PUT does not transmit an LAU before PM_LC_TIMER deadline, or recovery is entered.
5. The LVS transmits an LPMA and then transition to U1.
6. The test fails if the PUT does not transition to U1 when the PM_ENTRY_TIMER expires, if recovery is entered, or if the PUT sends any packet.
7. The LVS transmits a U1 Exit LFPS to transition to U0 and waits to receive U1 Exit LFPS to complete the U1 Exit LFPS handshake.
8. The test fails if the LFPS handshake does not conform to the following specifications from section 6.9.2:
 - a. Between 300ns – 2us elapses between the start of the LVS U1 Exit LFPS and the start of the PUT U1 Exit LFPS.
 - b. The PUT U1 Exit LFPS duration is within 0.9us – 1.2us.
 - c. The PUT enters Recovery before tNoLFPSResponseTimeout deadline after the start of its U1 exit LFPS.
 - d. The PUT enters U0 before Ux_EXIT_TIMER deadline.
9. The test passes if all packets are successful, recovery is entered once, no extra packets or LFPS signals are received, and the PUT returns to U0.

TD.7.24 Accepted Power Management Transaction for U2 Test (Upstream Port Only)

This test verifies that the PUT transitions to U2 if it receives an LGO_U2.

Covered Assertions

7.2.4.1.1#7,9
 7.2.4.2.1#4
 7.2.4.2.2#2,3
 7.2.4.2.3#2,8,9

7.2.4.2.7#2, 3

7.5.8.1#2

7.5.8.2#5

8.4.2#1

Overview of Test Steps

1. Do steps 1 to 4 of the Link Initialization Sequence.
2. The LVS transmits the Set Link Function LMP with the Force_LinkPM_Accept bit asserted.
3. The LVS transmits an LGO_U2 and waits to receive an LAU from the PUT.
4. The test fails if the PUT does not transmit an LAU before PM_LC_TIMER deadline, or if recovery is entered.
5. The LVS transmits an LPMA and then transitions to U2.
6. The test fails if the PUT does not transition to U2 when the PM_ENTRY_TIMER expires, recovery is entered, or if the PUT sends any packet.
7. The LVS transmits the U2 Exit LFPS to transition to U0 and waits to receive U2 Exit LFPS to complete the U2 Exit LFPS handshake.
8. The test fails if the LFPS handshake does not conform to the following specifications from section 6.9.2:
 - a. Between 300ns – 2ms elapses between the start of the LVS U2 Exit LFPS and the start of the PUT U2 Exit LFPS.
 - b. The PUT U2 Exit LFPS duration is within 80us – 2ms.
 - c. The PUT enters Recovery before tNoLFPSResponseTimeout deadline after the start of its U2 exit LFPS.
 - d. The PUT enters U0 before Ux_EXIT_TIMER deadline
9. The test passes if all packets are successful, recovery is entered once, no extra packets or LFPS signals are received, and the PUT enters Recovery.

TD.7.25 Accepted Power Management Transaction for U3 Test (Upstream Port Only)

This test verifies that the PUT transitions to U3 if it receives an LGO_U3.

Covered Assertions

7.2.4.1.1#7,97.2.4.2.1#4

7.2.4.2.4#2,3,7

7.2.4.2.7#2,3

7.5.9.1#3

7.5.9.2#5

Overview of Test Steps

1. Do steps 1 to 4 of the Link Initialization Sequence.
2. The LVS transmits an LGO_U3 and waits to receive an LAU from PUT.
3. The test fails if the PUT does not transmit an LAU before PM_LC_TIMER deadline, or if recovery is entered..

4. The LVS transmits an LPMA and then transitions to U3.
5. The test fails if the PUT does not transition to U3 when the PM_ENTRY_TIMER expires, if recovery is entered, or if the PUT sends any packet.
6. The LVS transmits the U3 Exit LFPS to transition to U0 and waits to receive U3 Exit LFPS to complete the U3 Exit LFPS handshake.
7. The test fails if the LFPS handshake does not conform to the following specifications from section 6.9.2:
 - a. Between 300ns – 10ms elapses between the start of the LVS U3 Exit LFPS and the start of the PUT U3 Exit LFPS.
 - b. The PUT U3 exit LFPS duration is within 80us – 10ms.
 - c. The PUT enters Recovery before tNoLFPSResponseTimeout deadline after the start of its U3 exit LFPS.
8. The test passes if all packets are successful, recovery is entered once, no extra packets or LFPS signals are received, and the PUT enters Recovery.

TD.7.26 Transition to U0 from Recovery Test

This test verifies that the PUT transitions to U0 when it is in Recovery.

Covered Assertions

7.2.4.1.1#3,4,7,9

7.3.6#17.5.10.3.1#1

7.5.10.3.2#1

7.5.10.4.2#1

7.5.10.5.1#1

7.5.10.5.2#1

Overview of Test Steps

1. Both the LVS and the PUT go through the initial steps of the LTSSM to reach U0.
2. The LVS does not transmit the Header Sequence Advertisement and the Rx Header Buffer Credit Advertisement or Type 1 and Type 2 Rx Header Buffer Credit Advertisements. The PUT will then transition to Recovery because the PENDING_HP_TIMER will time out.
3. The test fails if the PUT transitions to Recovery before PENDING_HP_TIMER deadline or it does not transition to Recovery when the PENDING_HP_TIMER expires.
4. The test fails if any of the following occur:
 - a. The PUT does not transmit TS1 ordered sets.
 - b. The PUT transmits TS2s before the LVS sends eight consecutive and identical TS1s or TS2s.
 - c. The PUT interrupts a TS1 ordered set to transmit a SKP or SYNC (for Gen 2 only) Ordered Set (between TS1 ordered sets is OK).
 - d. The PUT transmits Idle Symbols or any other Packet.
 - e. The PUT continues to transmit TS1 ordered sets after tRecoveryActiveTimeout expires.
5. The LVS transmits TS2 ordered sets and readies to complete the Recovery.Configuration handshake.
6. The test fails if any of the following occur:

- a. The PUT does not transmit at least sixteen consecutive TS2 ordered sets after receiving one TS2 ordered set.
 - b. The PUT sends Idle symbols before the LVS sends at least eight consecutive TS2 ordered sets.
 - c. The PUT interrupts transmission of a TS2 ordered set to transmit a SKP or SYNC (for Gen 2 only) ordered set (between TS2 ordered sets is OK).
 - d. The PUT continues to transmit TS2 ordered sets after tRecoveryConfigurationTimeout expires.
7. The LVS transmits Idle symbols. In Gen 2 operation the LVS transmits a single SDS Ordered Set and then data blocks with Idle Symbols.
 8. The test fails if upon entering U0, the PUT does not transmit the Header Sequence Number Advertisement and the Rx Header Buffer Credit Advertisement or Type 1 and Type 2 Rx Header Buffer Credit Advertisement before their respective timeouts, PENDING_HP_TIMER and (Type 1 and Type 2) CREDIT_HP_TIMER, expire.
 9. The LVS and PUT continue the test with the Link Initialization Sequence starting at step two.

TD.7.27 Hot Reset Detection in Polling Test (Upstream Port Only)

This test verifies that the PUT detects the Hot Reset in Polling.

Covered Assertions

7.2.4.1.1#6,8,17,22

7.4.2#4

7.5.4.7.2#4

7.5.12.3.1#1,3,4

7.5.12.3.2#1

7.5.12.4.1#1

7.5.12.4.2#1

Overview of Test Steps

1. Both LVS and PUT detect each other and then transition through Polling to Polling.RxEQ.
2. Both LVS and PUT transmit the TS1 ordered sets during Polling.Active.
3. The LVS waits to receive TS2 ordered sets.
4. The test fails if the PUT does not transmit TS2s before tPollingActiveTimeout expires.
5. The LVS initiates a Hot Reset and transmits TS2 ordered sets with the Reset bit asserted.
6. The test fails if the PUT does not transmit at least sixteen TS2 ordered sets with the Reset bit asserted followed by two consecutive TS2 ordered sets with the Reset bit de-asserted.
7. The LVS transmits four consecutive TS2 ordered sets with the Reset bit de-asserted, and then transmits Idle Symbols for Gen 1, or an SDS Ordered Set followed by Idle Symbols for Gen 2.
8. The test fails if upon entering U0, the PUT does not transmit the Header Sequence Number Advertisement and the (Type 1 / Type 2) Rx Header Buffer Credit Advertisement before their respective timeouts, PENDING_HP_TIMER and (Type 1 / Type 2) CREDIT_HP_TIMER, expire.
9. The LVS and PUT exchange Port Configuration transactions.

10. The LVS will keep the link active by sending Link Pollings (LUP when it is configured as an Upstream Port or LDN when it is configured as a Downstream Port) for 50ms.
11. The test fails if the Port Configuration exchange sequences are not successful or the link does not stay in U0 for at least 50ms.

TD.7.28 Hot Reset Detection in U0 Test (Upstream Port Only)

This test verifies that the PUT detects the Hot Reset in U0 and does not start the Port Configuration Sequences.

Covered Assertions

- 7.2.4.1.1#6,8,17,22
- 7.4.2#2,4
- 7.5.10.4.1#1
- 7.5.12.3.1#1,2
- 7.5.12.3.2#1
- 7.5.12.4.1#1
- 7.5.12.4.2#1

Overview of Test Steps

1. Do steps 1 to 5 of the Link Initialization Sequence.
2. The LVS transmits TS1 ordered set to transition to Recovery.
3. The LVS waits to receive TS1 ordered sets.
4. The test fails if the PUT does not transmit TS1s before tU0RecoveryTimeout expires.
5. The LVS initiates a Hot Reset by transmitting TS2 ordered sets with the Reset bit asserted.
6. The test fails if the PUT does not transmit at least sixteen TS2 ordered sets with the Reset bit asserted followed by two consecutive TS2 ordered sets with the Reset bit de-asserted.
7. The LVS transmits four consecutive TS2 ordered sets with the Reset bit de-asserted, and then transmits Idle Symbols for Gen 1, or SDS Ordered Set followed by Idle Symbols for Gen 2.
8. The test fails if upon entering U0, the PUT does not transmit the Header Sequence Number Advertisement and the (Type 1/Type 2) Rx Header Buffer Credit Advertisement before their respective timeouts, PENDING_HP_TIMER and (Type 1/Type 2) CREDIT_HP_TIMER, expire.
9. The LVS will keep the link active by sending Link Pollings (LUP when it is configured as an Upstream Port or LDN when it is configured as a Downstream Port) for 50ms.
10. The test fails if the PUT retransmits Port Capability or Port Configuration LMPs.
11. The test fails if the Port Configuration exchange sequences are not successful and the link does not stay in U0 for at least 50ms.

TD.7.29 Hot Reset Initiation in U0 Test (Downstream Port Only)

This test verifies that the PUT initiates Hot Reset in U0.

Covered Assertions

7.2.4.1.1#6,8,17,22

7.4.2#2,4,10

7.5.4.6.1#1

7.5.4.7.2#3

7.5.10.4.1#1

7.5.12.3.1#1,2

7.5.12.3.2#1

7.5.12.4.1#1

7.5.12.4.2#1

Overview of Test Steps

1. Do steps 1 to 5 of the Link Initialization Sequence.
2. The LVS prompts the test operator to initiate a Hot Reset on the PUT through USB30CV.
3. The LVS waits for the PUT to send TS1s.
4. The test fails if the PUT does not transmit TS1s before tU0RecoveryTimeout expires.
5. The LVS transmits TS1 ordered sets and waits to receive TS2 ordered sets with the Reset bit asserted.
6. The test fails if the PUT does not transmit at least sixteen TS2 ordered sets with Reset bit asserted. After sixteen TS2 ordered sets with Reset bit asserted, the PUT may send Idle symbols before sending more TS2 ordered sets with Reset bit asserted.
7. The LVS transmits at least sixteen TS2 ordered sets with the Reset bit asserted, and then transmits two consecutive TS2 ordered sets with the Reset bit de-asserted.
8. The test fails if any of the following occur:
 - a. After LVS transmitted TS2 ordered sets with Reset bit de-asserted, the PUT does not transmit four consecutive TS2 ordered sets with the Reset bit de-asserted, when tHotResetActiveTimeout expires
 - b. The PUT transmits anything other than TS2 ordered sets or Idle symbols, before the LVS transmits TS2 ordered sets with the Reset bit de-asserted.
9. The LVS transmits Idle Symbols for Gen 1, or SDS Ordered Set followed by Idle Symbols for Gen 2.
10. The test fails if upon entering U0, the PUT does not transmit the Header Sequence Number Advertisement and the (Type 1/Type 2) Rx Header Buffer Credit Advertisement before their respective timeouts, PENDING_HP_TIMER and (Type 1/Type 2) CREDIT_HP_TIMER, expire.
11. The LVS will keep the link active by sending Link Pollings (LUP when it is configured as an Upstream Port or LDN when it is configured as a Downstream Port) for 50ms.
12. The test fails if the PUT retransmits Port Capability or Port Configuration LMPs.
13. The test fails if the Port Configuration exchange sequences are not successful and the link does not stay in U0 for at least 50ms.

TD.7.30 Recovery on three consecutive failed RX Header Packets Test

This test verifies that the PUT will enter Recovery if it fails to receive a header packet three consecutive times.

Covered Assertions

7.2.4.1.1#7,9

7.2.4.1.4#5

7.5.10.3.1#1

7.5.10.3.2#1

7.5.10.4.2#1

7.5.10.5.1#1

7.5.10.5.2#1

Overview of Test Steps

1. Do steps 1 to 3 of the Link Initialization Sequence.

Note: LVS completes each step in a timely manner so as to not contribute to a tPortConfiguration timeout during steps 1-5.

2. The LVS and the PUT will exchange Port Configuration transactions, but the first packet sent by the LVS will have an invalid CRC-5.
 - a. LVS waits for the PUT's Port Capability LMP.
 - b. LVS verifies that the Port Capability LMP is valid.
 - c. LVS transmits its Port Capability LMP with an invalid CRC-5.
 - d. LVS verifies that the PUT replies with an LBAD.
 - e. LVS transmits an LRTY and then retransmits the packet with an invalid CRC-5.
 - f. LVS verifies that the PUT replies with an LBAD.
 - g. LVS transmits an LRTY and then retransmits the packet with an invalid CRC-5.
 - h. LVS verifies that the PUT initiates Recovery.
3. The test fails if any of the following occur:
 - a. The PUT does not reply with LBAD to the first two packets (which have invalid CRC-5s)
 - b. The PUT does not initiate Recovery in step g within tRecoveryTransition.
 - c. The PUT initiates Recovery before the third invalid packet is received.
4. The LVS and PUT transition through Recovery to U0.
5. The LVS and the PUT perform the Link Initialization Sequence and exchange all remaining Port Configuration transactions.
6. The test fails if the PUT retransmits its Port Capability LMP.
7. The LVS will keep the link active by sending Link Pollings (LUP when it is configured as an Upstream Port or LDN when it is configured as a Downstream Port) for 50ms.
8. The test passes if the exchanges are successful, no timeout is detected, recovery is entered once, all packets are successfully received by the PUT except for the packet with invalid CRC-5, all credits are restored and the link stays in U0 for at least 50ms.

TD.7.31 Hot Reset Failure Test (Downstream Port Only)

This test verifies that the PUT initiates a Warm Reset when Hot Reset training fails.

Covered Assertions

7.4.2#6,8,14
7.5.3.3.1#1
7.5.10.3.2#5
10.3.1.6#6

Overview of Test Steps

1. Perform the Link Initialization Sequence to bring the LVS and PUT link to U0.
2. The LVS software prompts the test operator to initiate a Hot Reset on the PUT through USB30CV.
3. The LVS waits for the PUT to send TS1s.
4. The test fails if the TS1 Ordered Sets have the Reset bit set.
5. The LVS does not transmit anything in response to the PUT.
6. The test fails if the PUT does not transmit a Warm Reset LFPS after the tRecoveryActiveTimeout deadline and before tRecoveryActiveTimeout expires.
 - a. For a port with a captive re-timer, the port fails if the PUT does not transmit a Warm Reset LFPS after the tRecoveryActiveTimeout deadline and before tRecoveryActiveTimeout + 200us expires.
7. The LVS responds to the Warm Reset LFPS by entering Rx.Detect.
8. The LVS and PUT perform the Link Initialization Sequence to bring the link to U0.
9. The LVS will keep the link active by sending Link Pollings (LUP when it is configured as an Upstream Port or LDN when it is configured as a Downstream Port) for 50ms.
10. The test passes if the exchanges are successful, the PUT initiates a Warm Reset LFPS after tRecoveryActiveTimeout in Recovery.Active and the link reaches U0 with a correct Port Configuration Transaction and stays there for at least 50ms.

TD.7.32 Warm Reset Rx.Detect Timeout Test (Hub Downstream Port Only)

This test has been deleted. The assert has been covered in TD 10.109.

TD.7.33 Exit Compliance Mode Test (Upstream Port Only)

This test verifies that a device exits Compliance Mode when it receives a Warm Reset LFPS.

Covered Assertions

7.4.2#9
7.5.4.3.2#1
7.5.5.1#2
7.5.5.2#2

Overview of Test Steps

1. The LVS makes sure VBUS is off to assure a PowerOn Reset.
2. The LVS prompts the test operator to power cycle a self-powered device.

3. The LVS turns on VBUS, bringing the link to Rx.Detect.
4. The LVS presents Terminations and waits for the PUT to present Terminations.
5. When the LVS detects Terminations from the PUT, the LVS starts a timer for tPollingLFPSTimeout and does not transmit an LFPS.
6. When the timer expires, the LVS verifies that the device is in Compliance Mode by sending Ping.LFPS until it can verify that the LVS is receiving a Compliance Pattern, (at most by the COMs in the 4th Compliance Pattern).
7. The test fails if the LVS cannot verify a Compliance Pattern coming from the PUT.
8. The LVS transmits a Reset.LFPS and enters Rx.Detect.
9. The LVS and PUT perform the Link Initialization Sequence to bring the LVS and PUT link to U0.
10. The LVS will keep the link active by sending Link Pollings (LUP when it is configured as an Upstream Port or LDN when it is configured as a Downstream Port) for 50ms.
11. The test passes if all exchanges are successful and the PUT stays in U0 for 50ms.

TD.7.34 Exit Compliance Mode Test (Downstream Port Only)

This test verifies that a downstream port instructed to Reset while in Compliance Mode initiates a Warm Reset.

Covered Assertions

7.4.2#9

7.5.4.3.2#2

7.5.5.1#2

7.5.5.2#1

Overview of Test Steps

1. The LVS prompts the test operator to enable Compliance Mode through USB30CV. CV will send SetPortFeature(PORT_LINK_STATE) = Compliance Mode for the PUT.
2. The LVS presents termination to the PUT.
3. When the LVS detects VBUS and Terminations from the PUT, the LVS starts a timer for tPollingLFPSTimeout and does not transmit an LFPS.
4. When the timer expires, the LVS verifies that the device is in Compliance Mode by sending Ping.LFPS until it can verify that the LVS is receiving a Compliance Pattern, (at most by the COMs in the 4th Compliance Pattern).
5. The test fails if the LVS cannot verify a Compliance Pattern coming from the PUT.
6. The LVS prompts the test operator to Reset the PUT through USB30CV and then hit “OK”.
7. The LVS waits to receive a Warm Reset LFPS from PUT.
8. The test fails if the LVS does not receive a Warm Reset LFPS before the test operator hits “OK”.
9. The LVS closes the prompt automatically when it receives a Warm Reset LFPS.
10. The LVS transitions to Rx.Detect.Reset for the duration of the Warm Reset LFPS.
11. The LVS transitions to Rx.Detect and the LVS and PUT transition through Polling to U0.

12. The LVS will keep the link active by sending Link Pollings (LUP when it is configured as an Upstream Port or LDN when it is configured as a Downstream Port) for 50ms.
13. The test passes after the Port Configuration exchange is successful and the link stays in U0 for 50ms.

TD.7.35 Exit U3 by Reset Test (Downstream Port Only)

This test verifies that a downstream port instructed to Reset during U3 initiates a Warm Reset.

Covered Assertions

7.2.4.2.4#1,4,5

7.5.9.2#2

Overview of Test Steps

1. Perform the Link Initialization Sequence to bring the LVS and PUT link to U0.
2. The LVS software prompts the test operator to Suspend the PUT to U3 through USB30CV.
3. The LVS waits to receive an LGO_U3 from the PUT.
4. The LVS sends an LAU when it receives an LGO_U3 from the PUT.
5. The LVS waits to receive an LPMA from the PUT.
6. The test fails if any of the following occur:
 - a. The LVS does not receive an LGO_U3
 - b. The LVS does not receive an LPMA before PM_ENTRY_TIMER deadline.
 - c. The PUT fails to transition to U3 after PM_ENTRY_TIMER expires.
7. The LVS prompts the test operator to Reset the PUT through USB30CV and then hit “OK” on the prompt.
8. The LVS waits to receive a Warm Reset LFPS from PUT.
9. The test fails if no Warm Reset LFPS is received by the LVS before the test operator hits “OK”.
10. When the LVS receives a Warm Reset LFPS the prompt is closed automatically.
11. The LVS transitions to Rx.Detect.Reset for the duration of the Warm Reset LFPS.
12. The LVS transitions to Rx.Detect and the LVS and PUT transition through Polling to U0.
13. The LVS will keep the link active by sending Link Pollings (LUP when it is configured as an Upstream Port or LDN when it is configured as a Downstream Port) for 50ms.
14. The test passes after the Port Configuration exchange is successful and the link stays in U0 for 50ms.

TD.7.36 Exit U3 Test (Host Downstream Port Only)

This test verifies that a downstream port initiates U3 exit with a U3 exit LFPS.

Note: This test is performed on host silicon only. This test is not performed on end products. The operator must install the Product-Specific host controller driver to perform this test. It cannot be tested with the Compliance driver. The LVS is configured to appear to the host controller as a device.

Covered Assertions

7.2.4.2.4#1,4,5

7.2.4.2.7#1

7.5.9.1#4

7.5.9.2#5

Overview of Test Steps

1. Perform the Link Initialization Sequence to bring the LVS and PUT link to U0. The PUT host controller machine enumerates the LVS.
2. The LVS software prompts the test operator to put the PUT host controller machine to sleep or, if the DUT is an Embedded Host and power is lost to the host during sleep, to U3.
3. The LVS waits to receive an LGO_U3 from the PUT.
4. The LVS sends an LAU when it receives an LGO_U3 from the PUT.
5. The LVS waits to receive an LPMA from the PUT.
6. The test fails if any of the following occur:
 - a. The LVS does not receive an LGO_U3
 - b. The LVS does not receive an LPMA before PM_ENTRY_TIMER deadline.
7. The LVS prompts the test operator to verify that the host controller machine is in a sleep state.
8. The LVS prompts the test operator to wake the host controller machine.
9. The LVS waits to receive a U3 Exit LFPS from PUT.
10. The test fails if no U3 Exit LFPS is received.
11. The LVS sends a U3 Exit LFPS 5ms after detecting an LFPS from the PUT.
12. The LVS and PUT transition through Recovery to U0.
13. The LVS will keep the link active by sending Link Pollings (LUP when it is configured as an Upstream Port or LDN when it is configured as a Downstream Port) for 50ms.

TD.7.37 Packet Pending Test (Upstream Port Only)

This test verifies that the PUT releases its Packet Pending flag at the end of a Control Transfer.

Covered Assertions

8.6#1

Overview of Test Steps

1. Perform the Link Initialization Sequence to bring the LVS and PUT link to U0. The LVS enumerates the PUT to a configured state.
2. If the PUT is an US port of a hub, the LVS issues a SetPortFeature(PLS=4) for each DS port on the hub.
3. The LVS software issues a GetDescriptor request SETUP packet, with the PP bit set to 1.
4. The LVS sends an ACK TP, with the PP bit set to 1, to start the IN stage of the GetDescriptor request.
5. The LVS waits to receive IN data from the PUT.

6. The LVS software issues a GetDescriptor STATUS packet, with a PP bit set to 0.
7. The LVS waits to receive ACK TP from the PUT, concluding the GetDescriptor request.
8. The test fails if the GetDescriptor request is not completed.
9. If the LVS has received an LDM Timestamp Exchange message:
 - a. The LVS waits until it receives three LDM Timestamp Exchange messages.
 - b. The LVS waits 125 uS.
10. The LVS sends an LGO_U1 and waits to receive LAU from the PUT.
11. The test fails if the PUT does not send an LAU.
12. The LVS transmits an LPMA and then transitions to U1.
13. The test fails if the PUT does not transition to U1, or if the PUT sends any packet.

TD.7.38 Port Capability Tiebreaker Test

This test verifies that the PUT accepts ports capable of both US and DS operation, and that a PUT capable of both US and DS operation resends its Port Capability info with a randomly generated tiebreaker after the first tiebreaker is the same value as its link partner's.

Covered Assertions

TBD

Overview of Test Steps

1. Perform steps 1 through 3 of the Link Initialization Sequence.
2. The LVS waits to receive the Port Capability LMP.
3. The test fails if the Port Capability LMP received is not valid.
4. If the LVS is configured as a Downstream Port:
 - a. The LVS sends a Port Capability LMP indicating it is capable of both US and DS operation.
 - b. The test continues at step 4.d. of the Link Initialization Sequence.
5. If the LVS is configured as an Upstream Port:
 - a. If the Port Capability LMP from the PUT indicates that the port only supports DS operation:
 - i. The LVS sends a Port Capability LMP indicating it is capable of both US and DS operations.
 - ii. The test continues at step 4.d of the Link Initialization Sequence.
 - b. If the Port Capability LMP from the PUT indicates that the port supports both US and DS operation:
 - i. The test continues at step 6 of this test.
6. The LVS records the tiebreaker value on the received LMP as X, and initializes a counter to 1.
7. The LVS sends a Port Capability LMP with DS and US capability set to 1, and its tiebreaker value set to X.
8. The LVS waits to receive another Port Capability LMP.
 - a. The test fails if the LVS does not receive another Port Capability LMP within tPortConfigurationTimeout.

- b. If the tiebreaker value is X and the counter value is less than 5:
 - i. Increment the counter.
 - ii. Go to step 7.
 - c. The test fails if the tiebreaker value is X and the counter value is 5.
 - d. If the tiebreaker value is not X, move to step 9.
9. The LVS sends a Port Capability LMP with DS and US capability set to 1, and its tiebreaker value set higher than the tiebreaker value on the received LMP.
10. Perform the Link Initialization Sequence starting at step 4.d with the LVS as a Downstream Port
11. The test fails if the PUT does not stay in U0 for 50ms.
12. If the PUT includes a captive re-timer:
- a. For a DFP:
 - i. Use USBCV31 Link Layer helper TD 7.18 to initiate an entry to LGO_U1
 - ii. The test fails if the LVS does not receive an LGO_U1
 - iii. The LVS sends an LAU and enters U1 after receiving LPMA or PM_ENTRY_TIMER timeout
 - iv. The test fails if the LVS receives TS1s
 - v. Wait 1 second
 - vi. The test fails if the LVS does not receive Ping.LFPSs after 300ms with tBurst and tRepeat as defined in Table 6-30.
 - b. For a UFP:
 - i. The LVS sends LGO_U1
 - ii. The test fails if the LVS does not receive an LAU
 - iii. The LVS sends an LPMA and enters U1
 - iv. The test fails if the LVS receives TS1s.
 - v. Wait 1 second
 - vi. The test fails if the LVS receives any LFPS

TD.7.39 PortMatch Retry Test (Gen 2 Only)

This test verifies that the PUT recovers to Polling.PortMatch when the tPollingActiveTimeout expires.

Covered Assertions

7.5.4.5.2#2

7.3.10#1

Overview of Test Steps

1. Both LVS and PUT detect each other and then transition through Polling to Polling.RxEQ.
2. The LVS does not transmit the TS1 ordered sets during Polling.Active.
3. The test fails if:
 - a) The PUT does not transition to Polling.PortMatch after tPollingActiveTimeout.

- b) The PUT does not transmit the next highest PHY Capability from its previous PHY Capability in its PHY Capability LBPMs.
- 4. Both LVS and PUT transition through Polling.RxEQ
- 5. If the PHY Capability was not negotiated to 5Gbps, return to step 2.
- 6. Both LVS and PUT transmit the TS1 ordered sets during Polling.Active and proceed to U0.
- 7. The LVS will keep the link active by sending Link Pollings (LUP when it is configured as an Upstream Port or LDN when it is configured as a Downstream Port) for 50ms.
- 8. The test fails if the Port Configuration exchange sequences are not successful or the link does not stay in U0 for at least 50ms.

TD.7.40 Polling Retry Test (Downstream Port Only)

This test verifies that the PUT recovers to Rx.Detect twice, and then eSS.Inactive when tPollingLFPSTimeout expires.

Covered Assertions

- 7.3.10#2,3
- 7.5.4.2#2
- 7.5.4.3.2#6,7
- 7.5.4.8.2#3,4
- 7.5.4.9.2#3

Overview of Test Steps

1. LVS presents terminations.
2. For a PUT with a captive re-timer:
 - (1) The test fails if PUT does not transition to Polling.LFPS within 200ms.
 - (2) LVS transmits 16 Polling.LFPS
 - (3) LVS prompts user to send Warm Reset through USB3CV
3. The LVS does not send any signal until step 15.
4. The test fails if the PUT does not transition to Polling.LFPS within 200ms.
5. For a PUT with a captive re-timer, note that the PUT should continuously cycle back to Rx.Detect after 24ms in Polling.LFPS and then transition back to Polling.LFPS within 8ms after. Therefore the LVS will detect the PUT in the Polling.LFPS state for at least 24ms each time it enters the state. When the PUT transitions to Rx.Detect due to the tPollingLFPSTimeout the LVS may detect a “short transition” where the PUT is in the Polling.LFPS state for less than 24ms before transitioning to Rx.Detect:
 - (1) The test fails if the PUT does not transition to Rx.Detect between 24 and 36 ms after each transition to Polling.LFPS.
 - (2) The test fails if the PUT does not transition to Polling.LFPS within 8ms after each transition to Rx.Detect.
 - (3) The test fails if the PUT detects a "short transition" before the tPollingLFPSTimeout deadline.

- (4) If a “short transition” occurs after tPollingLFPSTimeout deadline and before the expiration, the LVS resets the tPollingLFPSTimeout at the start of the Rx.Detect after the “short transition”.
 - (5) If no “short transition” is detected before the tPollingLFPSTimeout expiration, the last transition to Rx.Detect before the expiration will prompt the LVS to reset the tPollingLFPSTimeout.
 - (6) LVS continues to step 7.
6. The test fails if the PUT does not transition to Rx.Detect within tPollingLFPSTimeout expiration after the step 4 transition to Polling.LFPS.
7. The test fails if the PUT does not transition to Polling.LFPS within 200ms.
8. For a PUT with a captive re-timer:
 - (1) The test fails if the PUT does not transition to Rx.Detect between 24 and 36 ms after each transition to Polling.LFPS.
 - (2) The test fails if the PUT does not transition to Polling.LFPS within 8ms after each transition to Rx.Detect.
 - (3) The test fails if the PUT detects a "short transition" before the tPollingLFPSTimeout deadline.
 - (4) If a “short transition” occurs after tPollingLFPSTimeout deadline and before the expiration, the LVS resets the tPollingLFPSTimeout at the start of the Rx.Detect after the “short transition”.
 - (5) If no “short transition” is detected before the tPollingLFPSTimeout expiration, the last transition to Rx.Detect before the expiration will prompt the LVS to reset the tPollingLFPSTimeout.
 - (6) LVS continues to step 10.
9. The test fails if the PUT does not transition to Rx.Detect within tPollingLFPSTimeout expiration after the step 7 transition to Polling.LFPS.
10. The test fails if the PUT does not transition to Polling.LFPS within 200ms.
11. For a PUT with a captive re-timer:
 - (1) The test fails if the PUT does not transition to Rx.Detect between 24 and 36 ms after each transition to Polling.LFPS.
 - (2) The test fails if the PUT does not transition to Polling.LFPS within 8ms after each transition to Rx.Detect.
 - (3) The test fails if the PUT detects a "short transition" before the tPollingLFPSTimeout deadline.
12. The test fails if the PUT does not transition to eSS.Inactive within tPollingLFPSTimeout expiration after the step 10 transition to Polling.LFPS.
13. If PUT is operating in Gen 1x1, continue with the rest of the test steps.
14. The LVS removes terms for 200ms and presents terms.
15. The LVS and PUT transition through Polling.LFPS to Polling.Active.
16. The LVS does not transmit the TS1 ordered sets during Polling.Active.
17. The test fails if the PUT does not transition to Rx.Detect after tPollingActiveTimeout.
18. The LVS and PUT transition through Polling.LFPS to Polling.Configuration.
19. The LVS does not transmit the TS2 ordered sets during Polling.Configuration.
20. The test fails if the PUT does not transition to Rx.Detect after tPollingConfigurationTimeout.
21. The LVS and PUT transition through Polling.LFPS to Polling.Active.
22. The LVS does not transmit the TS1 ordered sets during Polling.Active.
23. The test fails if the PUT does not transition to eSS.Inactive after tPollingActiveTimeout.

TD.7.41 SetAddress TPF Bit Test (Gen 2 Upstream Port Only)

This test verifies that the PUT sets the TPF bit at the end of a SetAddress Control Transfer.

Covered Assertions

8.5.6.7#2

Overview of Test Steps

1. Perform the Link Initialization Sequence to bring the LVS and PUT link to U0.
2. The LVS sends a SetAddress command to the PUT.
3. The test fails if:
 - a. The SetAddress control transfer does not complete.
 - b. The ACK response to the STATUS packet of the control transfer does not have the TPF bit set to 1.

TD.7.42 Symbol to Block Alignment Test (Gen 2 Only)

Condition to be tested:

- A. Start every Packet in the 0th symbol of a block.
- B. Start every Packet in the 1st symbol of a block.
- C. Start every Packet in the 2nd symbol of a block.
- D. Start every Packet in the 3rd symbol of a block.
- E. Start every Packet in the 4th symbol of a block.
- F. Start every Packet in the 5th symbol of a block.
- G. Start every Packet in the 6th symbol of a block.
- H. Start every Packet in the 7th symbol of a block.
- I. Start every Packet in the 8th symbol of a block.
- J. Start every Packet in the 9th symbol of a block.
- K. Start every Packet in the 10th symbol of a block.
- L. Start every Packet in the 11th symbol of a block.
- M. Start every Packet in the 12th symbol of a block.
- N. Start every Packet in the 13th symbol of a block.
- O. Start every Packet in the 14th symbol of a block.
- P. Start every Packet in the 15th symbol of a block.

Covered Assertions

7.2.1.3#1,2

Overview of Test Steps

5. Do steps 1 to 4 of the Link Initialization Sequence.
6. The LVS will keep the link active by sending Link Pollings (LUP when it is configured as an Upstream Port or LDN when it is configured as a Downstream Port) for 50ms. All data blocks will be generated according to Condition A described above.
7. At this stage the Downstream Port is expected to issue a GetDeviceDescriptor request.

- a. If the LVS is configured as an Upstream Port:
 - i. The LVS prompts the test operator to have the PUT send a GetDeviceDescriptor request through USB30CV and then press “OK”.
 - ii. The test fails if no GetDeviceDescriptor request is received and the test operator has pressed “OK”.
 - iii. When the LVS receives a GetDeviceDescriptor request, it closes the prompt, and responds to the request as appropriate.
 - b. If the LVS is configured as a Downstream Port, it will issue a GetDeviceDescriptor request, and complete the transaction as appropriate.
8. The test passes if the exchanges are successful, no timeout is detected, no recovery is entered, all packets are successfully received, all credits are restored and the link stays in U0 for at least 50ms.
 9. Repeat the steps with the next combination listed above.