USB4™

Time Measurement Equipment – Setup Procedure

Date: September 2023

Revision: 1.03

Copyright © 2021 USB Implementers Forum, Inc.

All rights reserved

THIS PROCEDURE IS PROVIDED TO YOU “AS IS” WITH NO WARRANTIES WHATSOEVER, INCLUDING ANY WARRANTY OF MERCHANTABILITY, NON-INFRINGEMENT, OR FITNESS FOR ANY PARTICULAR PURPOSE. THE AUTHORS OF THIS SPECIFICATION DISCLAIM ALL LIABILITY, INCLUDING LIABILITY FOR INFRINGEMENT OF ANY PROPRIETARY RIGHTS, RELATING TO USE OR IMPLEMENTATION OF INFORMATION IN THIS SPECIFICATION. THE PROVISION OF THIS SPECIFICATION TO YOU DOES NOT PROVIDE YOU WITH ANY LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE, TO ANY INTELLECTUAL PROPERTY RIGHTS.

USB Type-C™, USB-C™, USB 2.0 Type-C™, and USB4™ are trademarks of the Universal Serial Bus Implementers Forum (USB-IF). Thunderbolt™ is a trademark of Intel Corporation. All product names are trademarks, registered trademarks, or service marks of their respective owners.

Revision History:

Revision	Issue Date	Comments
1.00	July 2021	Initial release.
1.01	August 2021	Editorial changes. Updated list of provided files to include **tmu_fpga.exe**. Made troubleshooting section for USB ethernet gadget into its own step.
1.02	March 2022	Editorial changes. Update instructions for making STLP cable to simpler method.
1.03	September 2023	Updated the KG USB4 Device board

Table of Contents

Introduction

Time Measurement Equipment is an essential part of Time Synchronization Compliance testing. It is based on the Serial Time Link Protocol (STLP) that transmits current Grand Master time every 16 □sec. STLP is parsed and analyzed by a *Time Measurement Equipment*, which is FPGA based hardware.

There are two usages for such equipment:

Standalone Measurement

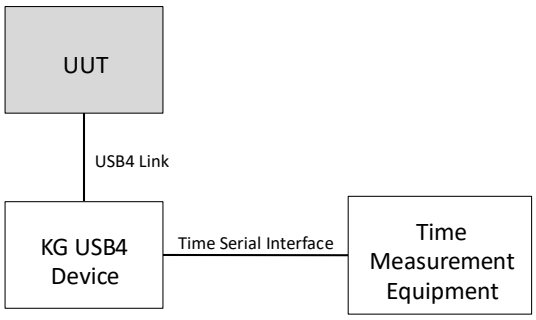


Figure 1: Standalone setup

Comparative Time Measurement

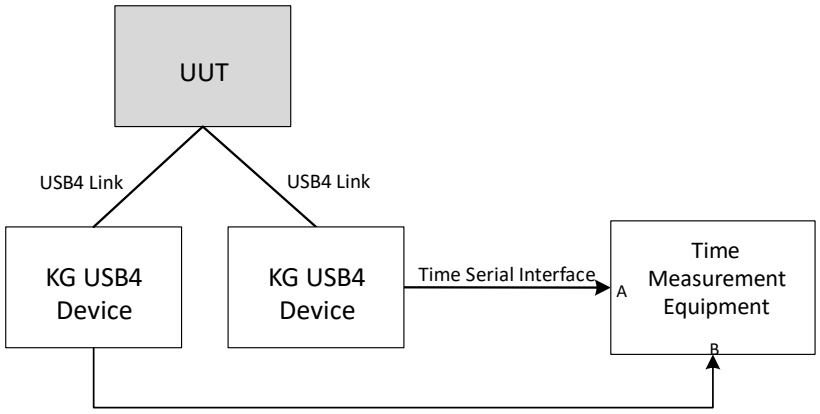


Figure 2: Pair Setup

A. Required Hardware and Software

Hardware	Vendor	Link

Quad Motherboard	proFPGA	https://www.profpga.com/products/motherboardsoverview/profpga-quad
Virtex 7 Module XC7V2000T	proFPGA	https://www.profpga.com/products/fpga-modulesoverview/virtex-7-based/profpga-xc7v2000t
Case (optional)	proFPGA	https://www.profpga.com/products/miscellaneousoverview/duo-
Goodway Gatkex Board with TMU CLK Out Board (**DBD1210L1)**	Good Way Technology Co., Ltd.	https://www.goodway.com.tw/

Software	**Vendor**	**Link**
proFPGA-2020C-install.exe	proFPGA	**Contact proFPGA for this software*
Files to use with USB4CV	USB-IF	https://usb.org/compliancetools#anchor_usb4tools

Please contact proFPGA about getting the necessary items listed above.

https://www.profpga.com/
email: profpga@prodesign-europe.com

A1. Quad Motherboard

Figure 3: Quad Motherboard

A2. Duo & Quad Casing (optional)

Figure 4: Optional case for FPGA

A3. Virtex® 7 module XC7V2000T

Figure 5: Virtex® 7 module

A4. Goodway Gatkex Board with TMU CLK Out as USB4 KG Device:

Contact Info: raymond_chan@goodway.com.tw & vivian_liao@goodway.com.tw

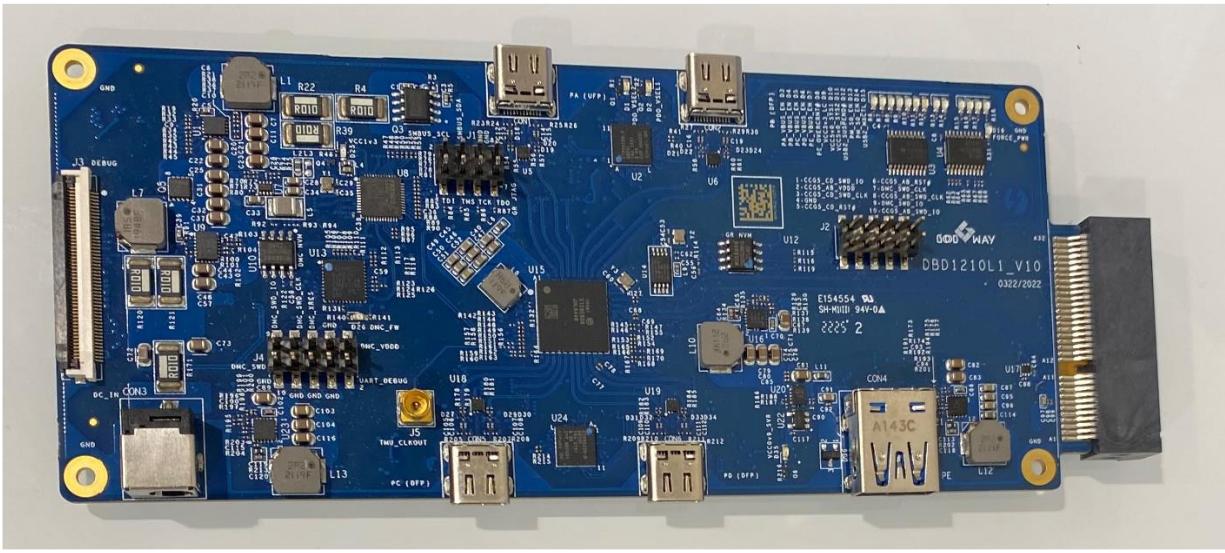


Figure 6: Goodway Gatkex Board with TMU CLK Out

A5. STLP Cable

STLP cable connects Goodway Gatkex Board TMU_CLK_OUT output and carries STLP protocol to FPGA.

The cable has 3 ends as shown on the following figure.

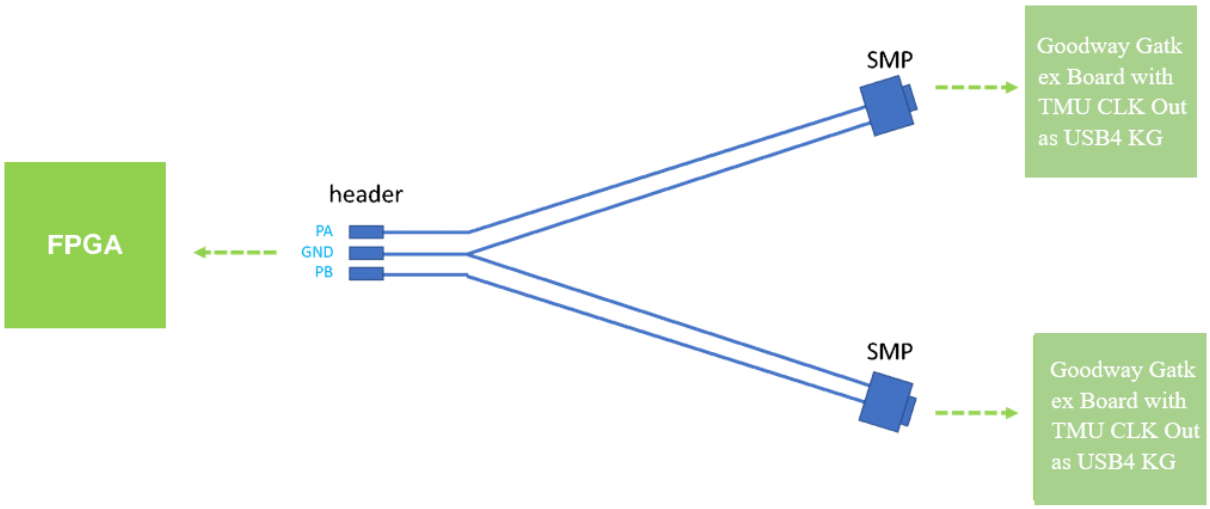


Figure 7: Example

One end of the cable connects to Goodway Gatkex Board with TMU CLK Out with SMP connector:

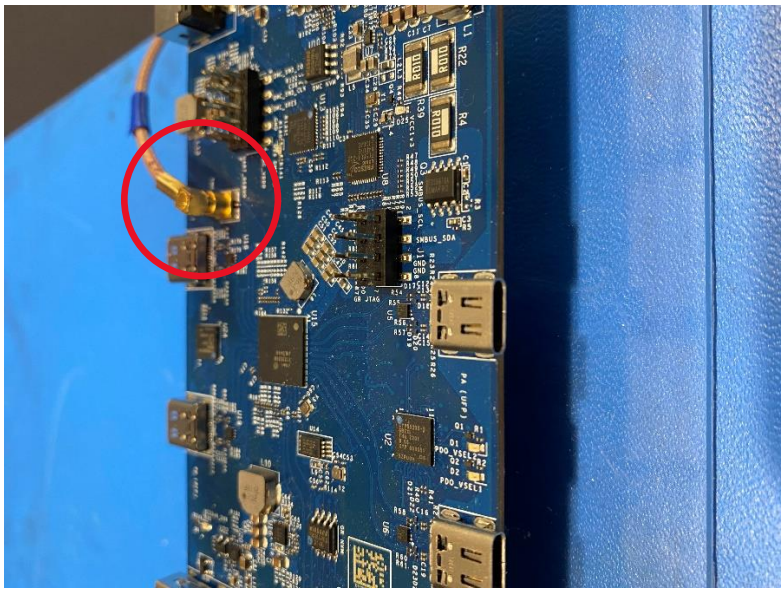


Figure 8: Connecting SMP to Goodway Gatkex Board with TMU CLK Out

The other end of the cable has female header (size 0.1”):

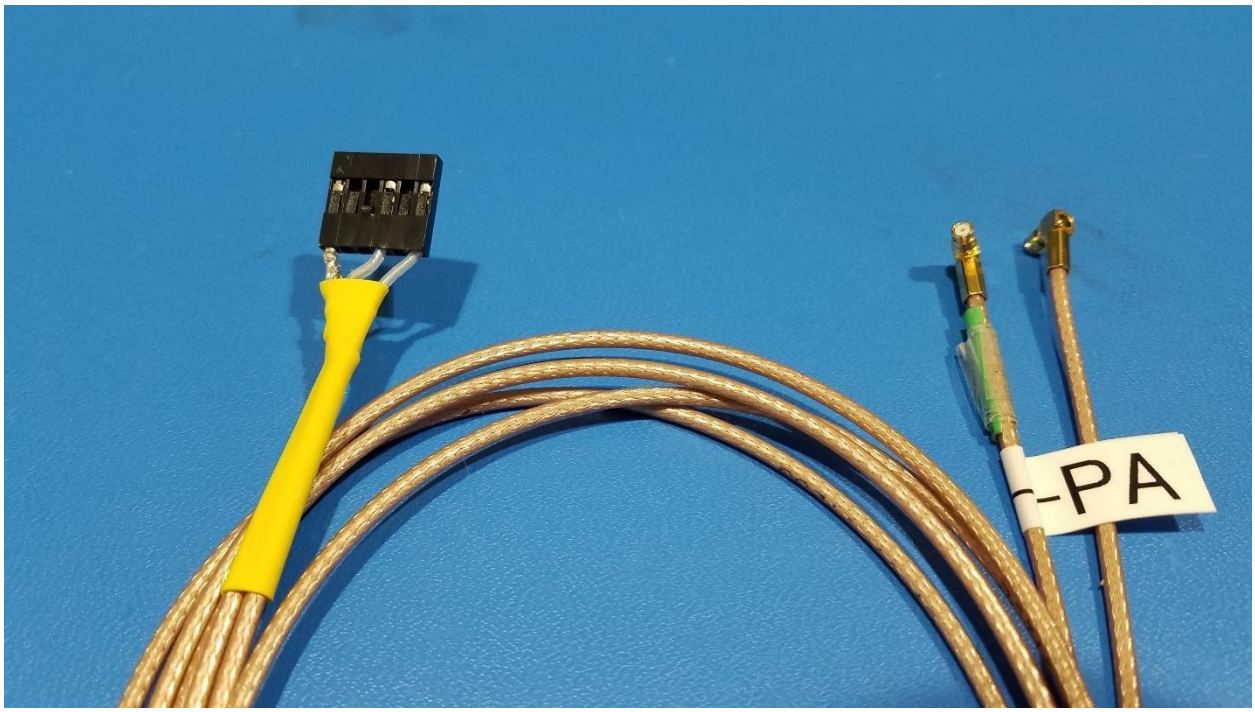


Figure 9: STLP cable showing both ends. 0.1” 6pin housing and push-on SMP connectors

A5.1. STLP Cable construction procedure for the Goodway Gatkex Board with TMU CLK Out

These instructions can be used to make custom cables for testing products that do not use SMP connectors for TMU_CLK_OUT.

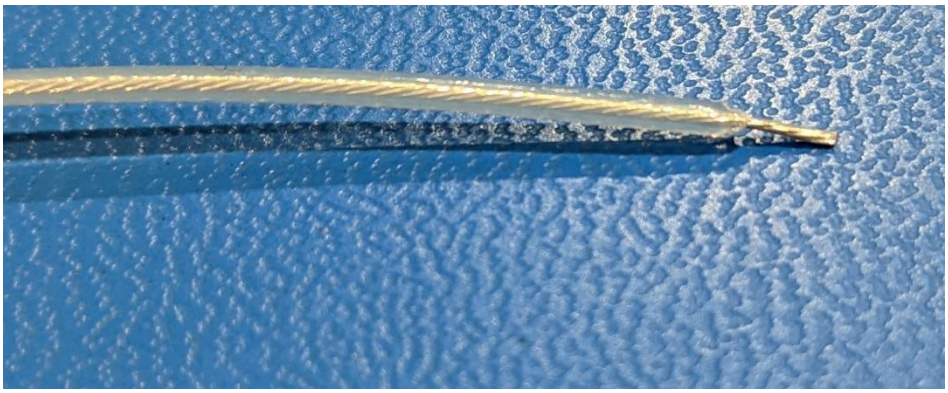
The following materials will be necessary:

- 2x RF cables each at least 48inches long with push-on SMP connectors.
  Note: Do not use semi-rigid type. Choose braided shielding (eg: PE3C3584/PH180-48)
- 1x 0.1inch (2.54mm) Crimp connector housing 1x6-pin
- Wire stripper
- Heat shrink tubes
- 3x Heat shrink tubes with solder ring
- Heat gun
- 3x 2inch pre-crimped wires
- Hot glue gun

1. Strip at least 1" of the outer insulation.

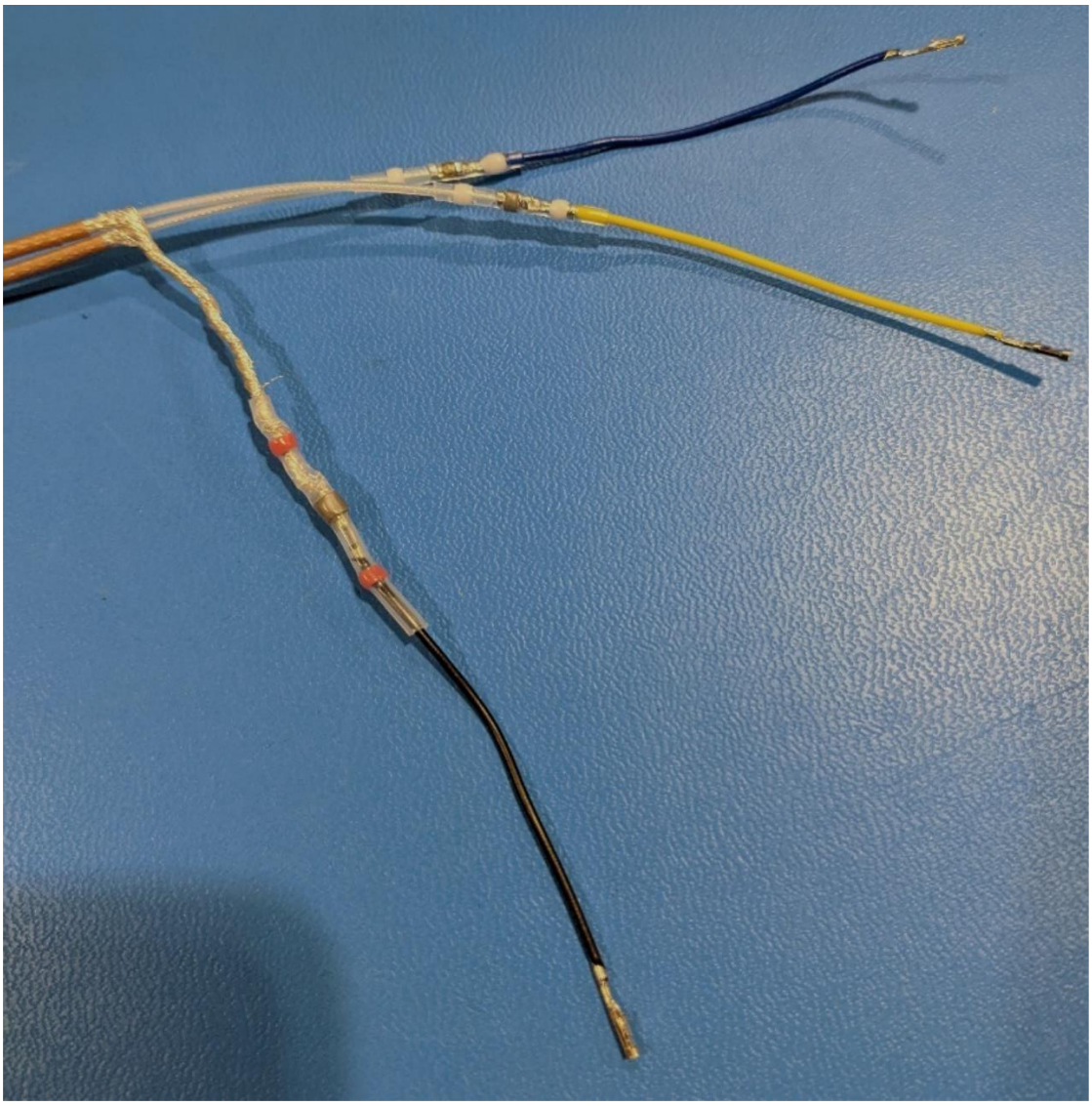
2. Carefully undo the braided shielding. It is recommended to use a small and fine tool to poke into the braids and pull towards the open end of the cable. Start from the end of the cable and slowly work down to slowly undo the braiding.

3. Strip about ¼ inch of the dielectric insulation to expose the center conductor.



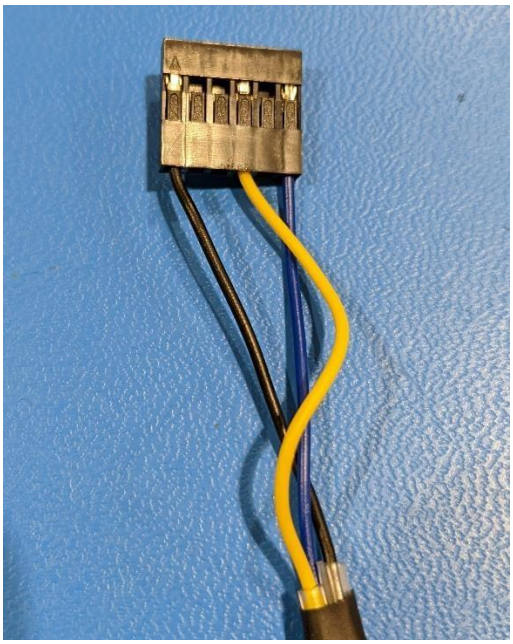
4. Take a pre-crimped wire and feed into a heat shrink tube with solder ring. Take the exposed center conductor and insert into one of the crimps. Then pull the heat shrink tube over this connection and line the solder ring up with the metal-to-metal contact portion.

5. Use heat gun to shrink the tube and pay extra attention to melt the solder ring. Solder ring should visibly deform or fill in gaps of the crimp contact.
6. Repeat steps 1-5 for the second cable.
7. Combine both Ground braids by twisting them together. Repeat steps 4 and 5 on this combined braid.

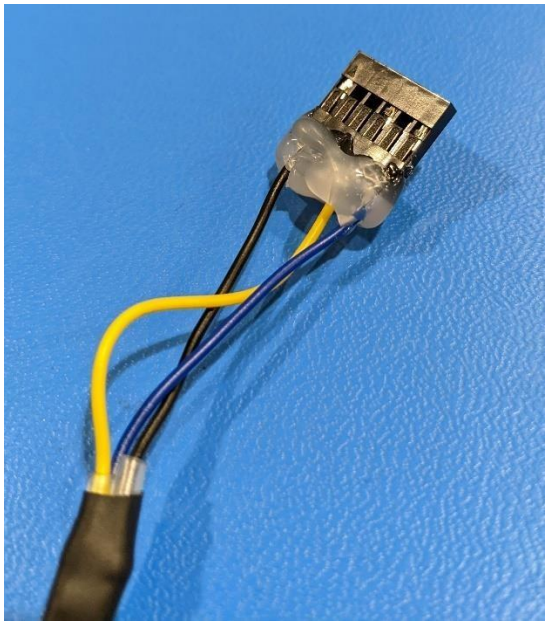


8. Use heat shrink (no solder ring) to cover excess exposed braiding.

9. Insert pins into the housing and give it a light tug test to ensure that the pin is secured in place:
    - GND braids to pin 1 (GND)
    - Choice of cable to pin 4 (PB)
    - Remaining cable to pin 6 (PA)



10. Apply hot glue to bottom of housing. Make sure to fill in spaces between the three cables and also overlap onto the plastic housing to prevent the cables from bending when attaching this cable to FPGA.



B. Connecting the system

B1. Installing the module

Virtex® 7 module shall be installed on connector TA1 of Quad Motherboard

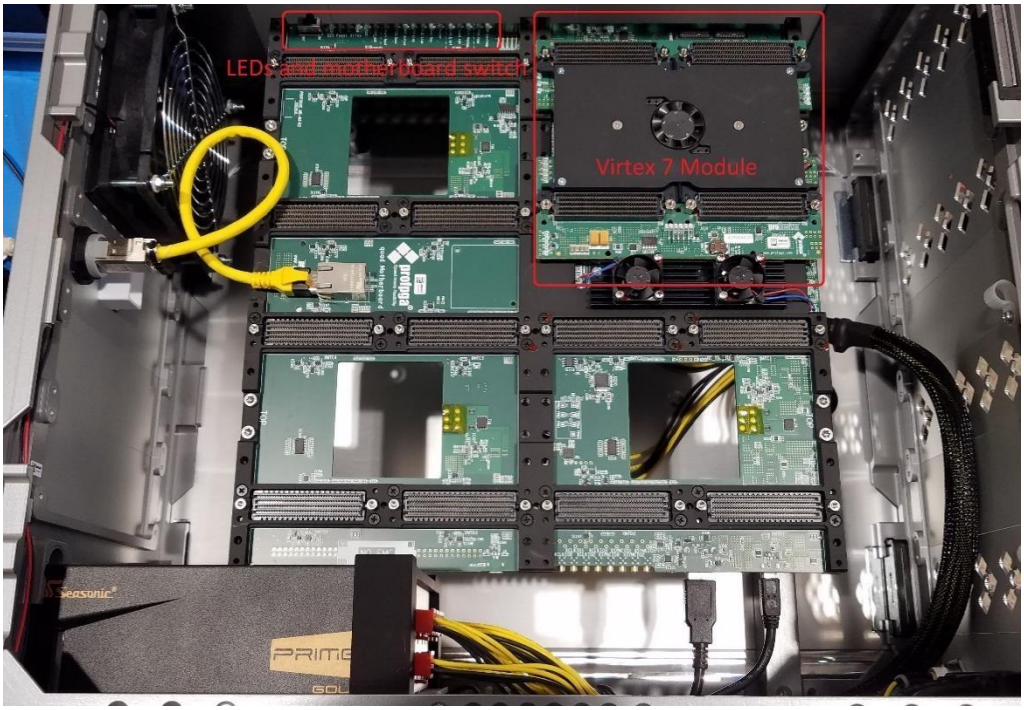


Figure 10: Virtex ® 7 Module position on Quad Motherboard

B2. Connecting STLP cable

STLP cable will need to be connected to the following pins located on the Virtex module:

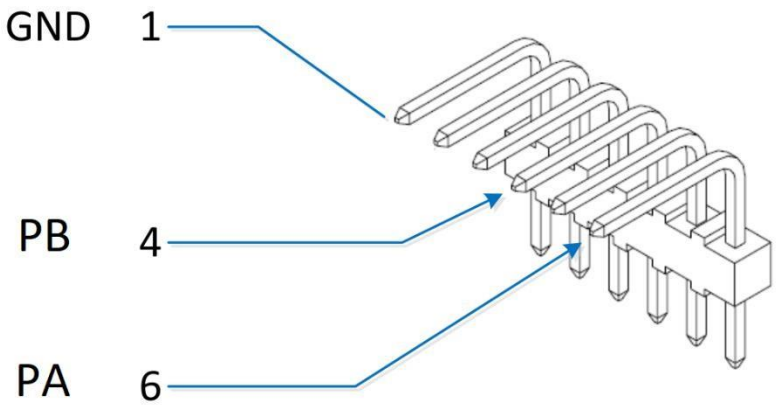


Figure 11: Virtex ® 7 Module Pins

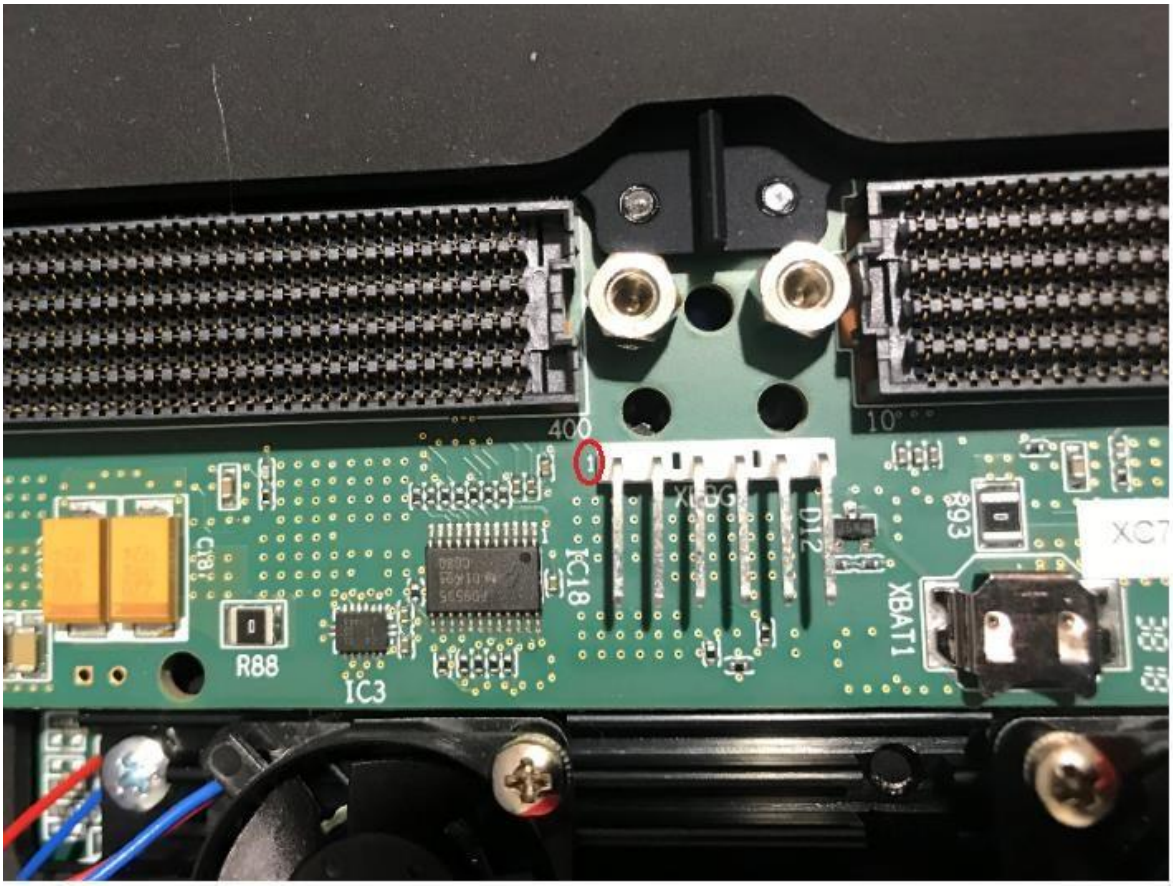


Figure 12: Pin 1 on ProFPGA

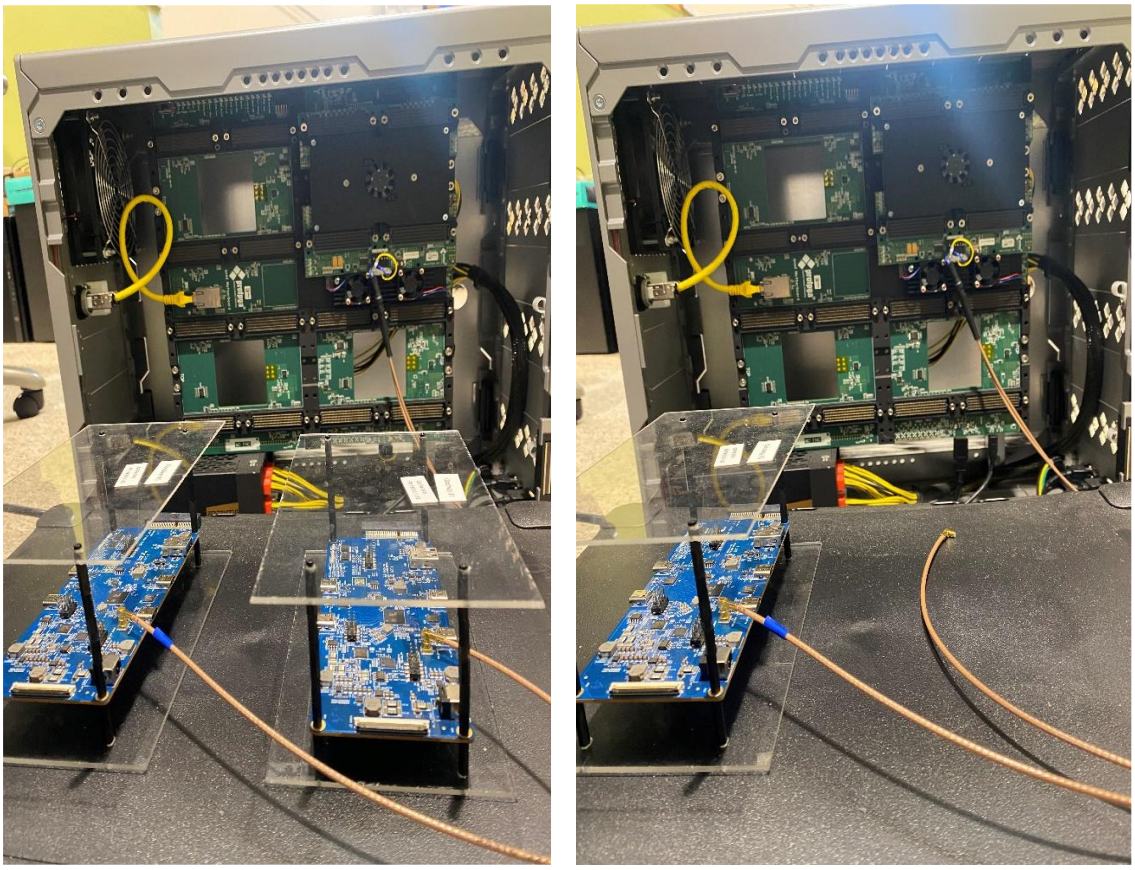


Figure 13: Connecting proFPGA and Goodway Gatkex Board using STLP cable. (Left) Both PA and PB connected. (Right) Only PA connected.

C. proFPGA Initial Setup on USB4CV System

This setup procedure only needs to be done once on a system and tester will only need to rely on the provided batch files for startup and shut down of the FPGA.

You will need to contact proFPGA for software install executable. Their contact can be found in the Required Hardware and Software section of this document.

The following files are provided by the USB-IF at https://usb.org/compliancetools#anchor_usb4tools to use proFPGA with USB4CV:

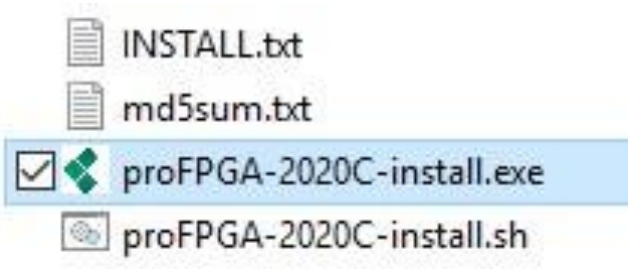
- TMU_FPGA.bat
- tmu_fpga.exe
- proj.cfg
- fmxc7v2000tr2.bit
- fpga_startup.bat
- fpga_shutdown.bat

All files should be placed into the following path to use with USB4CV:

C:\Users\Public\Documents\TMU_FPGA\USB4_Compliance

C1. Install proFPGA software

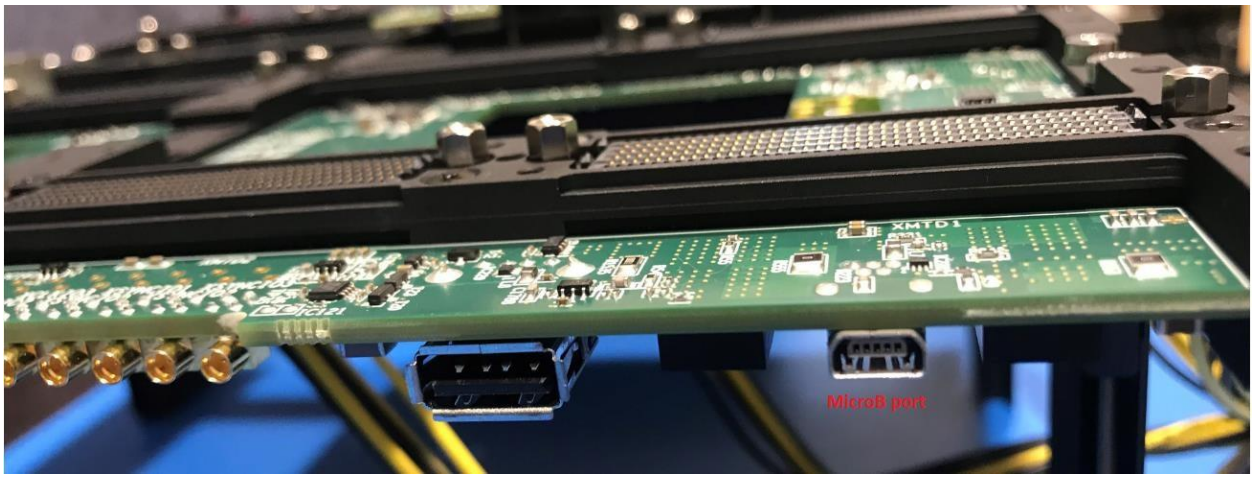
Run proFPGA software installation executable and set install path to **C:\ProDesign\proFPGA-2020C**



C2. Connect proFPGA to USB4CV System

1. Turn on the power supply.
2. Change the switch on mother board from OFF to ON
3. Connect proFPGA to USB4CV System:
   i. If you purchased the optional case for the FPGA, use a USB2.0 STD B to A cable to **connect STD B port on front of proFPGA to USB-A port on USB4CV System.** (Do not use the ethernet port on the FPGA)

   ii. If you did not get the optional case for the FPGA, use a USB2.0 microB to A cable to **connect from microB port on proFPGA to Type A port on USB4CV System**.



C3. Install Driver for USB Ethernet/RNDIS Gadget

This driver is needed to interface with the FPGA through the USB-A port.

C3.1. Identify Device Driver for FPGA

Open Device Manager. The device is most likely listed as a Serial Device COM under ‘Ports (COM & LPT)’.

Verify this device is the FPGA by unplugging FPGA from the USB4CV System and seeing if the device goes away.

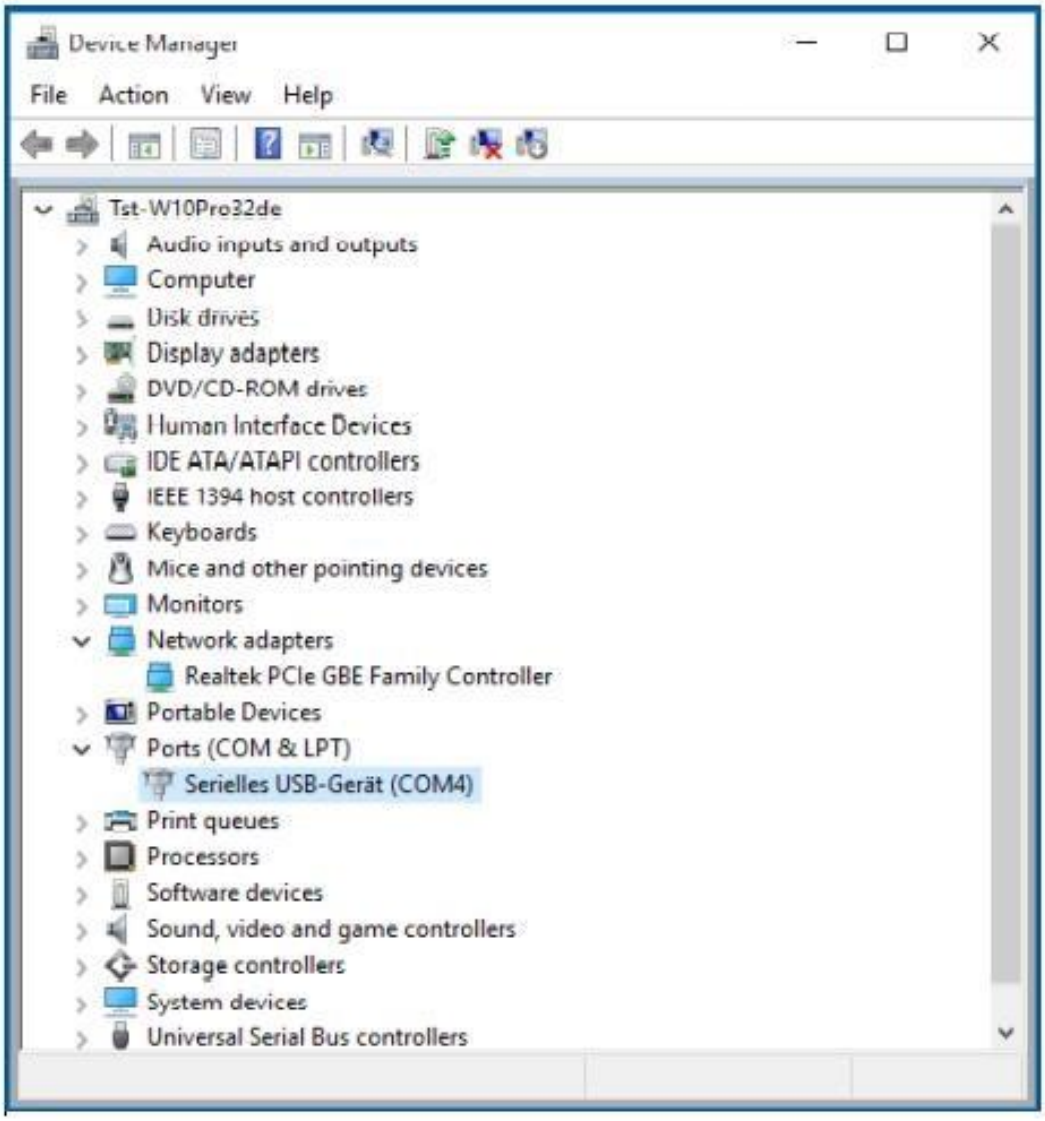


Figure 14: Update driver in Device Manager

C3.2 Update Driver Software

Right-click the Serial USB Device and select “Update Driver Software”. Select “Browse my computer for software”.

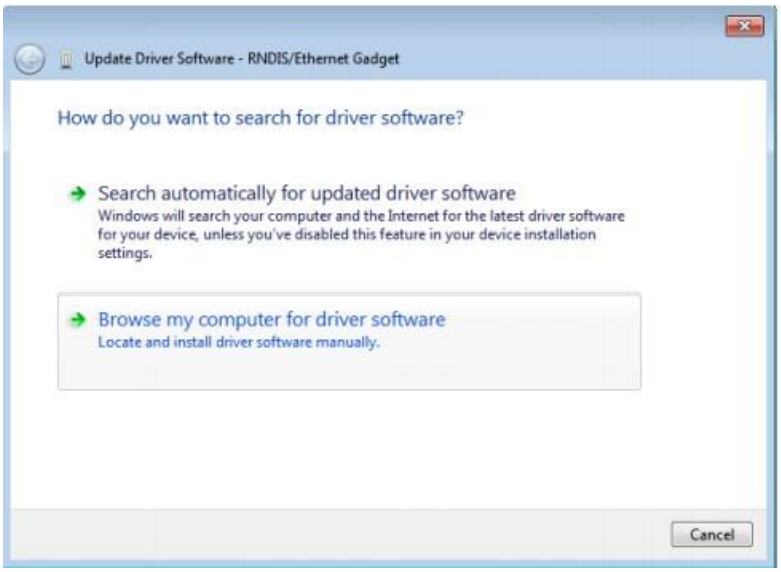


Figure 15: Select "Browse my computer for driver software"

Specify path to the proFPGA Windows drivers which came with the proFPGA software release and press 'Next':

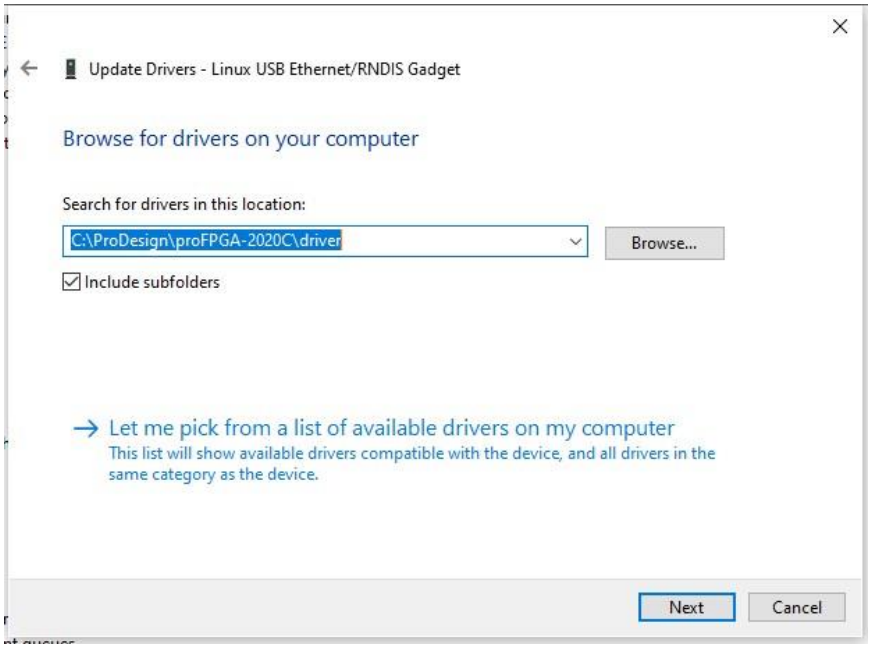


Figure 16: Specify path to the proFPGA

Allow installation of the driver. Press 'Install' to continue.

Figure 17: Allow installation

C4. Set Static IP Address for FPGA

To use a Static IP address, first set up your USB4CV System's IP address to Static IP Address.

1. Open **Control Panel** and select **Network and Sharing Center.**

Figure 18: Network and Sharing Center

2. Click on **Change Adapter Settings**

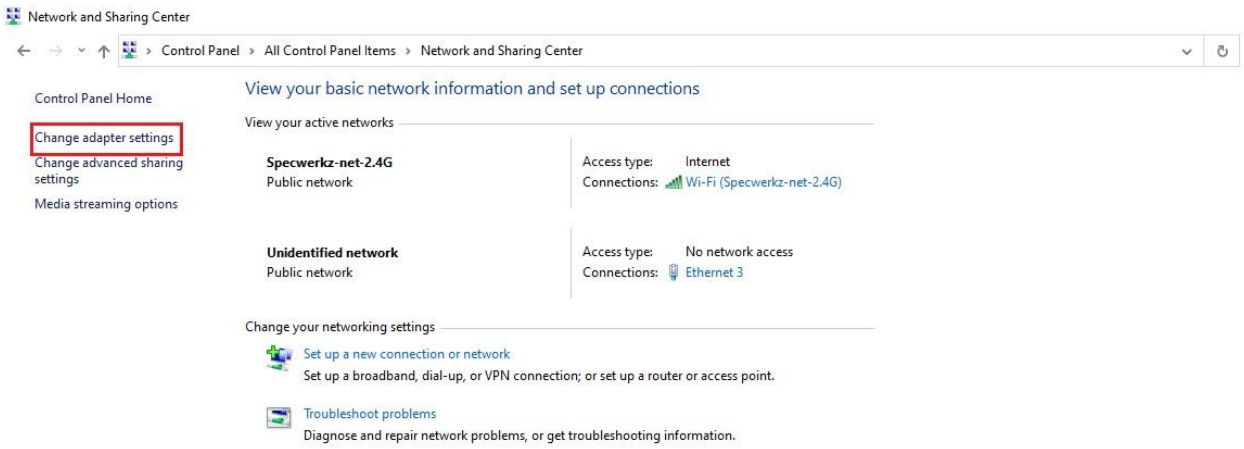


Figure 19: Change adapter setting

3. Click on “USB Ethernet/RNDIS Gadget”

Figure 20: USB Ethernet/RNDIS Gadget

4. Click on “Properties”.

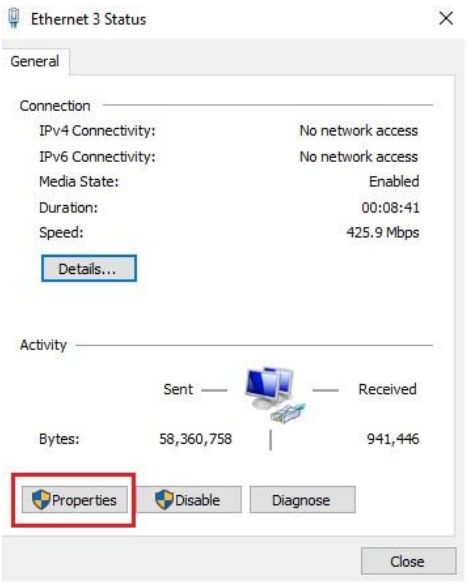


Figure 21: Choose "Properties"

5. Click on "**Internet Protocol Version 4 (TCP/IPv4)"** and open Properties.

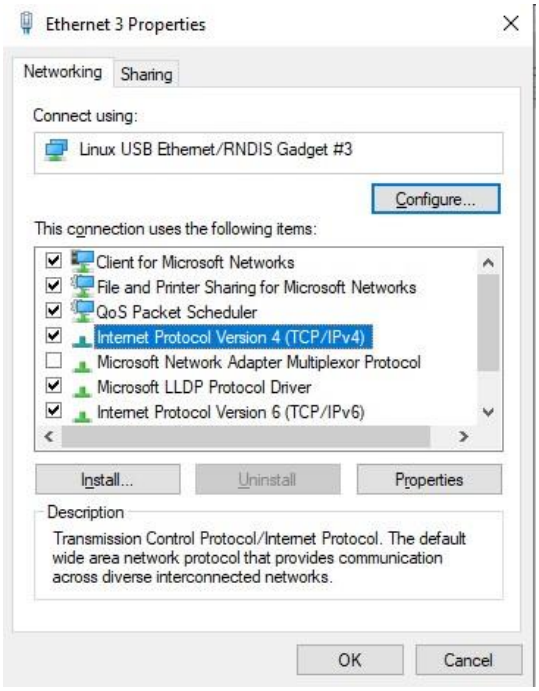


Figure 22: Internet Protocol Version 4 (TCP/IPv4)

6. Click on "**Use the following IP address**"

   In the IP address section type **169.254.0.1** (this is USB4CV System IP address)

In the subnet mask type **255.255.255.0**

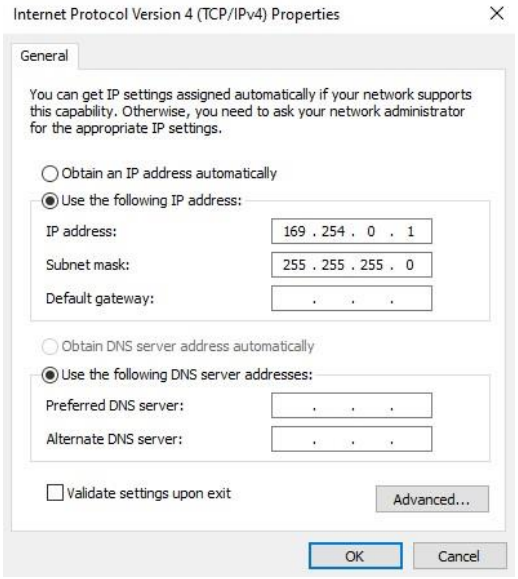


Figure 23: IP address and the subnet mask

7. Click "OK"

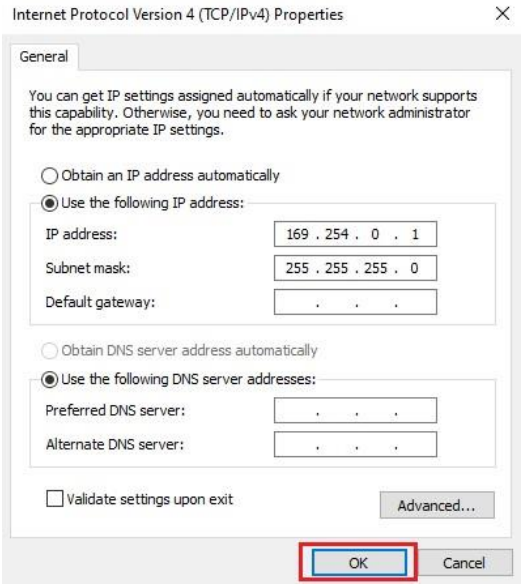


Figure 24: Click OK

Verify that FPGA connection to USB4CV System works

1. Open Command Prompt and enter **ping 169.254.0.2**

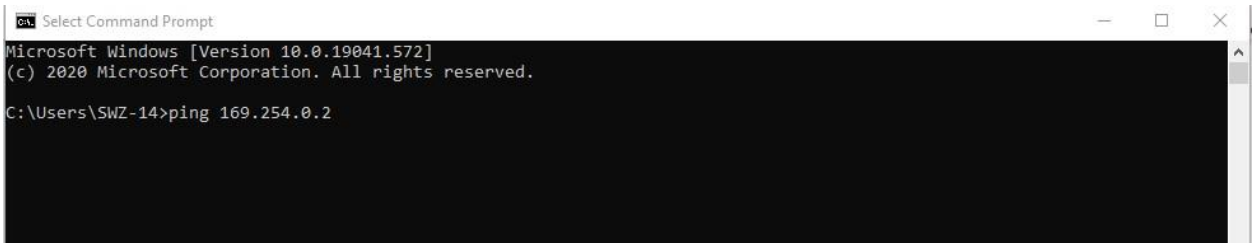


Figure 25: Ping proFPGA IP address

2. Make sure you received all packets

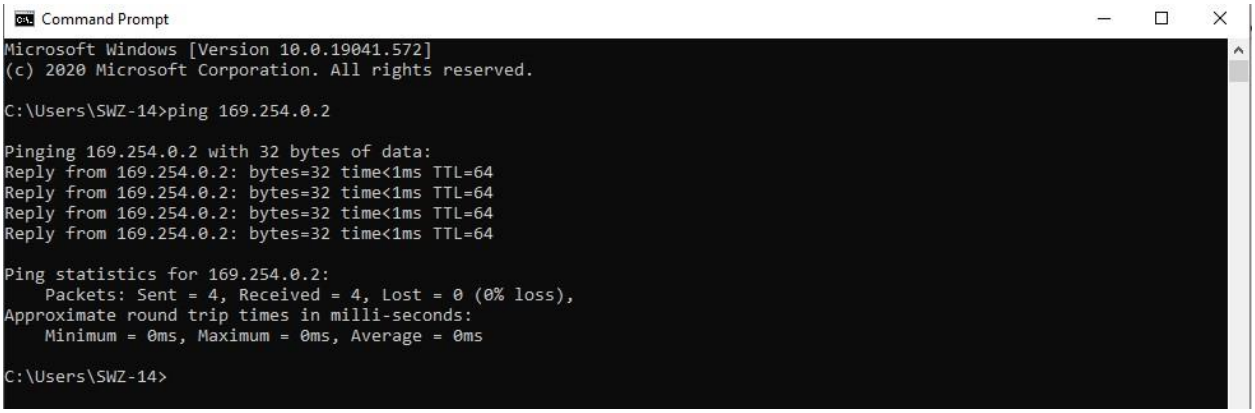


Figure 26: All packets received

D. Using proFPGA with USB4CV

With all files in the correct locations, all you need to do now is use the provided Windows Batch files to start up and shut down the FPGA. Every time the FPGA is powered on, you need to burn the bit file again using the provided startup batch file. Once you start up the FPGA, follow USB4 TMU CTS for connections to test setups.

A good indication for when the FPGA is ready to use is by looking for a line of LEDs next to the power switch on the Quad motherboard. When initially powering on the FPGA, only a few LEDs will be lit:

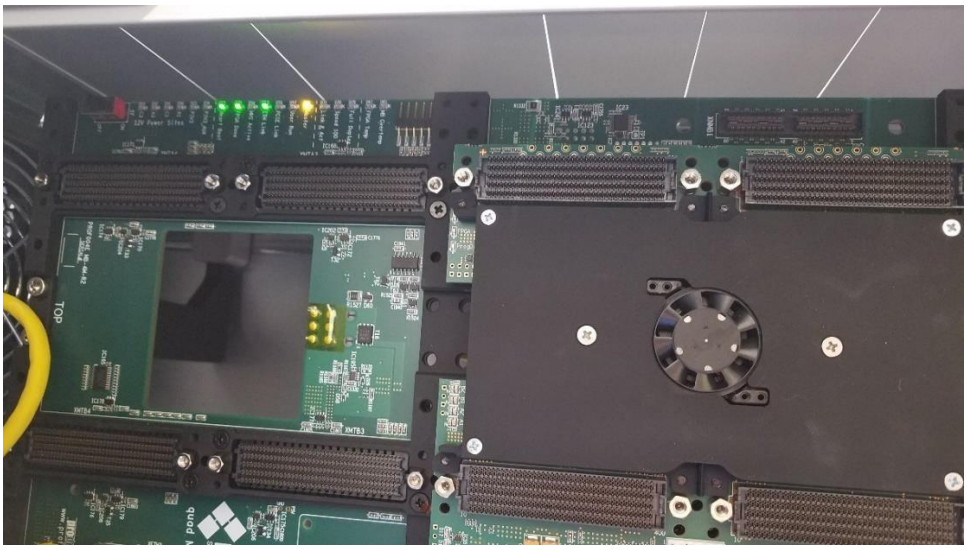


Figure 27: Top half of Quad motherboard

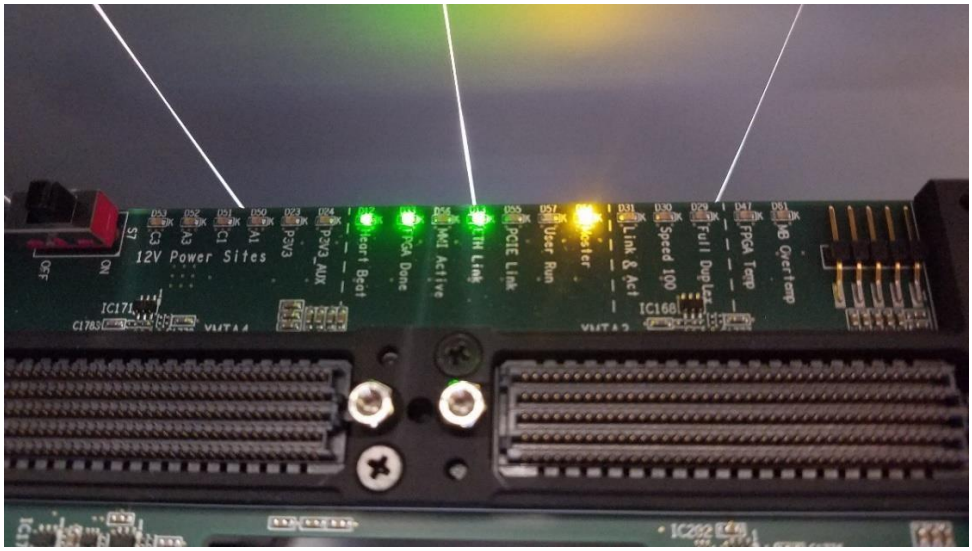


Figure 28: LEDs indicating bit file not burned

Once you've burned the bit file, you can see that many more LEDs are lit:

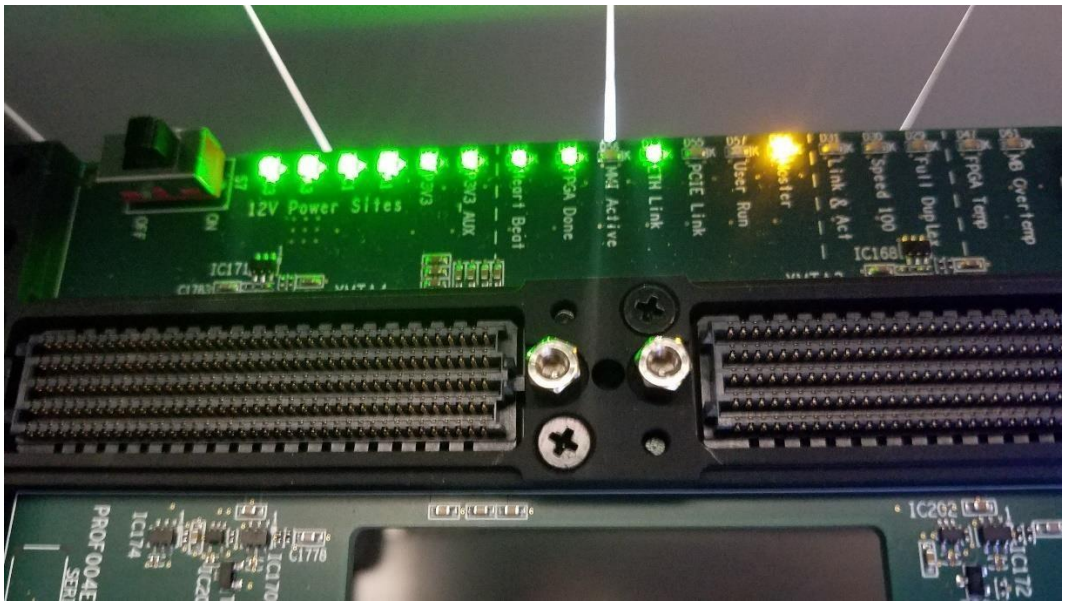
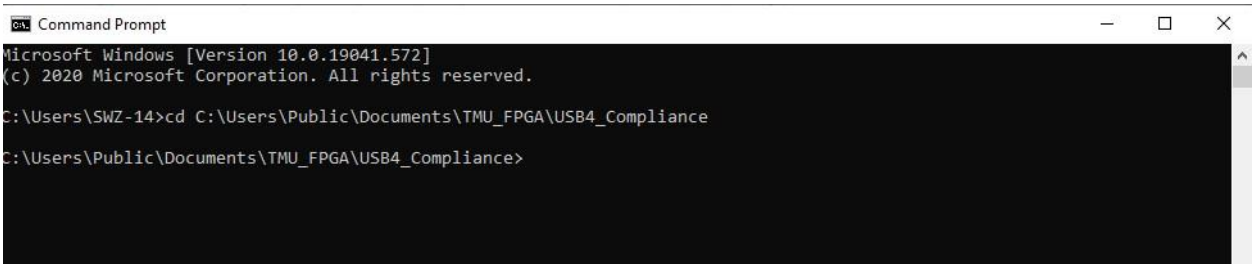


Figure 29: LEDs indicating bit file burned

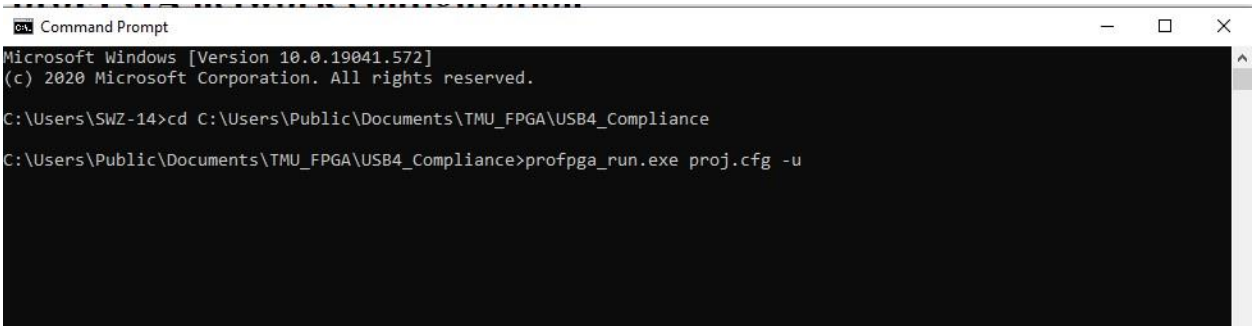
D1. Start up proFPGA (burning the bit file)

Every time the FPGA is powered up, it is necessary to burn the FPGA with the bit file. *fpga_start-up.bat* will do this by running the following commands:

a. **cd C:\Users\Public\Documents\TMU_FPGA\USB4_Compliance**



b. **profpga_run.exe proj.cfg -u**



c. Wait until loading .bit file is done

D2. Shut Down proFPGA

Please run the shutdown script and wait for proFPGA to fully shutdown before powering off the FPGA.

fpga_shutdown.bat will shut down the FPGA by running the following command:

profpga_selftest C:\Users\Public\Documents\TMU_FPGA\USB4_Compliance\proj.cfg -d

Wait until proFPGA finishes shutdown.

Troubleshooting:

If you are not able to turn on the FPGA with the batch files, please make sure that you followed the initial setup procedure correctly. Files need to be in a specific folder path and uses the specific IP address indicated in this procedure.

D3. LEDs for PA and PB

When connecting to test setups defined in TMU CTS, FPGA module has dedicated LEDs that will light up when it is getting TMU_CLK_OUT from a device that is connected to a host and has established a stable link.

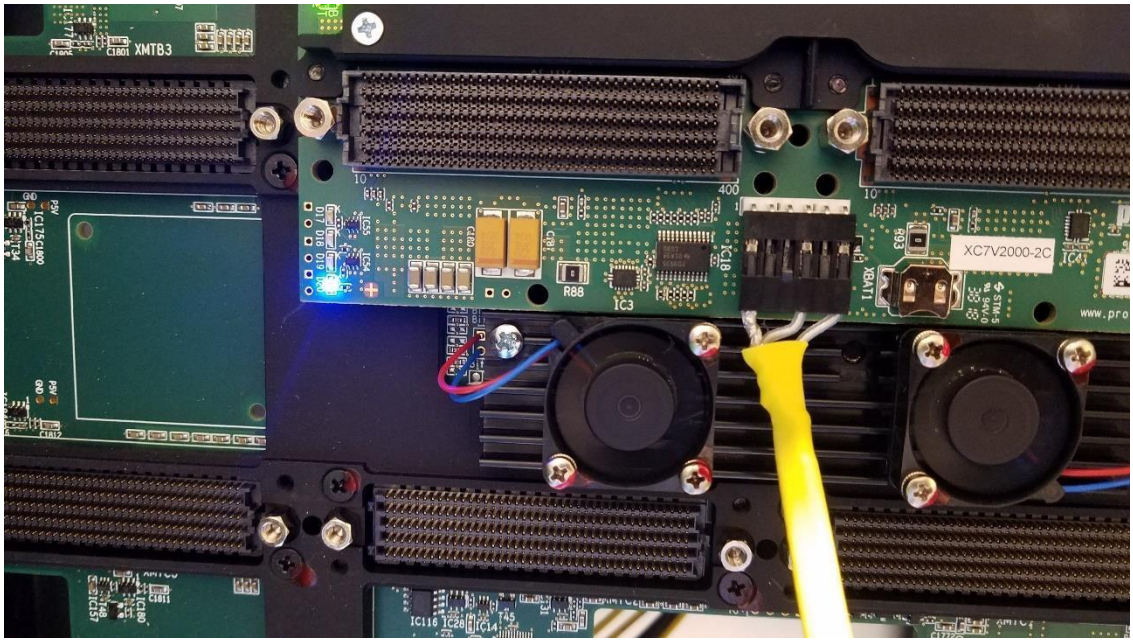


Figure 30: Blue LED lit for PA connection

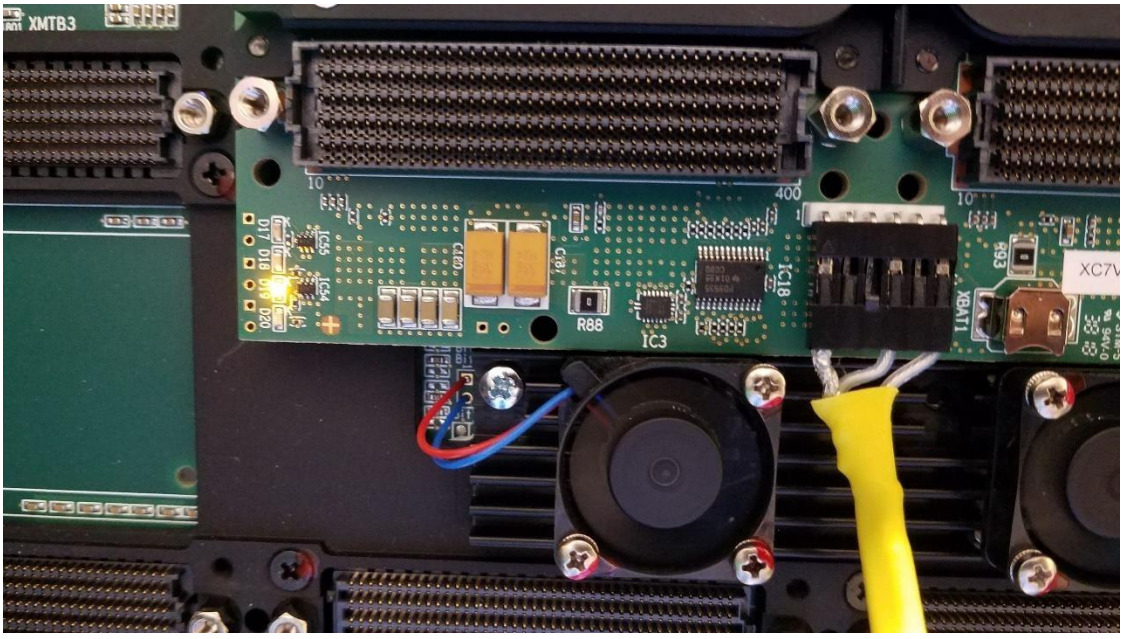


Figure 31: Orange LED lit for PB connection