



SPEC CPU®2017 Integer Rate Result

Copyright 2017-2021 Standard Performance Evaluation Corporation

Cisco Systems

SPECrate®2017_int_base = 222

Cisco UCS C225 M6 (AMD EPYC 7502P 32-Core)

SPECrate®2017_int_peak = 235

CPU2017 License: 9019

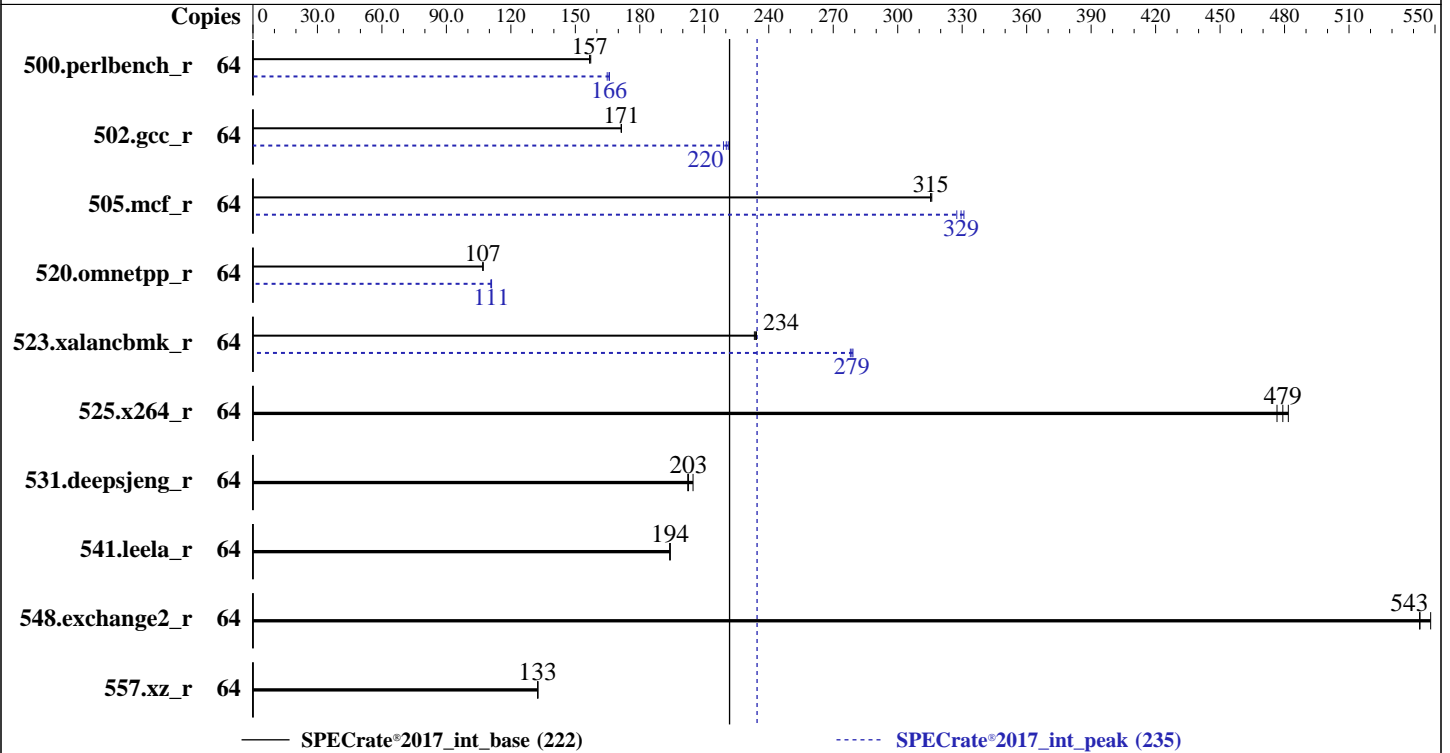
Test Date: Dec-2021

Test Sponsor: Cisco Systems

Hardware Availability: Jun-2021

Tested by: Cisco Systems

Software Availability: Jun-2021



Hardware

CPU Name: AMD EPYC 7502P
 Max MHz: 3350
 Nominal: 2500
 Enabled: 32 cores, 1 chip, 2 threads/core
 Orderable: 1 chips
 Cache L1: 32 KB I + 32 KB D on chip per core
 L2: 512 KB I+D on chip per core
 L3: 128 MB I+D on chip per chip,
 16 MB shared / 4 cores
 Other: None
 Memory: 1 TB (8 x 128 GB 4Rx4 PC4-3200V-L)
 Storage: 1 x 960 GB M.2 SSD SATA
 Other: None

Software

OS: SUSE Linux Enterprise Server 15 SP2 (x86_64)
 kernel version 5.3.18-22-default
 Compiler: C/C++/Fortran: Version 3.0.0 of AOCC
 Parallel: No
 Firmware: Version 4.2.1c released Aug-2021
 File System: xfs
 System State: Run level 3 (multi-user)
 Base Pointers: 64-bit
 Peak Pointers: 32/64-bit
 Other: jemalloc: jemalloc memory allocator library v5.1.0
 Power Management: BIOS and OS set to prefer performance at the cost of additional power usage



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Results Table

Benchmark	Base							Peak						
	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
500.perlbench_r	64	648	157	650	157	650	157	64	618	165	614	166	615	166
502.gcc_r	64	529	171	529	171	529	171	64	414	219	410	221	411	220
505.mcf_r	64	328	315	327	316	328	315	64	314	329	316	327	313	331
520.omnetpp_r	64	784	107	785	107	785	107	64	757	111	759	111	756	111
523.xalancbmk_r	64	290	233	288	234	289	234	64	243	279	243	278	242	279
525.x264_r	64	234	479	233	482	235	476	64	234	479	233	482	235	476
531.deepsjeng_r	64	362	203	358	205	363	202	64	362	203	358	205	363	202
541.leela_r	64	546	194	546	194	547	194	64	546	194	546	194	547	194
548.exchange2_r	64	309	543	306	548	309	543	64	309	543	306	548	309	543
557.xz_r	64	522	133	521	133	522	132	64	522	133	521	133	522	132

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Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Compiler Notes

The AMD64 AOCC Compiler Suite is available at <http://developer.amd.com/amd-aocc/>

Submit Notes

The config file option 'submit' was used.
'numactl' was used to bind copies to the cores.
See the configuration file for details.

Operating System Notes

'ulimit -s unlimited' was used to set environment stack size limit
'ulimit -l 2097152' was used to set environment locked pages in memory limit

runcpu command invoked through numactl i.e.:
numactl --interleave=all runcpu <etc>

To limit dirty cache to 8% of memory, 'sysctl -w vm.dirty_ratio=8' run as root.
To limit swap usage to minimum necessary, 'sysctl -w vm.swappiness=1' run as root.
To free node-local memory and avoid remote memory usage,
'sysctl -w vm.zone_reclaim_mode=1' run as root.
To clear filesystem caches, 'sync; sysctl -w vm.drop_caches=3' run as root.
To disable address space layout randomization (ASLR) to reduce run-to-run
variability, 'sysctl -w kernel.randomize_va_space=0' run as root.

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Operating System Notes (Continued)

To enable Transparent Hugepages (THP) only on request for base runs,
'echo madvise > /sys/kernel/mm/transparent_hugepage/enabled' run as root.
To enable THP for all allocations for peak runs,
'echo always > /sys/kernel/mm/transparent_hugepage/enabled' and
'echo always > /sys/kernel/mm/transparent_hugepage/defrag' run as root.

Environment Variables Notes

Environment variables set by runcpu before the start of the run:

```
LD_LIBRARY_PATH =  
    "/home/cpu2017/amd_rate_aocc300_milan_B_lib/lib;/home/cpu2017/amd_rate_a  
    occ300_milan_B_lib/lib32:"  
MALLOC_CONF = "retain:true"
```

Environment variables set by runcpu during the 523.xalancbmk_r peak run:

```
MALLOC_CONF = "thp:never"
```

General Notes

Binaries were compiled on a system with 2x AMD EPYC 7742 CPU + 1TiB Memory using OpenSUSE 15.2

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

jemalloc: configured and built with GCC v4.8.2 in RHEL 7.4 (No options specified)

jemalloc 5.1.0 is available here:

<https://github.com/jemalloc/jemalloc/releases/download/5.1.0/jemalloc-5.1.0.tar.bz2>

Platform Notes

BIOS Configuration

SMT Mode set to Auto

NUMA nodes per socket set to NPS4

ACPI SRAT L3 Cache As NUMA Domain set to Enabled

DRAM Scrub Time set to Disabled

Determinism Slider set to Power

Memory Interleaving set to Auto

APBDIS set to 1

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Software Availability: Jun-2021

Platform Notes (Continued)

sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6622 of 2021-04-07 982a61ec0915b55891ef0e16acafc64d
running on localhost Fri Dec 3 16:21:35 2021

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
<https://www.spec.org/cpu2017/Docs/config.html#sysinfo>

From /proc/cpuinfo

```
model name : AMD EPYC 7502P 32-Core Processor
 1 "physical id"s (chips)
 64 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following
excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 32
siblings : 64
physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24
25 26 27 28 29 30 31
```

From lscpu from util-linux 2.33.1:

```
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
Address sizes: 43 bits physical, 48 bits virtual
CPU(s): 64
On-line CPU(s) list: 0-63
Thread(s) per core: 2
Core(s) per socket: 32
Socket(s): 1
NUMA node(s): 8
Vendor ID: AuthenticAMD
CPU family: 23
Model: 49
Model name: AMD EPYC 7502P 32-Core Processor
Stepping: 0
CPU MHz: 1433.010
CPU max MHz: 2500.0000
CPU min MHz: 1500.0000
BogoMIPS: 4990.93
Virtualization: AMD-V
L1d cache: 32K
L1i cache: 32K
L2 cache: 512K
L3 cache: 16384K
NUMA node0 CPU(s): 0-3,32-35
NUMA node1 CPU(s): 4-7,36-39
```

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Platform Notes (Continued)

```

NUMA node2 CPU(s): 8-11,40-43
NUMA node3 CPU(s): 12-15,44-47
NUMA node4 CPU(s): 16-19,48-51
NUMA node5 CPU(s): 20-23,52-55
NUMA node6 CPU(s): 24-27,56-59
NUMA node7 CPU(s): 28-31,60-63
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush mmx fxsr sse sse2 ht syscall nx mmxext fxsr_opt pdpe1gb rdtscp lm
constant_tsc rep_good nopl nonstop_tsc cpuid extd_apicid aperfmperf pni pclmulqdq
monitor ssse3 fma cx16 sse4_1 sse4_2 movbe popcnt aes xsave avx f16c rdrand lahf_lm
cmp_legacy svm extapic cr8_legacy abm sse4a misalignsse 3dnowprefetch osvw ibs
skinit wdt tce topoext perfctr_core perfctr_nb bpext perfctr_llc mwaitx cpb cat_l3
cdp_l3 hw_pstate sme ssbd mba sev ibrs ibpb stibp vmmcall fsgsbase bmi1 avx2 smep
bmi2 cqm rdt_a rdseed adx smap clflushopt clwb sha_ni xsaveopt xsavec xgetbv1 xsaves
cqm_llc cqm_occup_llc cqm_mbm_total cqm_mbm_local clzero irperf xsaveerptr wbnoinvd
arat npt lbrv svm_lock nrip_save tsc_scale vmcb_clean flushbyasid decodeassists
pausefilter pfthreshold avic v_vmsave_vmload vgif umip rdpid overflow_recov succor
smca

```

```

/proc/cpuinfo cache data
cache size : 512 KB

```

```

From numactl --hardware
WARNING: a numactl 'node' might or might not correspond to a physical chip.
available: 8 nodes (0-7)
node 0 cpus: 0 1 2 3 32 33 34 35
node 0 size: 128839 MB
node 0 free: 128610 MB
node 1 cpus: 4 5 6 7 36 37 38 39
node 1 size: 129020 MB
node 1 free: 128750 MB
node 2 cpus: 8 9 10 11 40 41 42 43
node 2 size: 129021 MB
node 2 free: 128793 MB
node 3 cpus: 12 13 14 15 44 45 46 47
node 3 size: 129020 MB
node 3 free: 128837 MB
node 4 cpus: 16 17 18 19 48 49 50 51
node 4 size: 129021 MB
node 4 free: 128864 MB
node 5 cpus: 20 21 22 23 52 53 54 55
node 5 size: 129020 MB
node 5 free: 128837 MB
node 6 cpus: 24 25 26 27 56 57 58 59
node 6 size: 129021 MB
node 6 free: 128870 MB
node 7 cpus: 28 29 30 31 60 61 62 63

```

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Platform Notes (Continued)

```
node 7 size: 128974 MB
node 7 free: 128823 MB
node distances:
node  0  1  2  3  4  5  6  7
  0:  10 11 12 12 12 12 12 12
  1:  11 10 12 12 12 12 12 12
  2:  12 12 10 11 12 12 12 12
  3:  12 12 11 10 12 12 12 12
  4:  12 12 12 12 10 11 12 12
  5:  12 12 12 12 11 10 12 12
  6:  12 12 12 12 12 12 10 11
  7:  12 12 12 12 12 12 11 10
```

```
From /proc/meminfo
MemTotal:      1056708144 kB
HugePages_Total:      0
Hugepagesize:    2048 kB
```

```
/sys/devices/system/cpu/cpu*/cpufreq/scaling_governor has
ondemand
```

```
From /etc/*release* /etc/*version*
os-release:
NAME="SLES"
VERSION="15-SP2"
VERSION_ID="15.2"
PRETTY_NAME="SUSE Linux Enterprise Server 15 SP2"
ID="sles"
ID_LIKE="suse"
ANSI_COLOR="0;32"
CPE_NAME="/o:suse:sles:15:sp2"
```

```
uname -a:
Linux localhost 5.3.18-22-default #1 SMP Wed Jun 3 12:16:43 UTC 2020 (720aeba) x86_64
x86_64 x86_64 GNU/Linux
```

Kernel self-reported vulnerability status:

```
CVE-2018-12207 (iTLB Multihit):          Not affected
CVE-2018-3620 (L1 Terminal Fault):      Not affected
Microarchitectural Data Sampling:      Not affected
CVE-2017-5754 (Meltdown):              Not affected
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store
Bypass disabled via prctl and
seccomp
CVE-2017-5753 (Spectre variant 1):      Mitigation: usercopy/swapgs
barriers and __user pointer
```

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Platform Notes (Continued)

CVE-2017-5715 (Spectre variant 2): sanitization
 Mitigation: Full AMD retpoline,
 IBPB: conditional, IBRS_FW, STIBP:
 conditional, RSB filling

CVE-2020-0543 (Special Register Buffer Data Sampling): Not affected

CVE-2019-11135 (TSX Asynchronous Abort): Not affected

run-level 3 Dec 3 16:21

SPEC is set to: /home/cpu2017

Filesystem	Type	Size	Used	Avail	Use%	Mounted on
/dev/sdb2	xfs	223G	6.9G	217G	4%	/

From /sys/devices/virtual/dmi/id

Vendor: Cisco Systems Inc
 Product: UCSC-C225-M6S
 Serial: WZP252408JE

Additional information from dmidecode 3.2 follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

Memory:

8x 0xCE00 M386AAG40AM3-CWE 128 GB 4 rank 3200
 24x Unknown Unknown

BIOS:

BIOS Vendor: Cisco Systems Inc
 BIOS Version: C225M6.4.2.1c.0.0806211349
 BIOS Date: 08/06/2021
 BIOS Revision: 5.14

(End of data from sysinfo program)

Compiler Version Notes

```
=====
C | 502.gcc_r(peak)
=====
```

```
AMD clang version 12.0.0 (CLANG: AOCC_3.0.0-Build#78 2020_12_10) (based on
LLVM Mirror.Version.12.0.0)
Target: i386-unknown-linux-gnu
Thread model: posix
InstalledDir: /opt/AMD/aocc-compiler-3.0.0/bin
=====
```

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Compiler Version Notes (Continued)

```
=====
C          | 500.perlbench_r(base, peak) 502.gcc_r(base) 505.mcf_r(base, peak)
          | 525.x264_r(base, peak) 557.xz_r(base, peak)
-----
```

```
AMD clang version 12.0.0 (CLANG: AOCC_3.0.0-Build#78 2020_12_10) (based on
LLVM Mirror.Version.12.0.0)
Target: x86_64-unknown-linux-gnu
Thread model: posix
InstalledDir: /opt/AMD/aocc-compiler-3.0.0/bin
-----
```

```
=====
C          | 502.gcc_r(peak)
-----
```

```
AMD clang version 12.0.0 (CLANG: AOCC_3.0.0-Build#78 2020_12_10) (based on
LLVM Mirror.Version.12.0.0)
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```

```
=====
C          | 500.perlbench_r(base, peak) 502.gcc_r(base) 505.mcf_r(base, peak)
          | 525.x264_r(base, peak) 557.xz_r(base, peak)
-----
```

```
AMD clang version 12.0.0 (CLANG: AOCC_3.0.0-Build#78 2020_12_10) (based on
LLVM Mirror.Version.12.0.0)
Target: x86_64-unknown-linux-gnu
Thread model: posix
InstalledDir: /opt/AMD/aocc-compiler-3.0.0/bin
-----
```

```
=====
C++       | 523.xalanbmk_r(peak)
-----
```

```
AMD clang version 12.0.0 (CLANG: AOCC_3.0.0-Build#78 2020_12_10) (based on
LLVM Mirror.Version.12.0.0)
Target: i386-unknown-linux-gnu
Thread model: posix
InstalledDir: /opt/AMD/aocc-compiler-3.0.0/bin
-----
```

```
=====
C++       | 520.omnetpp_r(base, peak) 523.xalanbmk_r(base)
          | 531.deepsjeng_r(base, peak) 541.leela_r(base, peak)
-----
```

```
AMD clang version 12.0.0 (CLANG: AOCC_3.0.0-Build#78 2020_12_10) (based on
```

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Compiler Version Notes (Continued)

```

LLVM Mirror.Version.12.0.0)
Target: x86_64-unknown-linux-gnu
Thread model: posix
InstalledDir: /opt/AMD/aocc-compiler-3.0.0/bin
-----

```

```

=====
C++      | 523.xalancbmk_r(peak)
-----

```

```

AMD clang version 12.0.0 (CLANG: AOCC_3.0.0-Build#78 2020_12_10) (based on
LLVM Mirror.Version.12.0.0)
Target: i386-unknown-linux-gnu
Thread model: posix
InstalledDir: /opt/AMD/aocc-compiler-3.0.0/bin
-----

```

```

=====
C++      | 520.omnetpp_r(base, peak) 523.xalancbmk_r(base)
          | 531.deepsjeng_r(base, peak) 541.leela_r(base, peak)
-----

```

```

AMD clang version 12.0.0 (CLANG: AOCC_3.0.0-Build#78 2020_12_10) (based on
LLVM Mirror.Version.12.0.0)
Target: x86_64-unknown-linux-gnu
Thread model: posix
InstalledDir: /opt/AMD/aocc-compiler-3.0.0/bin
-----

```

```

=====
Fortran  | 548.exchange2_r(base, peak)
-----

```

```

AMD clang version 12.0.0 (CLANG: AOCC_3.0.0-Build#78 2020_12_10) (based on
LLVM Mirror.Version.12.0.0)
Target: x86_64-unknown-linux-gnu
Thread model: posix
InstalledDir: /opt/AMD/aocc-compiler-3.0.0/bin
-----

```

Base Compiler Invocation

C benchmarks:
clang

C++ benchmarks:
clang++

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Base Compiler Invocation (Continued)

Fortran benchmarks:

flang

Base Portability Flags

```
500.perlbench_r: -DSPEC_LINUX_X64 -DSPEC_LP64
502.gcc_r: -DSPEC_LP64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -DSPEC_LINUX -DSPEC_LP64
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64
```

Base Optimization Flags

C benchmarks:

```
-m64 -Wl,-allow-multiple-definition -Wl,-mllvm -Wl,-enable-licm-vrp
-flto -Wl,-mllvm -Wl,-region-vectorize
-Wl,-mllvm -Wl,-function-specialize
-Wl,-mllvm -Wl,-align-all-nofallthru-blocks=6
-Wl,-mllvm -Wl,-reduce-array-computations=3 -O3 -ffast-math
-march=znver3 -fveclib=AMDLIBM -fstruct-layout=5
-mllvm -unroll-threshold=50 -mllvm -inline-threshold=1000
-freemap-arrays -mllvm -function-specialize -flv-function-specialization
-mllvm -enable-gvn-hoist -mllvm -global-vectorize-slp=true
-mllvm -enable-licm-vrp -mllvm -reduce-array-computations=3 -z muldefs
-lamdlibm -ljemalloc -lflang -lflangrti
```

C++ benchmarks:

```
-m64 -std=c++98 -Wl,-mllvm -Wl,-do-block-reorder=aggressive -flto
-Wl,-mllvm -Wl,-region-vectorize -Wl,-mllvm -Wl,-function-specialize
-Wl,-mllvm -Wl,-align-all-nofallthru-blocks=6
-Wl,-mllvm -Wl,-reduce-array-computations=3 -O3 -ffast-math
-march=znver3 -fveclib=AMDLIBM -mllvm -enable-partial-unswitch
-mllvm -unroll-threshold=100 -finline-aggressive
-flv-function-specialization -mllvm -loop-unswitch-threshold=200000
-mllvm -reroll-loops -mllvm -aggressive-loop-unswitch
-mllvm -extra-vectorizer-passes -mllvm -reduce-array-computations=3
-mllvm -global-vectorize-slp=true -mllvm -convert-pow-exp-to-int=false
```

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Base Optimization Flags (Continued)

C++ benchmarks (continued):

-z muldefs -mllvm -do-block-reorder=aggressive
-fvirtual-function-elimination -fvisibility=hidden -lamdlibm
-ljemalloc -lflang -lflangrti

Fortran benchmarks:

-m64 -Wl,-mllvm -Wl,-inline-recursion=4
-Wl,-mllvm -Wl,-lsr-in-nested-loop -Wl,-mllvm -Wl,-enable-iv-split
-flto -Wl,-mllvm -Wl,-region-vectorize
-Wl,-mllvm -Wl,-function-specialize
-Wl,-mllvm -Wl,-align-all-nofallthru-blocks=6
-Wl,-mllvm -Wl,-reduce-array-computations=3 -O3 -ffast-math
-march=znver3 -fveclib=AMDLIBM -z muldefs -mllvm -unroll-aggressive
-mllvm -unroll-threshold=500 -lamdlibm -ljemalloc -lflang -lflangrti

Base Other Flags

C benchmarks:

-Wno-unused-command-line-argument

C++ benchmarks:

-Wno-unused-command-line-argument

Peak Compiler Invocation

C benchmarks:

clang

C++ benchmarks:

clang++

Fortran benchmarks:

flang

Peak Portability Flags

500.perlbench_r: -DSPEC_LINUX_X64 -DSPEC_LP64

502.gcc_r: -D_FILE_OFFSET_BITS=64

505.mcf_r: -DSPEC_LP64

(Continued on next page)



SPEC CPU®2017 Integer Rate Result

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Cisco Systems

SPECrate®2017_int_base = 222

Cisco UCS C225 M6 (AMD EPYC 7502P 32-Core)

SPECrate®2017_int_peak = 235

CPU2017 License: 9019

Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Dec-2021

Hardware Availability: Jun-2021

Software Availability: Jun-2021

Peak Portability Flags (Continued)

```

520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -DSPEC_LINUX -DSPEC_LP64
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64

```

Peak Optimization Flags

C benchmarks:

```

500.perlbench_r: -m64 -Wl,-allow-multiple-definition
-Wl,-mllvm -Wl,-enable-licm-vrp -flto
-Wl,-mllvm -Wl,-function-specialize
-Wl,-mllvm -Wl,-align-all-nofallthru-blocks=6
-Wl,-mllvm -Wl,-reduce-array-computations=3
-fprofile-instr-generate(pass 1)
-fprofile-instr-use(pass 2) -Ofast -march=znver3
-fveclib=AMDLIBM -fstruct-layout=7
-mllvm -unroll-threshold=50 -fremap-arrays
-flv-function-specialization -mllvm -inline-threshold=1000
-mllvm -enable-gvn-hoist -mllvm -global-vectorize-slp=false
-mllvm -function-specialize -mllvm -enable-licm-vrp
-mllvm -reduce-array-computations=3 -lamdlibm -ljemalloc

502.gcc_r: -m32 -Wl,-allow-multiple-definition
-Wl,-mllvm -Wl,-enable-licm-vrp -flto
-Wl,-mllvm -Wl,-function-specialize -Ofast -march=znver3
-fveclib=AMDLIBM -fstruct-layout=7
-mllvm -unroll-threshold=50 -fremap-arrays
-flv-function-specialization -mllvm -inline-threshold=1000
-mllvm -enable-gvn-hoist -mllvm -global-vectorize-slp=true
-mllvm -function-specialize -mllvm -enable-licm-vrp
-mllvm -reduce-array-computations=3 -fgnu89-inline
-ljemalloc

505.mcf_r: -m64 -Wl,-allow-multiple-definition
-Wl,-mllvm -Wl,-enable-licm-vrp -flto
-Wl,-mllvm -Wl,-function-specialize
-Wl,-mllvm -Wl,-align-all-nofallthru-blocks=6
-Wl,-mllvm -Wl,-reduce-array-computations=3 -Ofast
-march=znver3 -fveclib=AMDLIBM -fstruct-layout=7
-mllvm -unroll-threshold=50 -fremap-arrays

```

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Software Availability: Jun-2021

Peak Optimization Flags (Continued)

505.mcf_r (continued):

```
-flv-function-specialization -mllvm -inline-threshold=1000  
-mllvm -enable-gvn-hoist -mllvm -global-vectorize-slp=true  
-mllvm -function-specialize -mllvm -enable-licm-vrp  
-mllvm -reduce-array-computations=3 -lamdlibm -ljemalloc
```

525.x264_r: basepeak = yes

557.xz_r: basepeak = yes

C++ benchmarks:

520.omnetpp_r: -m64 -std=c++98

```
-Wl,-mllvm -Wl,-do-block-reorder=aggressive -flto  
-Wl,-mllvm -Wl,-function-specialize  
-Wl,-mllvm -Wl,-align-all-nofallthru-blocks=6  
-Wl,-mllvm -Wl,-reduce-array-computations=3 -Ofast  
-march=znver3 -fveclib=AMDLIBM -finline-aggressive  
-mllvm -unroll-threshold=100 -flv-function-specialization  
-mllvm -enable-licm-vrp -mllvm -reroll-loops  
-mllvm -aggressive-loop-unswitch  
-mllvm -reduce-array-computations=3  
-mllvm -global-vectorize-slp=true  
-mllvm -do-block-reorder=aggressive  
-fvirtual-function-elimination -fvisibility=hidden  
-lamdlibm -ljemalloc
```

523.xalancbmk_r: -m32 -Wl,-mllvm -Wl,-do-block-reorder=aggressive -flto

```
-Wl,-mllvm -Wl,-function-specialize  
-Wl,-mllvm -Wl,-align-all-nofallthru-blocks=6  
-Wl,-mllvm -Wl,-reduce-array-computations=3 -Ofast  
-march=znver3 -fveclib=AMDLIBM -finline-aggressive  
-mllvm -unroll-threshold=100 -flv-function-specialization  
-mllvm -enable-licm-vrp -mllvm -reroll-loops  
-mllvm -aggressive-loop-unswitch  
-mllvm -reduce-array-computations=3  
-mllvm -global-vectorize-slp=true  
-mllvm -do-block-reorder=aggressive  
-fvirtual-function-elimination -fvisibility=hidden  
-ljemalloc
```

531.deepsjeng_r: basepeak = yes

541.leela_r: basepeak = yes

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Peak Optimization Flags (Continued)

Fortran benchmarks:

548.exchange2_r: basepeak = yes

Peak Other Flags

C benchmarks (except as noted below):

-Wno-unused-command-line-argument

502.gcc_r: -L/usr/lib -Wno-unused-command-line-argument

-L/sppo/bin/cpu2017v115aocc3/amd_rate_aocc300_milan_A_lib/32

C++ benchmarks (except as noted below):

-Wno-unused-command-line-argument

523.xalancbmk_r: -L/usr/lib -Wno-unused-command-line-argument

-L/sppo/bin/cpu2017v115aocc3/amd_rate_aocc300_milan_A_lib/32

The flags files that were used to format this result can be browsed at

<http://www.spec.org/cpu2017/flags/aocc300-flags-B2.html>

<http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-AMD-v2-revC.html>

You can also download the XML flags sources by saving the following links:

<http://www.spec.org/cpu2017/flags/aocc300-flags-B2.xml>

<http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-AMD-v2-revC.xml>

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