SPEC CPU®2017 Integer Rate Result

Copyright 2017-2021 Standard Performance Evaluation Corporation

Supermicro
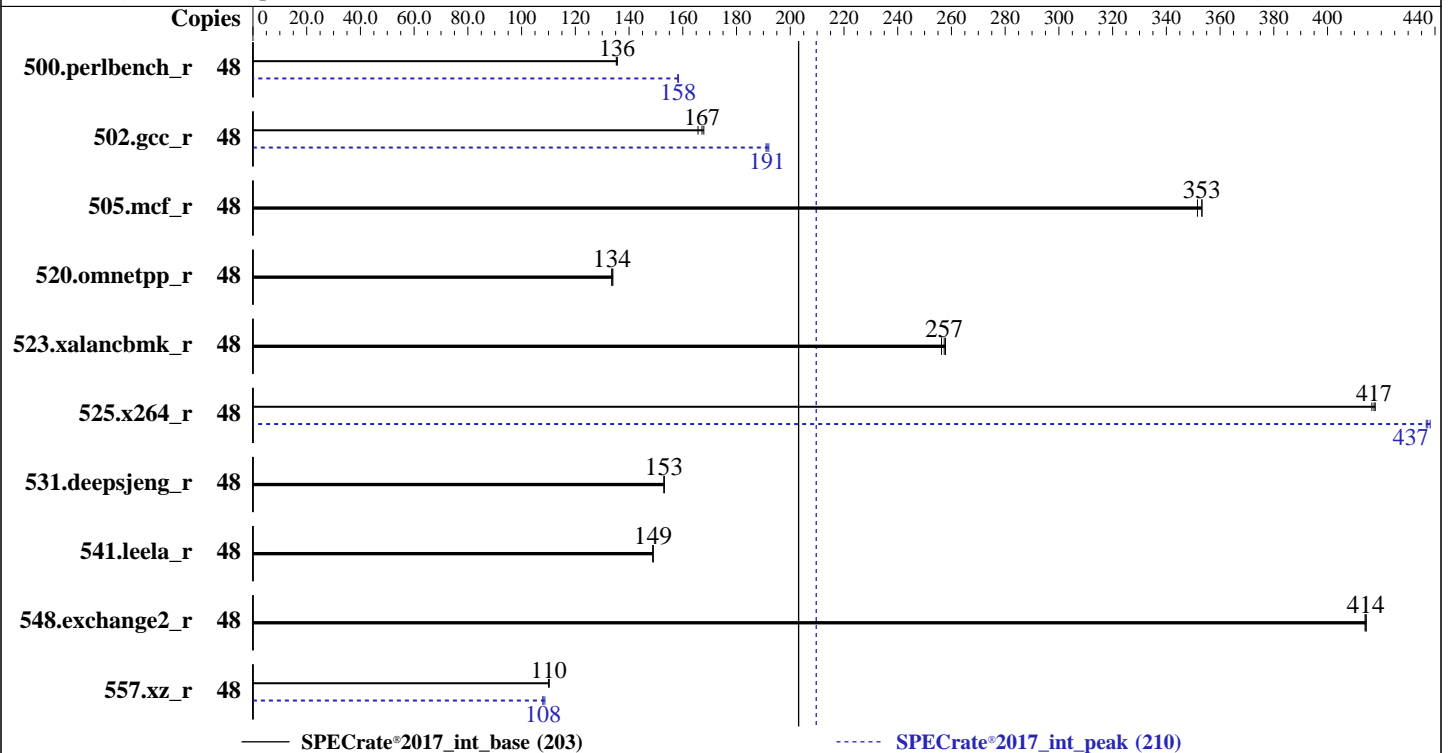
SuperServer SYS-620U-TNR
(X12DPU-6 , Intel Xeon Gold 5317)

$SPECrate^{®}2017\_int\_base = 203$

$SPECrate^{®}2017\_int\_peak = 210$

CPU2017 License: 001176
Test Sponsor: Supermicro
Tested by: Supermicro

Test Date: Nov-2021
Hardware Availability: Apr-2021
Software Availability: Jun-2021

Copies	0 20.0 40.0 60.0 80.0 100 120 140 160 180 200 220 240 260 280 300 320 340 360 380 400 440
500.perlbench_r 48	136 / 158
502.gcc_r 48	167 / 191
505.mcf_r 48	353
520.omnetpp_r 48	134
523.xalancbmk_r 48	257
525.x264_r 48	417 / 437
531.deepsjeng_r 48	153
541.leela_r 48	149
548.exchange2_r 48	414
557.xz_r 48	110 / 108

——— **SPECrate®2017_int_base (203)** - - - - **SPECrate®2017_int_peak (210)**

Hardware

CPU Name: Intel Xeon Gold 5317
 Max MHz: 3600
 Nominal: 3000
Enabled: 24 cores, 2 chips, 2 threads/core
Orderable: 1,2 Chips
Cache L1: 32 KB I + 48 KB D on chip per core
 L2: 1.25 MB I+D on chip per core
 L3: 18 MB I+D on chip per chip
 Other: None
Memory: 512 GB
 (16 x 32 GB 2Rx4 PC4-3200AA-R, running at 2933)
Storage: 1 x 1 TB NVMe SSD
Other: None

Software

OS: SUSE Linux Enterprise Server 15 SP3
 5.3.18-57-default
Compiler: C/C++: Version 2021.1 of Intel oneAPI DPC++/C++
 Compiler Build 20201113 for Linux;
 Fortran: Version 2021.1 of Intel Fortran Compiler
 Classic Build 20201112 for Linux;
 C/C++: Version 2021.1 of Intel C/C++ Compiler
 Classic Build 20201112 for Linux
Parallel: No
Firmware: Version 1.1 released Apr-2021
File System: xfs
System State: Run level 3 (multi-user)
Base Pointers: 64-bit
Peak Pointers: 32/64-bit
Other: jemalloc memory allocator V5.0.1
Power Management: BIOS and OS set to prefer performance at
 the cost of additional power usage.

SPEC CPU®2017 Integer Rate Result

Copyright 2017-2021 Standard Performance Evaluation Corporation

Supermicro

SuperServer SYS-620U-TNR
(X12DPU-6 , Intel Xeon Gold 5317)

$SPECrate®2017\_int\_base = 203$

$SPECrate®2017\_int\_peak = 210$

CPU2017 License: 001176	**Test Date:** Nov-2021
Test Sponsor: Supermicro	**Hardware Availability:** Apr-2021
Tested by: Supermicro	**Software Availability:** Jun-2021

Results Table

Benchmark	Base						Peak					
	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
500.perlbench_r	48	565	135	564	136	**564**	**136**	48	**483**	**158**	483	158	483	158
502.gcc_r	48	**407**	**167**	410	166	405	168	48	356	191	354	192	**355**	**191**
505.mcf_r	48	220	353	**220**	**353**	221	352	48	220	353	**220**	**353**	221	352
520.omnetpp_r	48	472	134	**471**	**134**	470	134	48	472	134	**471**	**134**	470	134
523.xalancbmk_r	48	197	258	198	256	**197**	**257**	48	197	258	198	256	**197**	**257**
525.x264_r	48	**201**	**417**	202	417	201	418	48	192	437	192	438	**192**	**437**
531.deepsjeng_r	48	**359**	**153**	359	153	359	153	48	**359**	**153**	359	153	359	153
541.leela_r	48	534	149	**534**	**149**	534	149	48	534	149	**534**	**149**	534	149
548.exchange2_r	48	**304**	**414**	304	414	303	414	48	**304**	**414**	304	414	303	414
557.xz_r	48	**470**	**110**	471	110	470	110	48	480	108	477	109	**480**	**108**

SPECrate®2017_int_base =	**203**
SPECrate®2017_int_peak =	**210**

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit'
was used to generate numactl commands to bind each copy to a specific processor.
For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

Environment Variables Notes

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH =
    "/home/cpu2017-1.1.8/lib/intel64:/home/cpu2017-1.1.8/lib/ia32:/home/cpu2
    017-1.1.8/je5.0.1-32"
MALLOC_CONF = "retain:true"

General Notes

Binaries compiled on a system with 1x Intel Core i9-7980XE CPU + 64GB RAM
memory using Red Hat Enterprise Linux 8.1
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3>   /proc/sys/vm/drop_caches

(Continued on next page)

Supermicro

SuperServer SYS-620U-TNR
(X12DPU-6 , Intel Xeon Gold 5317)

$SPECrate^{®}2017\_int\_base = 203$

$SPECrate^{®}2017\_int\_peak = 210$

CPU2017 License: 001176		**Test Date:**	Nov-2021
Test Sponsor:	Supermicro	**Hardware Availability:**	Apr-2021
Tested by:	Supermicro	**Software Availability:**	Jun-2021

General Notes (Continued)

```
 runcpu command invoked through numactl i.e.:
 numactl --interleave=all runcpu <etc>
```

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

```
 jemalloc, a general purpose malloc implementation
 built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5
 sources available from jemalloc.net or https://github.com/jemalloc/jemalloc/releases
```

Platform Notes

```
BIOS Settings:
Power Technology = Custom
Power Performance Tuning = BIOS Controls EPB
ENERGY_PERF_BIAS_CFG mode = Extreme Performance
SNC (Sub NUMA) = Enable
KTI Prefetch = Enable
LLC Dead Line Alloc = Disable
DCU Streamer Prefetcher = Disable

 Sysinfo program /home/cpu2017-1.1.8/bin/sysinfo
 Rev: r6622 of 2021-04-07 982a61ec0915b55891ef0e16acafc64d
 running on localhost Tue Nov 16 02:34:20 2021

 SUT (System Under Test) info as seen by some common utilities.
 For more information on this section, see
    https://www.spec.org/cpu2017/Docs/config.html#sysinfo

 From /proc/cpuinfo
    model name : Intel(R) Xeon(R) Gold 5317 CPU @ 3.00GHz
       2  "physical id"s (chips)
       48 "processors"
    cores, siblings (Caution: counting these is hw and system dependent. The following
    excerpts from /proc/cpuinfo might not be reliable.  Use with caution.)
       cpu cores : 12
       siblings  : 24
       physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11
       physical 1: cores 0 1 2 3 4 5 6 7 8 9 10 11

 From lscpu from util-linux 2.36.2:
    Architecture:                  x86_64
    CPU op-mode(s):                32-bit, 64-bit
```

(Continued on next page)

Supermicro

SuperServer SYS-620U-TNR
(X12DPU-6 , Intel Xeon Gold 5317)

SPECrate®2017_int_base = 203

SPECrate®2017_int_peak = 210

CPU2017 License: 001176

Test Sponsor: Supermicro

Tested by: Supermicro

Test Date: Nov-2021

Hardware Availability: Apr-2021

Software Availability: Jun-2021

Platform Notes (Continued)

```
         Byte Order:                     Little Endian
         Address sizes:                  46 bits physical, 57 bits virtual
         CPU(s):                         48
         On-line CPU(s) list:            0-47
         Thread(s) per core:             2
         Core(s) per socket:             12
         Socket(s):                      2
         NUMA node(s):                   4
         Vendor ID:                      GenuineIntel
         CPU family:                     6
         Model:                          106
         Model name:                     Intel(R) Xeon(R) Gold 5317 CPU @ 3.00GHz
         Stepping:                       6
         CPU MHz:                        1587.190
         BogoMIPS:                       6000.00
         Virtualization:                 VT-x
         L1d cache:                      1.1 MiB
         L1i cache:                      768 KiB
         L2 cache:                       30 MiB
         L3 cache:                       36 MiB
         NUMA node0 CPU(s):              0-5,24-29
         NUMA node1 CPU(s):              6-11,30-35
         NUMA node2 CPU(s):              12-17,36-41
         NUMA node3 CPU(s):              18-23,42-47
         Vulnerability Itlb multihit:    Not affected
         Vulnerability L1tf:             Not affected
         Vulnerability Mds:              Not affected
         Vulnerability Meltdown:         Not affected
         Vulnerability Spec store bypass: Mitigation; Speculative Store Bypass disabled via
         prctl and seccomp
         Vulnerability Spectre v1:       Mitigation; usercopy/swapgs barriers and __user
         pointer sanitization
         Vulnerability Spectre v2:       Mitigation; Enhanced IBRS, IBPB conditional, RSB
         filling
         Vulnerability Srbds:            Not affected
         Vulnerability Tsx async abort:  Not affected
         Flags:                          fpu vme de pse tsc msr pae mce cx8 apic sep mtrr
         pge mca cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx
         pdpe1gb rdtscp lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology
         nonstop_tsc cpuid aperfmperf pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2
         ssse3 sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt
         tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault
         epb cat_l3 invpcid_single ssbd mba ibrs ibpb stibp ibrs_enhanced tpr_shadow vnmi
         flexpriority ept vpid ept_ad fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms
         invpcid rtm cqm rdt_a avx512f avx512dq rdseed adx smap avx512ifma clflushopt clwb
         intel_pt avx512cd sha_ni avx512bw avx512vl xsaveopt xsavec xgetbv1 xsaves cqm_llc
         cqm_occup_llc cqm_mbm_total cqm_mbm_local split_lock_detect wbnoinvd dtherm ida arat
```

(Continued on next page)

Supermicro

SuperServer SYS-620U-TNR
(X12DPU-6 , Intel Xeon Gold 5317)

SPECrate®2017_int_base = 203

SPECrate®2017_int_peak = 210

CPU2017 License: 001176
Test Sponsor: Supermicro
Tested by: Supermicro

Test Date: Nov-2021
Hardware Availability: Apr-2021
Software Availability: Jun-2021

Platform Notes (Continued)

```
     pln pts avx512vbmi umip pku ospke avx512_vbmi2 gfni vaes vpclmulqdq avx512_vnni
     avx512_bitalg tme avx512_vpopcntdq la57 rdpid fsrm md_clear pconfig flush_l1d
     arch_capabilities

 From lscpu --cache:
     NAME ONE-SIZE ALL-SIZE WAYS TYPE         LEVEL   SETS PHY-LINE COHERENCY-SIZE
     L1d       48K     1.1M   12 Data             1     64        1             64
     L1i       32K     768K    8 Instruction      1     64        1             64
     L2       1.3M      30M   20 Unified          2   1024        1             64
     L3        18M      36M   12 Unified          3  24576        1             64

 /proc/cpuinfo cache data
    cache size : 18432 KB


 From numactl --hardware
 WARNING: a numactl 'node' might or might not correspond to a physical chip.
   available: 4 nodes (0-3)
   node 0 cpus: 0 1 2 3 4 5 24 25 26 27 28 29
   node 0 size: 128535 MB
   node 0 free: 128199 MB
   node 1 cpus: 6 7 8 9 10 11 30 31 32 33 34 35
   node 1 size: 129020 MB
   node 1 free: 128448 MB
   node 2 cpus: 12 13 14 15 16 17 36 37 38 39 40 41
   node 2 size: 129020 MB
   node 2 free: 128777 MB
   node 3 cpus: 18 19 20 21 22 23 42 43 44 45 46 47
   node 3 size: 129017 MB
   node 3 free: 128800 MB
   node distances:
   node   0   1   2   3
     0:  10  11  20  20
     1:  11  10  20  20
     2:  20  20  10  11
     3:  20  20  11  10

 From /proc/meminfo
    MemTotal:       527969672 kB
    HugePages_Total:        0
    Hugepagesize:        2048 kB

 From /etc/*release* /etc/*version*
    os-release:
      NAME="SLES"
      VERSION="15-SP3"
      VERSION_ID="15.3"
      PRETTY_NAME="SUSE Linux Enterprise Server 15 SP3"
```

(Continued on next page)

Supermicro

SuperServer SYS-620U-TNR
(X12DPU-6 , Intel Xeon Gold 5317)

SPECrate®2017_int_base = 203

SPECrate®2017_int_peak = 210

CPU2017 License: 001176
Test Sponsor: Supermicro
Tested by: Supermicro

Test Date: Nov-2021
Hardware Availability: Apr-2021
Software Availability: Jun-2021

Platform Notes (Continued)

```
        ID="sles"
        ID_LIKE="suse"
        ANSI_COLOR="0;32"
        CPE_NAME="cpe:/o:suse:sles:15:sp3"

uname -a:
   Linux localhost 5.3.18-57-default #1 SMP Wed Apr 28 10:54:41 UTC 2021 (ba3c2e9) x86_64
   x86_64 x86_64 GNU/Linux


Kernel self-reported vulnerability status:

CVE-2018-12207 (iTLB Multihit):                        Not affected
CVE-2018-3620 (L1 Terminal Fault):                     Not affected
Microarchitectural Data Sampling:                      Not affected
CVE-2017-5754 (Meltdown):                              Not affected
CVE-2018-3639 (Speculative Store Bypass):              Mitigation: Speculative Store
                                                       Bypass disabled via prctl and
                                                       seccomp
CVE-2017-5753 (Spectre variant 1):                     Mitigation: usercopy/swapgs
                                                       barriers and __user pointer
                                                       sanitization
CVE-2017-5715 (Spectre variant 2):                     Mitigation: Enhanced IBRS, IBPB:
                                                       conditional, RSB filling
CVE-2020-0543 (Special Register Buffer Data Sampling): Not affected
CVE-2019-11135 (TSX Asynchronous Abort):               Not affected

run-level 3 Nov 16 02:30

SPEC is set to: /home/cpu2017-1.1.8
   Filesystem     Type  Size  Used Avail Use% Mounted on
   /dev/nvme0n1p4 xfs   815G   31G  784G   4% /home


From /sys/devices/virtual/dmi/id
    Vendor:         Supermicro
    Product:        Super Server
    Product Family: Family
    Serial:         0123456789


Additional information from dmidecode 3.2 follows.  WARNING: Use caution when you
interpret this section. The 'dmidecode' program reads system data which is "intended to
allow hardware to be accurately determined", but the intent may not be met, as there are
frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
  Memory:
    16x SK Hynix HMA84GR7DJR4N-XN 32 GB 2 rank 3200, configured at 2933

BIOS:
    BIOS Vendor:        American Megatrends International, LLC.
```

(Continued on next page)

Supermicro

SuperServer SYS-620U-TNR
(X12DPU-6 , Intel Xeon Gold 5317)

SPECrate®2017_int_base = 203

SPECrate®2017_int_peak = 210

CPU2017 License: 001176
Test Sponsor: Supermicro
Tested by: Supermicro

Test Date: Nov-2021
Hardware Availability: Apr-2021
Software Availability: Jun-2021

Platform Notes (Continued)

```
      BIOS Version:      1.1
      BIOS Date:         04/21/2021
      BIOS Revision:     5.22


  (End of data from sysinfo program)
```

Compiler Version Notes

```
==============================================================================
C        | 500.perlbench_r(peak) 557.xz_r(peak)
------------------------------------------------------------------------------
Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R)
  64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation.  All rights reserved.
------------------------------------------------------------------------------


==============================================================================
C        | 502.gcc_r(peak)
------------------------------------------------------------------------------
Intel(R) oneAPI DPC++/C++ Compiler for applications running on IA-32, Version
  2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------


==============================================================================
C        | 500.perlbench_r(base) 502.gcc_r(base) 505.mcf_r(base, peak)
         | 525.x264_r(base, peak) 557.xz_r(base)
------------------------------------------------------------------------------
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
  Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------


==============================================================================
C        | 500.perlbench_r(peak) 557.xz_r(peak)
------------------------------------------------------------------------------
Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R)
  64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation.  All rights reserved.
------------------------------------------------------------------------------


==============================================================================
C        | 502.gcc_r(peak)
------------------------------------------------------------------------------
Intel(R) oneAPI DPC++/C++ Compiler for applications running on IA-32, Version
  2021.1 Build 20201113
```

(Continued on next page)

Supermicro

SuperServer SYS-620U-TNR
(X12DPU-6 , Intel Xeon Gold 5317)

SPECrate®2017_int_base = 203

SPECrate®2017_int_peak = 210

Compiler Version Notes (Continued)

```
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
--------------------------------------------------------------------------------


================================================================================
C         | 500.perlbench_r(base) 502.gcc_r(base) 505.mcf_r(base, peak)
          | 525.x264_r(base, peak) 557.xz_r(base)
--------------------------------------------------------------------------------
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
  Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
--------------------------------------------------------------------------------


================================================================================
C         | 500.perlbench_r(peak) 557.xz_r(peak)
--------------------------------------------------------------------------------
Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R)
  64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation.  All rights reserved.
--------------------------------------------------------------------------------


================================================================================
C         | 502.gcc_r(peak)
--------------------------------------------------------------------------------
Intel(R) oneAPI DPC++/C++ Compiler for applications running on IA-32, Version
  2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
--------------------------------------------------------------------------------


================================================================================
C         | 500.perlbench_r(base) 502.gcc_r(base) 505.mcf_r(base, peak)
          | 525.x264_r(base, peak) 557.xz_r(base)
--------------------------------------------------------------------------------
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
  Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
--------------------------------------------------------------------------------


================================================================================
C++       | 520.omnetpp_r(base, peak) 523.xalancbmk_r(base, peak)
          | 531.deepsjeng_r(base, peak) 541.leela_r(base, peak)
--------------------------------------------------------------------------------
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
  Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
--------------------------------------------------------------------------------


================================================================================
```

(Continued on next page)

SPEC CPU®2017 Integer Rate Result

Supermicro

SuperServer SYS-620U-TNR
(X12DPU-6 , Intel Xeon Gold 5317)

SPECrate®2017_int_base = 203

SPECrate®2017_int_peak = 210

Compiler Version Notes (Continued)

```
Fortran | 548.exchange2_r(base, peak)
------------------------------------------------------------------------
Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on
  Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation.  All rights reserved.
------------------------------------------------------------------------
```

Base Compiler Invocation

C benchmarks:
icx

C++ benchmarks:
icpx

Fortran benchmarks:
ifort

Base Portability Flags

500.perlbench_r: `-DSPEC_LP64 -DSPEC_LINUX_X64`
502.gcc_r: `-DSPEC_LP64`
505.mcf_r: `-DSPEC_LP64`
520.omnetpp_r: `-DSPEC_LP64`
523.xalancbmk_r: `-DSPEC_LP64 -DSPEC_LINUX`
525.x264_r: `-DSPEC_LP64`
531.deepsjeng_r: `-DSPEC_LP64`
541.leela_r: `-DSPEC_LP64`
548.exchange2_r: `-DSPEC_LP64`
557.xz_r: `-DSPEC_LP64`

Base Optimization Flags

C benchmarks:
```
-w -std=c11 -m64 -Wl,-z,muldefs -xCORE-AVX512 -O3 -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries
-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin
-lqkmalloc
```

(Continued on next page)

Supermicro

SuperServer SYS-620U-TNR
(X12DPU-6 , Intel Xeon Gold 5317)

SPECrate®2017_int_base = 203

SPECrate®2017_int_peak = 210

CPU2017 License: 001176
Test Sponsor: Supermicro
Tested by: Supermicro

Test Date: Nov-2021
Hardware Availability: Apr-2021
Software Availability: Jun-2021

Base Optimization Flags (Continued)

C++ benchmarks:
```
-w -m64 -Wl,-z,muldefs -xCORE-AVX512 -O3 -ffast-math -flto
-mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries
-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin
-lqkmalloc
```

Fortran benchmarks:
```
-w -m64 -Wl,-z,muldefs -xCORE-AVX512 -O3 -ipo -no-prec-div
-qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte
-auto -mbranches-within-32B-boundaries
-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin
-lqkmalloc
```

Peak Compiler Invocation

C benchmarks (except as noted below):
```
icx
```

500.perlbench_r: `icc`

557.xz_r: `icc`

C++ benchmarks:
```
icpx
```

Fortran benchmarks:
```
ifort
```

Peak Portability Flags

500.perlbench_r: `-DSPEC_LP64 -DSPEC_LINUX_X64`
502.gcc_r: `-D_FILE_OFFSET_BITS=64`
505.mcf_r: `-DSPEC_LP64`
520.omnetpp_r: `-DSPEC_LP64`
523.xalancbmk_r: `-DSPEC_LP64 -DSPEC_LINUX`
525.x264_r: `-DSPEC_LP64`
531.deepsjeng_r: `-DSPEC_LP64`
541.leela_r: `-DSPEC_LP64`
548.exchange2_r: `-DSPEC_LP64`
557.xz_r: `-DSPEC_LP64`

SPEC CPU®2017 Integer Rate Result

Copyright 2017-2021 Standard Performance Evaluation Corporation

Supermicro

SuperServer SYS-620U-TNR
(X12DPU-6 , Intel Xeon Gold 5317)

SPECrate®2017_int_base = 203

SPECrate®2017_int_peak = 210

CPU2017 License: 001176
Test Sponsor: Supermicro
Tested by: Supermicro

Test Date: Nov-2021
Hardware Availability: Apr-2021
Software Availability: Jun-2021

Peak Optimization Flags

C benchmarks:

```
500.perlbench_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2)
-xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -fno-strict-overflow
-mbranches-within-32B-boundaries
-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin
-lqkmalloc
```

```
502.gcc_r: -m32
-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/ia32_lin
-std=gnu89 -Wl,-z,muldefs -fprofile-generate(pass 1)
-fprofile-use=default.profdata(pass 2) -xCORE-AVX512 -flto
-Ofast(pass 1) -O3 -ffast-math -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries
-L/usr/local/jemalloc32-5.0.1/lib -ljemalloc
```

```
505.mcf_r: basepeak = yes
```

```
525.x264_r: -w -std=c11 -m64 -Wl,-z,muldefs -xCORE-AVX512 -flto
-O3 -ffast-math -qopt-mem-layout-trans=4 -fno-alias
-mbranches-within-32B-boundaries
-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin
-lqkmalloc
```

```
557.xz_r: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -mbranches-within-32B-boundaries
-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin
-lqkmalloc
```

C++ benchmarks:

```
520.omnetpp_r: basepeak = yes
```

```
523.xalancbmk_r: basepeak = yes
```

```
531.deepsjeng_r: basepeak = yes
```

```
541.leela_r: basepeak = yes
```

Fortran benchmarks:

```
548.exchange2_r: basepeak = yes
```

Standard Performance Evaluation Corporation (info@spec.org)
https://www.spec.org/

SPEC CPU®2017 Integer Rate Result

Copyright 2017-2021 Standard Performance Evaluation Corporation

Supermicro

SuperServer SYS-620U-TNR
(X12DPU-6 , Intel Xeon Gold 5317)

SPECrate®2017_int_base = 203

SPECrate®2017_int_peak = 210

CPU2017 License: 001176		**Test Date:**	Nov-2021
Test Sponsor:	Supermicro	**Hardware Availability:**	Apr-2021
Tested by:	Supermicro	**Software Availability:**	Jun-2021

The flags files that were used to format this result can be browsed at

http://www.spec.org/cpu2017/flags/Intel-ic2021-official-linux64_revA.html
http://www.spec.org/cpu2017/flags/Supermicro-Platform-Settings-V1.2-ICX-revB.html

You can also download the XML flags sources by saving the following links:

http://www.spec.org/cpu2017/flags/Intel-ic2021-official-linux64_revA.xml
http://www.spec.org/cpu2017/flags/Supermicro-Platform-Settings-V1.2-ICX-revB.xml

SPEC CPU and SPECrate are registered trademarks of the Standard Performance Evaluation Corporation. All other brand and product names appearing in this result are trademarks or registered trademarks of their respective holders.

For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.1.8 on 2021-11-16 05:34:20-0500.
Report generated on 2021-12-07 16:57:47 by CPU2017 PDF formatter v6442.
Originally published on 2021-12-07.