



# SPEC CPU®2017 Integer Rate Result

Copyright 2017-2021 Standard Performance Evaluation Corporation

## Tyrone Systems

(Test Sponsor: Netweb Pte Ltd)

Tyrone Camarero DIT400TR-48RL  
(2.20 GHz, Intel Xeon Silver 4214)

SPECrate®2017\_int\_base = 144

SPECrate®2017\_int\_peak = 149

CPU2017 License: 006042

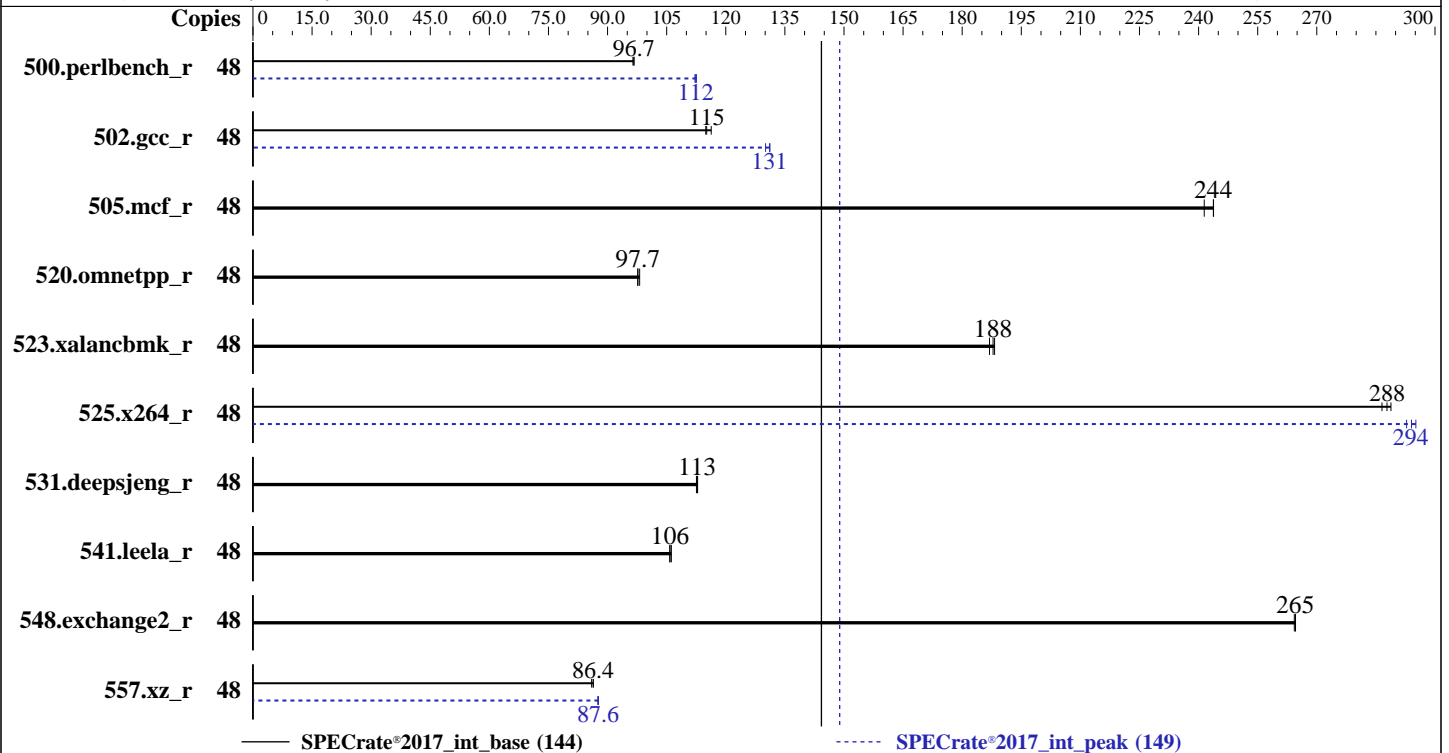
Test Sponsor: Netweb Pte Ltd

Tested by: Tyrone Systems

Test Date: Aug-2021

Hardware Availability: Apr-2019

Software Availability: Jul-2021



### Hardware

CPU Name: Intel Xeon Silver 4214  
 Max MHz: 3200  
 Nominal: 2200  
 Enabled: 24 cores, 2 chips, 2 threads/core  
 Orderable: 1,2 Chips  
 Cache L1: 32 KB I + 32 KB D on chip per core  
 L2: 1 MB I+D on chip per core  
 L3: 16.5 MB I+D on chip per chip  
 Other: None  
 Memory: 384 GB (12 x 32 GB 2Rx4 PC4-2933P-R, running at 2400)  
 Storage: 1 x 480 GB SATA SSD  
 Other: None

### Software

OS: CentOS Linux release 8.4.2105  
 Kernel 4.18.0-305.3.1.el8.x86\_64  
 Compiler: C/C++: Version 2021.1 of Intel oneAPI DPC++/C++ Compiler Build 20201113 for Linux;  
 Fortran: Version 2021.1 of Intel Fortran Compiler Classic Build 20201112 for Linux;  
 C/C++: Version 2021.1 of Intel C/C++ Compiler Classic Build 20201112 for Linux  
 Parallel: No  
 Firmware: Version V8.104 released Jul-2021  
 File System: xfs  
 System State: Run level 3 (multi-user)  
 Base Pointers: 64-bit  
 Peak Pointers: 32/64-bit  
 Other: jemalloc memory allocator V5.0.1  
 Power Management: BIOS set to prefer performance at the cost of additional power usage.



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## Results Table

Benchmark	Base							Peak						
	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
500.perlbench_r	48	<b>790</b>	<b>96.7</b>	792	96.4	790	96.7	48	<b>680</b>	<b>112</b>	679	113	681	112
502.gcc_r	48	<b>590</b>	<b>115</b>	584	116	591	115	48	<b>522</b>	<b>130</b>	<b>518</b>	<b>131</b>	518	131
505.mcf_r	48	321	241	<b>318</b>	<b>244</b>	318	244	48	321	241	<b>318</b>	<b>244</b>	318	244
520.omnetpp_r	48	645	97.6	642	98.1	<b>645</b>	<b>97.7</b>	48	645	97.6	642	98.1	<b>645</b>	<b>97.7</b>
523.xalancbmk_r	48	271	187	269	188	<b>270</b>	<b>188</b>	48	271	187	269	188	<b>270</b>	<b>188</b>
525.x264_r	48	293	287	<b>292</b>	<b>288</b>	291	289	48	<b>286</b>	<b>294</b>	285	295	287	293
531.deepsjeng_r	48	489	113	487	113	<b>488</b>	<b>113</b>	48	489	113	487	113	<b>488</b>	<b>113</b>
541.leela_r	48	749	106	<b>751</b>	<b>106</b>	752	106	48	749	106	<b>751</b>	<b>106</b>	752	106
548.exchange2_r	48	475	265	476	264	<b>475</b>	<b>265</b>	48	475	265	476	264	<b>475</b>	<b>265</b>
557.xz_r	48	<b>600</b>	<b>86.4</b>	603	85.9	600	86.4	48	592	87.5	591	87.7	<b>592</b>	<b>87.6</b>

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Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

## Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

## Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

## Environment Variables Notes

Environment variables set by runcpu before the start of the run:

LD\_LIBRARY\_PATH =

"/home/cpu2017/lib/intel64:/home/cpu2017/lib/ia32:/home/cpu2017/je5.0.1-32"

MALLOC\_CONF = "retain:true"

## General Notes

Binaries compiled locally by Netweb  
Transparent Huge Pages enabled by default  
Prior to runcpu invocation  
Filesystem page cache synced and cleared with:  
sync; echo 3> /proc/sys/vm/drop\_caches  
runcpu command invoked through numactl i.e.:  
numactl --interleave=all runcpu <etc>

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## General Notes (Continued)

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

jemalloc, a general purpose malloc implementation

built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5

sources available from jemalloc.net or <https://github.com/jemalloc/jemalloc/releases>

## Platform Notes

BIOS Settings:

Power Technology set to Custom

Power Performance Tuning set to BIOS Controls EPB

ENERGY\_PERF\_BIAS\_CFG mode set to Performance

LLC Dead Line Alloc set to Disable

sysinfo program /home/cpu2017/bin/sysinfo

Rev: r6622 of 2021-04-07 982a61ec0915b55891ef0e16acafc64d

running on localhost.localdomain Wed Aug 11 21:07:04 2021

SUT (System Under Test) info as seen by some common utilities.

For more information on this section, see

<https://www.spec.org/cpu2017/Docs/config.html#sysinfo>

From /proc/cpuinfo

model name : Intel(R) Xeon(R) Silver 4214 CPU @ 2.20GHz

2 "physical id"s (chips)

48 "processors"

cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)

cpu cores : 12

siblings : 24

physical 0: cores 0 1 2 3 4 5 8 9 10 11 12 13

physical 1: cores 0 1 2 3 4 5 8 9 10 11 12 13

From lscpu from util-linux 2.32.1:

Architecture: x86\_64

CPU op-mode(s): 32-bit, 64-bit

Byte Order: Little Endian

CPU(s): 48

On-line CPU(s) list: 0-47

Thread(s) per core: 2

Core(s) per socket: 12

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## Platform Notes (Continued)

```

Socket(s):                2
NUMA node(s):            2
Vendor ID:               GenuineIntel
BIOS Vendor ID:         Intel(R) Corporation
CPU family:              6
Model:                   85
Model name:              Intel(R) Xeon(R) Silver 4214 CPU @ 2.20GHz
BIOS Model name:         Intel(R) Xeon(R) Silver 4214 CPU @ 2.20GHz
Stepping:                7
CPU MHz:                 1000.120
CPU max MHz:             3200.0000
CPU min MHz:             1000.0000
BogoMIPS:                4400.00
Virtualization:         VT-x
L1d cache:               32K
L1i cache:               32K
L2 cache:                1024K
L3 cache:                16896K
NUMA node0 CPU(s):      0-11,24-35
NUMA node1 CPU(s):      12-23,36-47
Flags:                   fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
aperfmpperf pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16
xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave
avx fl6c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_l3 cdp_l3
invpcid_single intel_ppin ssbd mba ibrs ibpb stibp ibrs_enhanced tpr_shadow vnmi
flexpriority ept vpid ept_ad fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms
invpcid cqm mpx rdt_a avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt
avx512cd avx512bw avx512vl xsaveopt xsavec xgetbv1 xsaves cqm_llc cqm_occup_llc
cqm_mbm_total cqm_mbm_local dtherm ida arat pln pts hwp hwp_act_window hwp_epp
hwp_pkg_req pku ospke avx512_vnni md_clear flush_lld arch_capabilities

```

```

/proc/cpuinfo cache data
cache size : 16896 KB

```

From numactl --hardware

WARNING: a numactl 'node' might or might not correspond to a physical chip.

```

available: 2 nodes (0-1)
node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 24 25 26 27 28 29 30 31 32 33 34 35
node 0 size: 192070 MB
node 0 free: 191490 MB
node 1 cpus: 12 13 14 15 16 17 18 19 20 21 22 23 36 37 38 39 40 41 42 43 44 45 46 47
node 1 size: 193530 MB
node 1 free: 192915 MB
node distances:
node  0  1

```

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## Platform Notes (Continued)

```
0: 10 21
1: 21 10
```

From /proc/meminfo

```
MemTotal:      394855532 kB
HugePages_Total:      0
Hugepagesize:    2048 kB
```

/sbin/tuned-adm active

Current active profile: throughput-performance

/sys/devices/system/cpu/cpu\*/cpufreq/scaling\_governor has performance

From /etc/\*release\* /etc/\*version\*

```
centos-release: CentOS Linux release 8.4.2105
centos-release-upstream: Derived from Red Hat Enterprise Linux 8.4
os-release:
  NAME="CentOS Linux"
  VERSION="8"
  ID="centos"
  ID_LIKE="rhel fedora"
  VERSION_ID="8"
  PLATFORM_ID="platform:el8"
  PRETTY_NAME="CentOS Linux 8"
  ANSI_COLOR="0;31"
redhat-release: CentOS Linux release 8.4.2105
system-release: CentOS Linux release 8.4.2105
system-release-cpe: cpe:/o:centos:centos:8
```

uname -a:

```
Linux localhost.localdomain 4.18.0-305.3.1.el8.x86_64 #1 SMP Tue Jun 1 16:14:33 UTC
2021 x86_64 x86_64 x86_64 GNU/Linux
```

Kernel self-reported vulnerability status:

```
CVE-2018-12207 (iTLB Multihit):          KVM: Mitigation: Split huge pages
CVE-2018-3620 (L1 Terminal Fault):       Not affected
Microarchitectural Data Sampling:       Not affected
CVE-2017-5754 (Meltdown):               Not affected
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled via prctl and seccomp
CVE-2017-5753 (Spectre variant 1):       Mitigation: usercopy/swapgs barriers and __user pointer sanitization
CVE-2017-5715 (Spectre variant 2):       Mitigation: Enhanced IBRS, IBPB:
```

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## Platform Notes (Continued)

CVE-2020-0543 (Special Register Buffer Data Sampling): Not affected  
CVE-2019-11135 (TSX Asynchronous Abort): Mitigation: TSX disabled

run-level 3 Aug 11 21:05

SPEC is set to: /home/cpu2017

Filesystem	Type	Size	Used	Avail	Use%	Mounted on
/dev/mapper/cl-home	xfs	372G	76G	296G	21%	/home

From /sys/devices/virtual/dmi/id

```
Vendor:      Tyrone Systems
Product:    Tyrone Camarero DIT400TR-48RL
Product Family: empty
Serial:     empty
```

Additional information from dmidecode 3.2 follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

Memory:

12x Samsung M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2400

BIOS:

```
BIOS Vendor:    American Megatrends Inc.
BIOS Version:   V8.104
BIOS Date:      07/27/2021
BIOS Revision:  5.14
Firmware Revision: 6.1
```

(End of data from sysinfo program)

## Compiler Version Notes

```
=====
C      | 500.perlbench_r(peak) 557.xz_r(peak)
-----
```

```
Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R)
64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
-----
```

```
=====
C      | 502.gcc_r(peak)
-----
```

Intel(R) oneAPI DPC++/C++ Compiler for applications running on IA-32, Version

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## Compiler Version Notes (Continued)

2021.1 Build 20201113

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=====  
C | 500.perlbench\_r(base) 502.gcc\_r(base) 505.mcf\_r(base, peak)  
| 525.x264\_r(base, peak) 557.xz\_r(base)  
=====

Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,  
Version 2021.1 Build 20201113

Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

=====  
C | 500.perlbench\_r(peak) 557.xz\_r(peak)  
=====

Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R)  
64, Version 2021.1 Build 20201112\_000000

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=====  
C | 502.gcc\_r(peak)  
=====

Intel(R) oneAPI DPC++/C++ Compiler for applications running on IA-32, Version  
2021.1 Build 20201113

Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

=====  
C | 500.perlbench\_r(base) 502.gcc\_r(base) 505.mcf\_r(base, peak)  
| 525.x264\_r(base, peak) 557.xz\_r(base)  
=====

Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,  
Version 2021.1 Build 20201113

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=====  
C | 500.perlbench\_r(peak) 557.xz\_r(peak)  
=====

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## Compiler Version Notes (Continued)

C | 502.gcc\_r(peak)

-----  
Intel(R) oneAPI DPC++/C++ Compiler for applications running on IA-32, Version  
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-----

=====  
C | 500.perlbench\_r(base) 502.gcc\_r(base) 505.mcf\_r(base, peak)  
525.x264\_r(base, peak) 557.xz\_r(base)

Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,  
Version 2021.1 Build 20201113  
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-----

=====  
C++ | 520.omnetpp\_r(base, peak) 523.xalancbmk\_r(base, peak)  
531.deepsjeng\_r(base, peak) 541.leela\_r(base, peak)

Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,  
Version 2021.1 Build 20201113  
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.  
-----

=====  
Fortran | 548.exchange2\_r(base, peak)  
-----

Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on  
Intel(R) 64, Version 2021.1 Build 20201112\_000000  
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.  
-----

## Base Compiler Invocation

C benchmarks:

icx

C++ benchmarks:

icpx

Fortran benchmarks:

ifort





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## Base Portability Flags

```
500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502 gcc_r: -DSPEC_LP64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64
```

## Base Optimization Flags

C benchmarks:

```
-w -std=c11 -m64 -Wl,-z,muldefs -xCORE-AVX512 -O3 -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries
-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin
-lqkmalloc
```

C++ benchmarks:

```
-w -m64 -Wl,-z,muldefs -xCORE-AVX512 -O3 -ffast-math -flto
-mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries
-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin
-lqkmalloc
```

Fortran benchmarks:

```
-w -m64 -Wl,-z,muldefs -xCORE-AVX512 -O3 -ipo -no-prec-div
-qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte
-auto -mbranches-within-32B-boundaries
-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin
-lqkmalloc
```

## Peak Compiler Invocation

C benchmarks (except as noted below):

icx

500.perlbench\_r: icc

(Continued on next page)



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## Peak Compiler Invocation (Continued)

557.xz\_r: icc

C++ benchmarks:

icpx

Fortran benchmarks:

ifort

## Peak Portability Flags

500.perlbench\_r: -DSPEC\_LP64 -DSPEC\_LINUX\_X64

502.gcc\_r: -D\_FILE\_OFFSET\_BITS=64

505.mcf\_r: -DSPEC\_LP64

520.omnetpp\_r: -DSPEC\_LP64

523.xalancbmk\_r: -DSPEC\_LP64 -DSPEC\_LINUX

525.x264\_r: -DSPEC\_LP64

531.deepsjeng\_r: -DSPEC\_LP64

541.leela\_r: -DSPEC\_LP64

548.exchange2\_r: -DSPEC\_LP64

557.xz\_r: -DSPEC\_LP64

## Peak Optimization Flags

C benchmarks:

500.perlbench\_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2)

-xCORE-AVX512 -ipo -O3 -no-prec-div

-qopt-mem-layout-trans=4 -fno-strict-overflow

-mbranches-within-32B-boundaries

-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64\_lin

-lqkmalloc

502.gcc\_r: -m32

-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/ia32\_lin

-std=gnu89 -Wl,-z,muldefs -fprofile-generate(pass 1)

-fprofile-use=default.profddata(pass 2) -xCORE-AVX512 -flto

-Ofast(pass 1) -O3 -ffast-math -qopt-mem-layout-trans=4

-mbranches-within-32B-boundaries

-L/usr/local/je5.0.1-32/lib -ljemalloc

505.mcf\_r: basepeak = yes

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## Peak Optimization Flags (Continued)

```
525.x264_r: -w -std=c11 -m64 -Wl,-z,muldefs -xCORE-AVX512 -flto
-O3 -ffast-math -qopt-mem-layout-trans=4 -fno-alias
-mbranches-within-32B-boundaries
-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin
-lqkmalloc
```

```
557.xz_r: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -mbranches-within-32B-boundaries
-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin
-lqkmalloc
```

C++ benchmarks:

520.omnetpp\_r: basepeak = yes

523.xalancbmk\_r: basepeak = yes

531.deepsjeng\_r: basepeak = yes

541.leela\_r: basepeak = yes

Fortran benchmarks:

548.exchange2\_r: basepeak = yes

The flags files that were used to format this result can be browsed at

[http://www.spec.org/cpu2017/flags/Intel-ic2021-official-linux64\\_revA.html](http://www.spec.org/cpu2017/flags/Intel-ic2021-official-linux64_revA.html)

<http://www.spec.org/cpu2017/flags/Tyrone-Platform-Settings-V1.2-CLX-revI.html>

You can also download the XML flags sources by saving the following links:

[http://www.spec.org/cpu2017/flags/Intel-ic2021-official-linux64\\_revA.xml](http://www.spec.org/cpu2017/flags/Intel-ic2021-official-linux64_revA.xml)

<http://www.spec.org/cpu2017/flags/Tyrone-Platform-Settings-V1.2-CLX-revI.xml>

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For questions about this result, please contact the tester. For other inquiries, please contact [info@spec.org](mailto:info@spec.org).

Tested with SPEC CPU®2017 v1.1.8 on 2021-08-11 21:07:03-0400.

Report generated on 2021-09-21 16:17:14 by CPU2017 PDF formatter v6442.

Originally published on 2021-09-21.