SPEC CPU®2017 Floating Point Speed Result

Cisco Systems

Cisco UCS B200 M5 (Intel Xeon Platinum 8256, 3.80GHz)

SPECspeed®2017_fp_base =

SPECspeed®2017_fp_peak =

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Sep-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

SPEC has determined that this result does not comply with the SPEC OSG Guidelines for General Availability and the SPEC CPU 2017 run and reporting rules. Specifically, the submitter has notified SPEC that the system was run with a CPU that is not supported by Cisco with the given system configuration.

Threads
603.bwaves_s
607.cactuBSSN_s
619.lbm_s
621.wrf_s
627.cam4_s
628.pop2_s
638.imagick_s
644.nab_s
649.fotonik3d_s
654.roms_s

Hardware

CPU Name: Intel Xeon Platinum 8256
Max MHz: 390
Nominal: 3800
Enabled: 8 cores, chip
Orderable: 1, 2 chip(s)
: 32 KB I + 32 KB D on chip per core
2: 1 MB I+D on chip per core
L3: 16.5 MB I+D on chip per chip
Other: None
Memory: 768 GB (24 x 32 GB 2Rx4 PC4-2933V-R)
Storage: 1 x 960 GB M.2 SATA SSD
Other: None

Software

OS: SUSE Linux Enterprise Server 15
4.12.14-23-default
Compiler: C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux;
Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux
Parallel: Yes
Firmware: Version 4.0.4b released Apr-2019
File System: btrfs
System State: Run level 3 (multi-user)
Base Pointers: 64-bit
Peak Pointers: Not Applicable
Other: None
Power Management: --

Cisco Systems

Cisco UCS B200 M5 (Intel Xeon Platinum 8256, 3.80GHz)

SPECspeed®2017_fp_base =

SPECspeed®2017_fp_peak =

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Sep-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

SPEC has determined that this result does not comply with the SPEC OSG Guidelines for General Availability and the SPEC CPU 2017 run and reporting rules. Specifically, the submitter has notified SPEC that the system was run with a CPU that is not supported by Cisco with the given system configuration.

Results Table

Benchmark	Base							Peak						
	Threads	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Threads	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
603.bwaves_s	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC
607.cactuBSSN_s	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC
619.lbm_s	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC
621.wrf_s	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC
627.cam4_s	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC
628.pop2_s	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC
638.imagick_s	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC
644.nab_s	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC
649.fotonik3d_s	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC
654.roms_s	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC

SPECspeed®2017_fp_base =
SPECspeed®2017_fp_peak =

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Operating System Notes

```
Stack size set to unlimited using "ulimit -s unlimited"
```

General Notes

```
Environment variables set by runcpu before the start of the run:
KMP_AFFINITY = "granularity=fine,compact"
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64"
OMP_STACKSIZE = "192M"

 Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM
 memory using Redhat Enterprise Linux 7.5
 Transparent Huge Pages enabled by default
 Prior to runcpu invocation
 Filesystem page cache synced and cleared with:
 sync; echo 3>       /proc/sys/vm/drop_caches
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown)
is mitigated in the system as tested and documented.
```

(Continued on next page)

General Notes (Continued)

```
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2)
is mitigated in the system as tested and documented.
```

Platform Notes

```
BIOS Settings:
Intel HyperThreading Technology set to Disabled
CPU performance set to Enterprise
Power Performance Tuning set to OS Controls
SNC set to Disabled
IMC Interleaving set to Auto
Patrol Scrub set to Disabled
 Sysinfo program /home/cpu2017/bin/sysinfo
 Rev: r5797 of 2019-06-14 b6c45e4568ad54c135fd618bcc091c0f
 running on linux-5vvl Sat Sep 28 16:29:55 2019

 SUT (System Under Test) info as seen by some common utilities.
 For more information on this section, see
   https://www.spec.org/cpu2017/Docs/config.html#sysinfo

 From /proc/cpuinfo
    model name : Intel(R) Xeon(R) Platinum 8256 CPU @ 3.80GHz
       2  "physical id"s (chips)
       8 "processors"
    cores, siblings (Caution: counting these is hw and system dependent. The following
    excerpts from /proc/cpuinfo might not be reliable.  Use with caution.)
       cpu cores : 4
       siblings  : 4
       physical 0: cores 2 4 9 13
       physical 1: cores 1 2 4 13

 From lscpu:
      Architecture:        x86_64
      CPU op-mode(s):      32-bit, 64-bit
      Byte Order:          Little Endian
```


(Continued on next page)

Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Platinum 8256, 3.80GHz)

SPECspeed®2017_fp_base =
SPECspeed®2017_fp_peak =

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Sep-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

Platform Notes (Continued)

```
      CPU(s):              8
      On-line CPU(s) list: 0-7
      Thread(s) per core:  1
      Core(s) per socket:  4
      Socket(s):           2
      NUMA node(s):        2
      Vendor ID:           GenuineIntel
      CPU family:          6
      Model:               85
      Model name:          Intel(R) Xeon(R) Platinum 8256 CPU @ 3.80GHz
      Stepping:            6
      CPU MHz:             3800.000
      CPU max MHz:         3900.0000
      CPU min MHz:         1200.0000
      BogoMIPS:            7600.00
      Virtualization:      VT-x
      L1d cache:           32K
      L1i cache:           32K
      L2 cache:            1024K
      L3 cache:            16896K
      NUMA node0 CPU(s):   0-3
      NUMA node1 CPU(s):   4-7
      Flags:               fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
                           pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
                           lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
                           aperfmperf tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3
                           sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt
                           tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault
                           epb cat_l3 cdp_l3 invpcid_single intel_ppin mba tpr_shadow vnmi flexpriority ept
                           vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm cqm mpx rdt_a
                           avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl
                           xsaveopt xsavec xgetbv1 xsaves cqm_llc cqm_occup_llc cqm_mbm_total cqm_mbm_local
                           ibpb ibrs stibp dtherm ida arat pln pts hwp hwp_act_window hwp_epp hwp_pkg_req pku
                           ospke avx512_vnni arch_capabilities ssbd

    /proc/cpuinfo cache data
       cache size : 16896 KB
```

(Continued on next page)

Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Platinum 8256, 3.80GHz)

SPECspeed®2017_fp_base =
SPECspeed®2017_fp_peak =

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Sep-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

SPEC has determined that this result does not comply with the SPEC OSG Guidelines for General Availability and the SPEC CPU 2017 run and reporting rules. Specifically, the submitter has notified SPEC that the system was run with a CPU that is not supported by Cisco with the given system configuration.

Platform Notes (Continued)

```
From numactl --hardware  WARNING: a numactl 'node' might or might not correspond to a
physical chip.
  available: 2 nodes (0-1)
  node 0 cpus: 0 1 2 3
  node 0 size: 385619 MB
  node 0 free: 383193 MB
  node 1 cpus: 4 5 6 7
  node 1 size: 387018 MB
  node 1 free: 379951 MB
  node distances:
  node   0   1
    0:  10  21
    1:  21  10

From /proc/meminfo
   MemTotal:       791181844 kB
   HugePages_Total:       0
   Hugepagesize:       2048 kB

From /etc/*release* /etc/*version*
   os-release:
      NAME="SLES"
      VERSION="15"
      VERSION_ID="15"
      PRETTY_NAME="SUSE Linux Enterprise Server 15"
      ID="sles"
      ID_LIKE="suse"
      ANSI_COLOR="0;32"
      CPE_NAME="cpe:/o:suse:sles:15"

uname -a:
   Linux linux-5vrl 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
   x86_64 x86_64 x86_64 GNU/Linux

run-level 3 Sep 28 06:41
```

(Continued on next page)

Platform Notes (Continued)

```
SPEC is set to: /home/cpu2017
   Filesystem     Type   Size  Used Avail Use% Mounted on
   /dev/sdb1      btrfs  224G   22G  202G  10% /home

Additional information from dmidecode follows.  WARNING: Use caution when you interpret
this section. The 'dmidecode' program reads system data which is "intended to allow
hardware to be accurately determined", but the intent may not be met, as there are
frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
  BIOS Cisco Systems, Inc. B200M5.4.0.4b.0.0407191258 04/07/2019
  Memory:
   24x 0xCE00 M393A4K40CB2-CV[illegible]GB 2 rank 2933, configured at 2934

(End of data from sysinfo program)
```

Compiler Version Notes

```
==============================================================================
C                619.lbm_s(base) 638.imagick_s(base) 644.nab_s(base)
------------------------------------------------------------------------------
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
  Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation.  All rights reserved.
------------------------------------------------------------------------------

==============================================================================
C++, C, Fortran | 607.cactuBSSN_s(base)
------------------------------------------------------------------------------
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
  Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation.  All rights reserved.
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
  Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation.  All rights reserved.
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
  64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation.  All rights reserved.
------------------------------------------------------------------------------
```


(Continued on next page)

SPEC has determined that this result does not comply with the SPEC OSG Guidelines for General Availability and the SPEC CPU 2017 run and reporting rules. Specifically, the submitter has notified SPEC that the system was run with a CPU that is not supported by Cisco with the given system configuration.

Compiler Version Notes (Continued)

```
==============================================================================
Fortran         | 603.bwaves_s(base) 649.fotonik3d_s(base) 654.roms_s(base)
------------------------------------------------------------------------------
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
  64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation.  All rights reserved.
------------------------------------------------------------------------------

==============================================================================
Fortran, C      | 621.wrf_s(base) 627.cam4_s(base) 628.pop2_s(base)
------------------------------------------------------------------------------
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
  64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation.  All rights reserved.
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
  Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation.  All rights reserved.
------------------------------------------------------------------------------
```

Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

Fortran benchmarks:
ifort -m64

Benchmarks using both Fortran and C:
ifort -m64 icc -m64 -std=c11

Benchmarks using Fortran, C, and C++:
icpc -m64 icc -m64 -std=c11 ifort -m64

Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Platinum 8256, 3.80GHz)

SPECspeed®2017_fp_base =
SPECspeed®2017_fp_peak =

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Sep-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

SPEC has determined that this result does not comply with the SPEC OSG Guidelines for General Availability and the SPEC CPU 2017 run and reporting rules. Specifically, the submitter has notified SPEC that the system was run with a CPU that is not supported by Cisco with the given system configuration.

Base Portability Flags

603.bwaves_s: -DSPEC_LP64
607.cactuBSSN_s: -DSPEC_LP64
619.lbm_s: -DSPEC_LP64
621.wrf_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
627.cam4_s: -DSPEC_LP64 -DSPEC_CASE_FLAG
628.pop2_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian -assume byterecl
638.imagick_s: -DSPEC_LP64
644.nab_s: -DSPEC_LP64
649.fotonik3d_s: -DSPEC_LP64
654.roms_s: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP

Fortran benchmarks:
-DSPEC_OPENMP -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -nostandard-realloc-lhs

Benchmarks using both Fortran and C:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP -nostandard-realloc-lhs

Benchmarks using Fortran, C, and C++:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP -nostandard-realloc-lhs

SPEC has determined that this result does not comply with the SPEC OSG Guidelines for General Availability and the SPEC CPU 2017 run and reporting rules. Specifically, the submitter has notified SPEC that the system was run with a CPU that is not supported by Cisco with the given system configuration.

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2017/flags/Intel-ic19.0u1-official-linux64.2019-07-09.html
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revJ.html

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Intel-ic19.0u1-official-linux64.2019-07-09.xml
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revJ.xml

For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.0.2 on 2019-09-28 19:29:54-0400.
Report generated on 2020-07-13 20:11:34 by CPU2017 PDF formatter v6255.
Originally published on 2019-11-04.