# SPEC® CPU2017 Floating Point Rate Result

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## Cisco Systems

Cisco UCS C480 M5 (Intel Xeon Gold 6146 3.20 GHz)

SPECrate2017_fp_base =  350

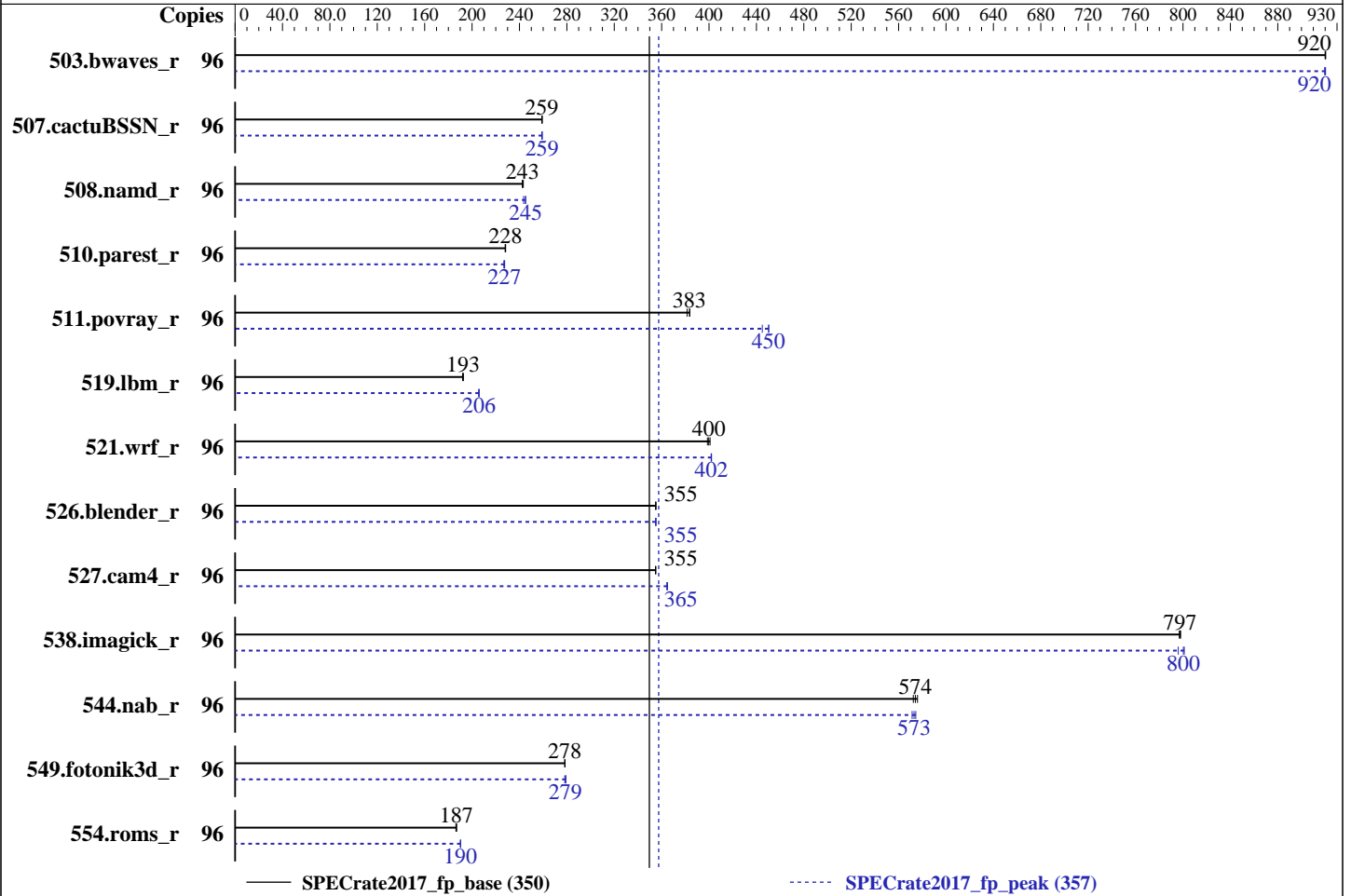SPECrate2017_fp_peak =  357

**CPU2017 License:** 9019

**Test Sponsor:** Cisco Systems

**Tested by:** Cisco Systems

**Test Date:** Nov-2018

**Hardware Availability:** Aug-2017

**Software Availability:** Mar-2018

| Benchmark | Copies | base | peak |
|-----------|--------|------|------|
| 503.bwaves_r | 96 | 920 | 920 |
| 507.cactuBSSN_r | 96 | 259 | 259 |
| 508.namd_r | 96 | 243 | 245 |
| 510.parest_r | 96 | 228 | 227 |
| 511.povray_r | 96 | 383 | 450 |
| 519.lbm_r | 96 | 193 | 206 |
| 521.wrf_r | 96 | 400 | 402 |
| 526.blender_r | 96 | 355 | 355 |
| 527.cam4_r | 96 | 355 | 365 |
| 538.imagick_r | 96 | 797 | 800 |
| 544.nab_r | 96 | 574 | 573 |
| 549.fotonik3d_r | 96 | 278 | 279 |
| 554.roms_r | 96 | 187 | 190 |

—— SPECrate2017_fp_base (350)        ----- SPECrate2017_fp_peak (357)

## Hardware

CPU Name: Intel Xeon Gold 6146
 Max MHz.: 4200
 Nominal: 3200
Enabled: 48 cores, 4 chips, 2 threads/core
Orderable: 2,4 Chips
Cache L1: 32 KB I + 32 KB D on chip per core
 L2: 1 MB I+D on chip per core
 L3: 24.75 MB I+D on chip per chip
 Other: None
Memory: 1536 GB (48 x 32 GB 2Rx4 PC4-2666V-R)
Storage: 1 x 1 TB  HDD, 7.2K RPM
Other: None

## Software

OS: SUSE Linux Enterprise Server 12 SP2 (x86_64)
 4.4.120-92.70-default
Compiler: C/C++: Version 18.0.2.199 of Intel C/C++
 Compiler for Linux;
 Fortran: Version 18.0.2.199 of Intel Fortran
 Compiler for Linux
Parallel: No
Firmware: Version 3.1.3e released Jun-2018
File System: xfs
System State: Run level 3 (multi-user)
Base Pointers: 64-bit
Peak Pointers: 64-bit
Other: None

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## Results Table

| Benchmark | Base | | | | | | Peak | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Copies | Seconds | Ratio | Seconds | Ratio | Seconds | Ratio | Copies | Seconds | Ratio | Seconds | Ratio | Seconds | Ratio |
| 503.bwaves_r | 96 | 1046 | 920 | 1046 | 920 | **1046** | **920** | 96 | 1046 | 920 | **1047** | **920** | 1047 | 920 |
| 507.cactuBSSN_r | 96 | 469 | 259 | 469 | 259 | **469** | **259** | 96 | **469** | **259** | 470 | 259 | 469 | 259 |
| 508.namd_r | 96 | 375 | 243 | **376** | **243** | 376 | 242 | 96 | **372** | **245** | 374 | 244 | 372 | 245 |
| 510.parest_r | 96 | **1101** | **228** | 1102 | 228 | 1100 | 228 | 96 | 1104 | 228 | 1107 | 227 | **1105** | **227** |
| 511.povray_r | 96 | **585** | **383** | 588 | 381 | 584 | 384 | 96 | 498 | 450 | **498** | **450** | 504 | 445 |
| 519.lbm_r | 96 | 527 | 192 | 525 | 193 | **526** | **193** | 96 | 492 | 206 | 492 | 206 | **492** | **206** |
| 521.wrf_r | 96 | 539 | 399 | **538** | **400** | 536 | 401 | 96 | **535** | **402** | 535 | 402 | 535 | 402 |
| 526.blender_r | 96 | 412 | 355 | **412** | **355** | 412 | 355 | 96 | 412 | 355 | 412 | 355 | **412** | **355** |
| 527.cam4_r | 96 | 473 | 355 | 473 | 355 | **473** | **355** | 96 | 460 | 365 | **460** | **365** | 461 | 364 |
| 538.imagick_r | 96 | 300 | 797 | **299** | **797** | 299 | 798 | 96 | 300 | 796 | 298 | 801 | **298** | **800** |
| 544.nab_r | 96 | 282 | 572 | 281 | 576 | **281** | **574** | 96 | 283 | 571 | **282** | **573** | 281 | 574 |
| 549.fotonik3d_r | 96 | 1345 | 278 | **1344** | **278** | 1344 | 278 | 96 | **1342** | **279** | 1344 | 278 | 1340 | 279 |
| 554.roms_r | 96 | 816 | 187 | 818 | 186 | **817** | **187** | 96 | **802** | **190** | 801 | 190 | 802 | 190 |

SPECrate2017_fp_base = **350**

SPECrate2017_fp_peak = **357**

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

## Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit'
was used to generate numactl commands to bind each copy to a specific processor.
For details, please see the config file.

## Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

## General Notes

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/cpu2017/lib/ia32:/home/cpu2017/lib/intel64"

Binaries compiled on a system with 1x Intel Core i7-6700K CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3>       /proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:
numactl --interleave=all runcpu <etc>
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown)

**(Continued on next page)**

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## General Notes (Continued)

is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2)
is mitigated in the system as tested and documented.

## Platform Notes

```
BIOS Settings:
Intel HyperThreading Technology set to Enabled
CPU performance set to Enterprise
Power Performance Tuning set to OS Controls
SNC set to Enabled
IMC Interleaving set to 1-way Interleave
Patrol Scrub set to Disabled
 Sysinfo program /home/cpu2017/bin/sysinfo
 Rev: r5797 of 2017-06-14 96c45e4568ad54c135fd618bcc091c0f
 running on linux-9r4j Wed Nov 28 17:35:39 2018

 SUT (System Under Test) info as seen by some common utilities.
 For more information on this section, see
    https://www.spec.org/cpu2017/Docs/config.html#sysinfo

 From /proc/cpuinfo
    model name : Intel(R) Xeon(R) Gold 6146 CPU @ 3.20GHz
       4  "physical id"s (chips)
       96 "processors"
    cores, siblings (Caution: counting these is hw and system dependent. The following
    excerpts from /proc/cpuinfo might not be reliable.  Use with caution.)
       cpu cores : 12
       siblings  : 24
       physical 0: cores 0 1 2 3 4 9 10 16 18 19 25 26
       physical 1: cores 0 1 2 3 4 9 10 16 18 19 25 26
       physical 2: cores 0 1 2 3 4 9 10 16 18 19 25 26
       physical 3: cores 0 1 2 3 4 9 10 16 18 19 25 26

 From lscpu:
       Architecture:          x86_64
       CPU op-mode(s):        32-bit, 64-bit
       Byte Order:            Little Endian
       CPU(s):                96
       On-line CPU(s) list:   0-95
       Thread(s) per core:    2
       Core(s) per socket:    12
       Socket(s):             4
```

(Continued on next page)

Standard Performance Evaluation Corporation (info@spec.org)
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### Platform Notes (Continued)

```
       NUMA node(s):           8
       Vendor ID:              GenuineIntel
       CPU family:             6
       Model:                  85
       Model name:             Intel(R) Xeon(R) Gold 6146 CPU @ 3.20GHz
       Stepping:               4
       CPU MHz:                3522.677
       CPU max MHz:            4200.0000
       CPU min MHz:            1200.0000
       BogoMIPS:               6393.08
       Virtualization:         VT-x
       L1d cache:              32K
       L1i cache:              32K
       L2 cache:               1024K
       L3 cache:               25344K
       NUMA node0 CPU(s):      0-2,5,7,10,48-50,53,55,58
       NUMA node1 CPU(s):      3,4,6,8,9,11,51,52,54,56,57,59
       NUMA node2 CPU(s):      12-14,17,19,22,60-62,65,67,70
       NUMA node3 CPU(s):      15,16,18,20,21,23,63,64,66,68,69,71
       NUMA node4 CPU(s):      24-26,29,31,34,72-74,77,79,82
       NUMA node5 CPU(s):      27,28,30,32,33,35,75,76,78,80,81,83
       NUMA node6 CPU(s):      36-38,41,43,46,84-86,89,91,94
       NUMA node7 CPU(s):      39,40,42,44,45,47,87,88,90,92,93,95
       Flags:                  fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
   pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
   lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc
   aperfmperf eagerfpu pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg
   fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes
   xsave avx f16c rdrand lahf_lm abm 3dnowprefetch ida arat epb invpcid_single pln pts
   dtherm hwp hwp_act_window hwp_epp hwp_pkg_req intel_pt rsb_ctxsw spec_ctrl stibp
   retpoline kaiser tpr_shadow vnmi flexpriority ept vpid fsgsbase tsc_adjust bmi1 hle
   avx2 smep bmi2 erms invpcid rtm cqm mpx avx512f avx512dq rdseed adx smap clflushopt
   clwb avx512cd avx512bw avx512vl xsaveopt xsavec xgetbv1 cqm_llc cqm_occup_llc

 /proc/cpuinfo cache data
    cache size : 25344 KB

 From numactl --hardware  WARNING: a numactl 'node' might or might not correspond to a
 physical chip.
    available: 8 nodes (0-7)
    node 0 cpus: 0 1 2 5 7 10 48 49 50 53 55 58
    node 0 size: 192093 MB
    node 0 free: 191933 MB
    node 1 cpus: 3 4 6 8 9 11 51 52 54 56 57 59
    node 1 size: 193528 MB
    node 1 free: 193339 MB
    node 2 cpus: 12 13 14 17 19 22 60 61 62 65 67 70
```

**(Continued on next page)**

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### Platform Notes (Continued)

```
   node 2 size: 193528 MB
   node 2 free: 193383 MB
   node 3 cpus: 15 16 18 20 21 23 63 64 66 68 69 71
   node 3 size: 193528 MB
   node 3 free: 193237 MB
   node 4 cpus: 24 25 26 29 31 34 72 73 74 77 79 82
   node 4 size: 193528 MB
   node 4 free: 193376 MB
   node 5 cpus: 27 28 30 32 33 35 75 76 78 80 81 83
   node 5 size: 193528 MB
   node 5 free: 193383 MB
   node 6 cpus: 36 37 38 41 43 46 84 85 86 89 91 94
   node 6 size: 193528 MB
   node 6 free: 193364 MB
   node 7 cpus: 39 40 42 44 45 47 87 88 90 92 93 95
   node 7 size: 193525 MB
   node 7 free: 193381 MB
   node distances:
   node   0   1   2   3   4   5   6   7
     0:  10  11  21  21  21  21  21  21
     1:  11  10  21  21  21  21  21  21
     2:  21  21  10  11  21  21  21  21
     3:  21  21  11  10  21  21  21  21
     4:  21  21  21  21  10  11  21  21
     5:  21  21  21  21  11  10  21  21
     6:  21  21  21  21  21  21  10  11
     7:  21  21  21  21  21  21  11  10

 From /proc/meminfo
   MemTotal:       1583913312 kB
   HugePages_Total:        0
   Hugepagesize:        2048 kB

 From /etc/*release* /etc/*version*
   SuSE-release:
      SUSE Linux Enterprise Server 12 (x86_64)
      VERSION = 12
      PATCHLEVEL = 2
      # This file is deprecated and will be removed in a future service pack or release.
      # Please check /etc/os-release for details about this release.
   os-release:
      NAME="SLES"
      VERSION="12-SP2"
      VERSION_ID="12.2"
      PRETTY_NAME="SUSE Linux Enterprise Server 12 SP2"
      ID="sles"
      ANSI_COLOR="0;32"
```

**(Continued on next page)**

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| | | | |
|---|---|---|---|
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| **Test Sponsor:** | Cisco Systems | **Hardware Availability:** | Aug-2017 |
| **Tested by:** | Cisco Systems | **Software Availability:** | Mar-2018 |

## Platform Notes (Continued)

```
        CPE_NAME="cpe:/o:suse:sles:12:sp2"

 uname -a:
    Linux linux-9r4j 4.4.120-92.70-default #1 SMP Wed Mar 14 15:59:43 UTC 2018 (52a83de)
    x86_64 x86_64 x86_64 GNU/Linux

 run-level 3 Oct 20 07:44

 SPEC is set to: /home/cpu2017
    Filesystem      Type  Size  Used Avail Use% Mounted on
    /dev/sda1       xfs   930G  246G  685G  27% /

 Additional information from dmidecode follows.  WARNING: Use caution when you interpret
 this section. The 'dmidecode' program reads system data which is "intended to allow
 hardware to be accurately determined", but the intent may not be met, as there are
 frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
   BIOS Cisco Systems, Inc. C480M5.3.1.3e.0.0613181101 06/13/2018
   Memory:
    48x 0xCE00 M393A4K40BB2-CTD 32 GB 2 rank 2666

 (End of data from sysinfo program)
```

## Compiler Version Notes

```
==============================================================================
  CC   519.lbm_r(base) 538.imagick_r(base, peak) 544.nab_r(base, peak)
------------------------------------------------------------------------------
 icc (ICC) 18.0.2 20180210
 Copyright (C) 1985-2018 Intel Corporation.  All rights reserved.
------------------------------------------------------------------------------


==============================================================================
  CC   519.lbm_r(peak)
------------------------------------------------------------------------------
 icc (ICC) 18.0.2 20180210
 Copyright (C) 1985-2018 Intel Corporation.  All rights reserved.
------------------------------------------------------------------------------


==============================================================================
  CXXC 508.namd_r(base) 510.parest_r(base, peak)
------------------------------------------------------------------------------
 icpc (ICC) 18.0.2 20180210
 Copyright (C) 1985-2018 Intel Corporation.  All rights reserved.
------------------------------------------------------------------------------


==============================================================================
```

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## Compiler Version Notes (Continued)

```
CXXC 508.namd_r(peak)
------------------------------------------------------------------------------
icpc (ICC) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation.  All rights reserved.
------------------------------------------------------------------------------


==============================================================================
 CC   511.povray_r(base) 526.blender_r(base, peak)
------------------------------------------------------------------------------
icpc (ICC) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation.  All rights reserved.
icc (ICC) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation.  All rights reserved.
------------------------------------------------------------------------------


==============================================================================
CC    511.povray_r(peak)
------------------------------------------------------------------------------
icpc (ICC) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation.  All rights reserved.
icc (ICC) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation.  All rights reserved.
------------------------------------------------------------------------------


==============================================================================
 FC  507.cactuBSSN_r(base, peak)
------------------------------------------------------------------------------
icpc (ICC) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation.  All rights reserved.
icc (ICC) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation.  All rights reserved.
ifort (IFORT) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation.  All rights reserved.
------------------------------------------------------------------------------


==============================================================================
 FC  503.bwaves_r(base, peak) 549.fotonik3d_r(base, peak) 554.roms_r(base)
------------------------------------------------------------------------------
ifort (IFORT) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation.  All rights reserved.
------------------------------------------------------------------------------


==============================================================================
FC    554.roms_r(peak)
------------------------------------------------------------------------------
ifort (IFORT) 18.0.2 20180210
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```

**(Continued on next page)**

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## Compiler Version Notes (Continued)

```
--------------------------------------------------------------------------

==========================================================================
  CC  521.wrf_r(base) 527.cam4_r(base)
--------------------------------------------------------------------------
ifort (IFORT) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation.  All rights reserved.
icc (ICC) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation.  All rights reserved.
--------------------------------------------------------------------------

==========================================================================
CC   521.wrf_r(peak) 527.cam4_r(peak)
--------------------------------------------------------------------------
ifort (IFORT) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation.  All rights reserved.
icc (ICC) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation.  All rights reserved.
--------------------------------------------------------------------------
```

## Base Compiler Invocation

C benchmarks:
```
icc -m64 -std=c11
```

C++ benchmarks:
```
icpc -m64
```

Fortran benchmarks:
```
ifort -m64
```

Benchmarks using both Fortran and C:
```
ifort -m64 icc -m64 -std=c11
```

Benchmarks using both C and C++:
```
icpc -m64 icc -m64 -std=c11
```

Benchmarks using Fortran, C, and C++:
```
icpc -m64 icc -m64 -std=c11 ifort -m64
```

## Base Portability Flags

503.bwaves_r: `-DSPEC_LP64`

**(Continued on next page)**

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## Base Portability Flags (Continued)

507.cactuBSSN_r: `-DSPEC_LP64`

508.namd_r: `-DSPEC_LP64`

510.parest_r: `-DSPEC_LP64`

511.povray_r: `-DSPEC_LP64`

519.lbm_r: `-DSPEC_LP64`

521.wrf_r: `-DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian`

526.blender_r: `-DSPEC_LP64 -DSPEC_LINUX -funsigned-char`

527.cam4_r: `-DSPEC_LP64 -DSPEC_CASE_FLAG`

538.imagick_r: `-DSPEC_LP64`

544.nab_r: `-DSPEC_LP64`

549.fotonik3d_r: `-DSPEC_LP64`

554.roms_r: `-DSPEC_LP64`

## Base Optimization Flags

C benchmarks:

`-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=3`

C++ benchmarks:

`-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=3`

Fortran benchmarks:

`-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=3 -auto -nostandard-realloc-lhs`

Benchmarks using both Fortran and C:

`-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=3 -auto -nostandard-realloc-lhs`

Benchmarks using both C and C++:

`-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=3`

Benchmarks using Fortran, C, and C++:

`-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=3 -auto -nostandard-realloc-lhs`

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## Peak Compiler Invocation

C benchmarks:
```
icc -m64 -std=c11
```

C++ benchmarks:
```
icpc -m64
```

Fortran benchmarks:
```
ifort -m64
```

Benchmarks using both Fortran and C:
```
ifort -m64 icc -m64 -std=c11
```

Benchmarks using both C and C++:
```
icpc -m64 icc -m64 -std=c11
```

Benchmarks using Fortran, C, and C++:
```
icpc -m64 icc -m64 -std=c11 ifort -m64
```

## Peak Portability Flags

```
Same as Base Portability Flags
```

## Peak Optimization Flags

C benchmarks:

519.lbm_r: `-prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=3`

538.imagick_r: `-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=3`

544.nab_r: `Same as 538.imagick_r`

C++ benchmarks:

508.namd_r: `-prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=3`

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# Peak Optimization Flags (Continued)

510.parest_r: `-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=3`

Fortran benchmarks:

503.bwaves_r: `-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=3 -auto -nostandard-realloc-lhs`

549.fotonik3d_r: `Same as 503.bwaves_r`

554.roms_r: `-prof-gen`(pass 1) `-prof-use`(pass 2) `-ipo -xCORE-AVX2 -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=3 -auto -nostandard-realloc-lhs`

Benchmarks using both Fortran and C:
`-prof-gen`(pass 1) `-prof-use`(pass 2) `-ipo -xCORE-AVX2 -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=3 -auto -nostandard-realloc-lhs`

Benchmarks using both C and C++:

511.povray_r: `-prof-gen`(pass 1) `-prof-use`(pass 2) `-ipo -xCORE-AVX2 -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=3`

526.blender_r: `-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=3`

Benchmarks using Fortran, C, and C++:
`-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=3 -auto -nostandard-realloc-lhs`

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.2017-12-21.html
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revH.html

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.2017-12-21.xml
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revH.xml

Standard Performance Evaluation Corporation (info@spec.org)

https://www.spec.org/

# SPEC CPU2017 Floating Point Rate Result

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## Cisco Systems

Cisco UCS C480 M5 (Intel Xeon Gold 6146 3.20 GHz)

SPECrate2017_fp_base =   350

SPECrate2017_fp_peak =   357

**CPU2017 License:** 9019

**Test Sponsor:** Cisco Systems

**Tested by:** Cisco Systems

**Test Date:** Nov-2018

**Hardware Availability:** Aug-2017

**Software Availability:** Mar-2018

For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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