



SPEC CPU®2017 Floating Point Speed Result

Copyright 2017-2019 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS B200 M5 (Intel Xeon Gold 6130, 2.10 GHz)

SPECspeed®2017_fp_base = 105

SPECspeed®2017_fp_peak = 106

CPU2017 License: 9019

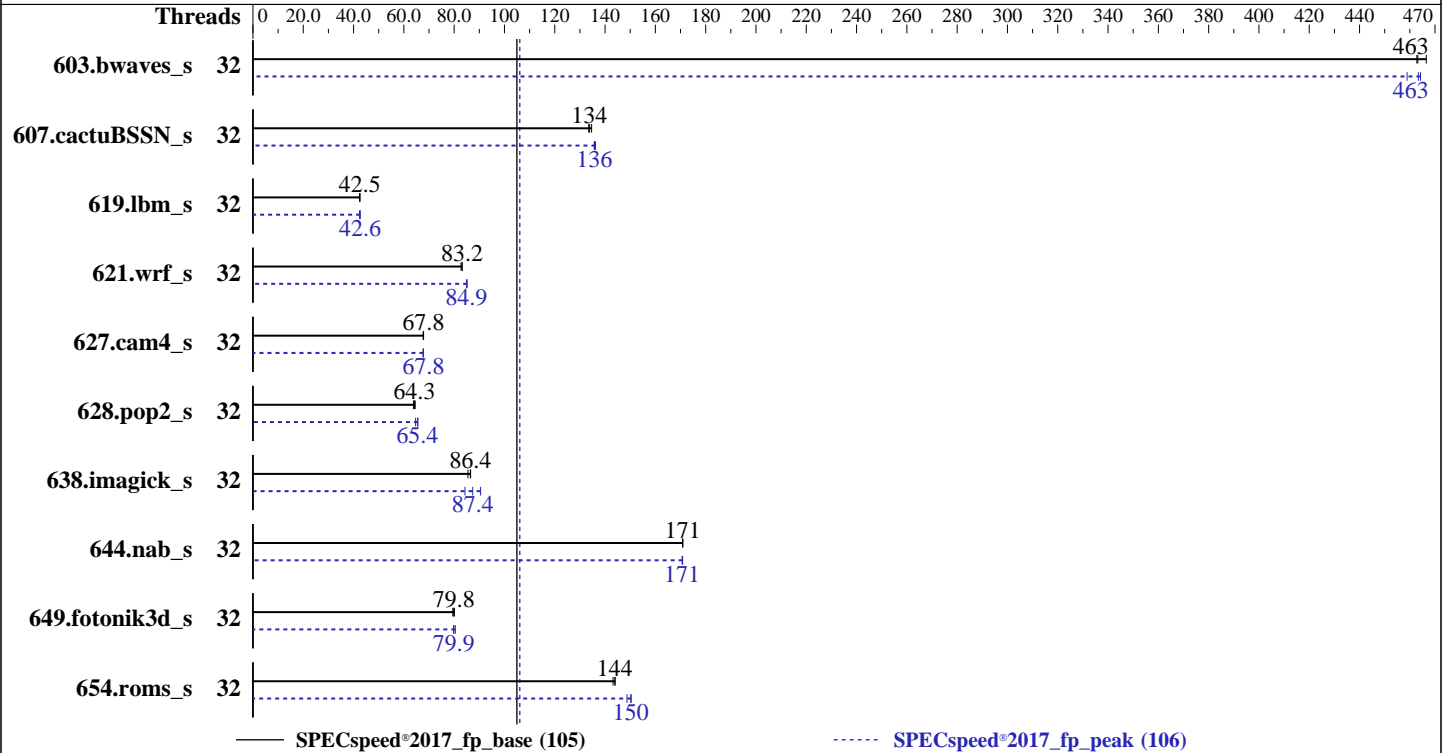
Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Jun-2018

Hardware Availability: Aug-2017

Software Availability: Mar-2018



Hardware

CPU Name: Intel Xeon Gold 6130
 Max MHz: 3700
 Nominal: 2100
 Enabled: 32 cores, 2 chips
 Orderable: 1,2 Chips
 Cache L1: 32 KB I + 32 KB D on chip per core
 L2: 1 MB I+D on chip per core
 L3: 22 MB I+D on chip per chip
 Other: None
 Memory: 384 GB (24 x 16 GB 2Rx4 PC4-2666V-R)
 Storage: 1 x 240 GB M.2 SATA SSD
 Other: None

Software

OS: SUSE Linux Enterprise Server 12 SP2 (x86_64) 4.4.103-92.56-default
 Compiler: C/C++: Version 18.0.2.199 of Intel C/C++ Compiler for Linux;
 Fortran: Version 18.0.2.199 of Intel Fortran Compiler for Linux
 Parallel: Yes
 Firmware: Version 3.2.3c released Mar-2018
 File System: xfs
 System State: Run level 3 (multi-user)
 Base Pointers: 64-bit
 Peak Pointers: 64-bit
 Other: None
 Power Management: --



SPEC CPU®2017 Floating Point Speed Result

Copyright 2017-2019 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS B200 M5 (Intel Xeon Gold 6130, 2.10 GHz)

SPECSpeed®2017_fp_base = 105

SPECSpeed®2017_fp_peak = 106

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Jun-2018
Hardware Availability: Aug-2017
Software Availability: Mar-2018

Results Table

Benchmark	Base						Peak							
	Threads	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Threads	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
603.bwaves_s	32	126	467	127	463	<u>127</u>	<u>463</u>	32	<u>127</u>	<u>463</u>	127	464	129	459
607.cactuBSSN_s	32	124	135	<u>125</u>	<u>134</u>	125	133	32	123	136	122	136	<u>123</u>	<u>136</u>
619.lbm_s	32	123	42.5	<u>123</u>	<u>42.5</u>	123	42.5	32	<u>123</u>	<u>42.6</u>	124	42.4	123	42.6
621.wrf_s	32	160	82.7	159	83.2	<u>159</u>	<u>83.2</u>	32	<u>156</u>	<u>84.9</u>	156	84.9	155	85.2
627.cam4_s	32	131	67.8	<u>131</u>	<u>67.8</u>	131	67.7	32	<u>131</u>	<u>67.8</u>	131	67.8	131	67.6
628.pop2_s	32	186	63.8	<u>185</u>	<u>64.3</u>	184	64.5	32	181	65.6	<u>182</u>	<u>65.4</u>	184	64.7
638.imagick_s	32	169	85.5	167	86.5	<u>167</u>	<u>86.4</u>	32	159	90.5	171	84.3	<u>165</u>	<u>87.4</u>
644.nab_s	32	102	171	<u>102</u>	<u>171</u>	102	171	32	<u>102</u>	<u>171</u>	102	171	102	171
649.fotonik3d_s	32	114	80.1	115	79.5	<u>114</u>	<u>79.8</u>	32	<u>114</u>	<u>79.9</u>	113	80.5	114	79.8
654.roms_s	32	109	144	<u>109</u>	<u>144</u>	110	143	32	105	150	<u>105</u>	<u>150</u>	106	149

SPECSpeed®2017_fp_base = **105**

SPECSpeed®2017_fp_peak = **106**

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

General Notes

Environment variables set by runcpu before the start of the run:

KMP_AFFINITY = "granularity=fine,compact"

LD_LIBRARY_PATH = "/home/cpu2017/lib/ia32:/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-32:/home/cpu2017/je5.0.1-64"

OMP_STACKSIZE = "192M"

Binaries compiled on a system with 1x Intel Core i7-4790 CPU + 32GB RAM

memory using Redhat Enterprise Linux 7.4

Transparent Huge Pages enabled by default

Prior to runcpu invocation

Filesystem page cache synced and cleared with:

```
sync; echo 3> /proc/sys/vm/drop_caches
```

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

Platform Notes

BIOS Settings:

Intel HyperThreading Technology set to Disabled

(Continued on next page)



SPEC CPU®2017 Floating Point Speed Result

Copyright 2017-2019 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS B200 M5 (Intel Xeon Gold 6130, 2.10 GHz)

SPECspeed®2017_fp_base = 105

SPECspeed®2017_fp_peak = 106

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Jun-2018
Hardware Availability: Aug-2017
Software Availability: Mar-2018

Platform Notes (Continued)

CPU performance set to Enterprise
Power Performance Tuning set to OS Controls
SNC set to Disabled
Patrol Scrub set to Disabled
Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r5797 of 2017-06-14 96c45e4568ad54c135fd618bcc091c0f
running on linux-qc7k Thu Jun 7 01:32:38 2018

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
<https://www.spec.org/cpu2017/Docs/config.html#sysinfo>

```
From /proc/cpuinfo
model name : Intel(R) Xeon(R) Gold 6130 CPU @ 2.10GHz
 2 "physical id"s (chips)
 32 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following
excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
  cpu cores : 16
  siblings  : 16
 physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
 physical 1: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
```

```
From lscpu:
Architecture:          x86_64
CPU op-mode(s):        32-bit, 64-bit
Byte Order:             Little Endian
CPU(s):                 32
On-line CPU(s) list:   0-31
Thread(s) per core:    1
Core(s) per socket:    16
Socket(s):              2
NUMA node(s):          2
Vendor ID:              GenuineIntel
CPU family:             6
Model:                  85
Model name:             Intel(R) Xeon(R) Gold 6130 CPU @ 2.10GHz
Stepping:               4
CPU MHz:                3219.870
CPU max MHz:           3700.0000
CPU min MHz:           1000.0000
BogoMIPS:               4199.97
Virtualization:        VT-x
L1d cache:              32K
L1i cache:              32K
L2 cache:               1024K
L3 cache:               22528K
```

(Continued on next page)



SPEC CPU®2017 Floating Point Speed Result

Copyright 2017-2019 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS B200 M5 (Intel Xeon Gold 6130, 2.10 GHz)

SPECspeed®2017_fp_base = 105

SPECspeed®2017_fp_peak = 106

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Jun-2018
Hardware Availability: Aug-2017
Software Availability: Mar-2018

Platform Notes (Continued)

```
NUMA node0 CPU(s):      0-15
NUMA node1 CPU(s):      16-31
Flags:                   fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc
aperfmpperf eagerfpu pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg
fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes
xsave avx f16c rdrand lahf_lm abm 3dnowprefetch ida arat epb invpcid_single pln pts
dtherm hwp hwp_act_window hwp_epp hwp_pkg_req intel_pt spec_ctrl kaiser tpr_shadow
vnm flexpriority ept vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid
rtm cqm mpx avx512f avx512dq rdseed adx smap clflushopt clwb avx512cd avx512bw
avx512vl xsaveopt xsavec xgetbv1 cqm_llc cqm_occup_llc
```

```
/proc/cpuinfo cache data
cache size : 22528 KB
```

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.

```
available: 2 nodes (0-1)
node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
node 0 size: 192074 MB
node 0 free: 191709 MB
node 1 cpus: 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31
node 1 size: 193504 MB
node 1 free: 193152 MB
node distances:
node  0  1
  0:  10  21
  1:  21  10
```

```
From /proc/meminfo
MemTotal:      394832488 kB
HugePages_Total:      0
Hugepagesize:    2048 kB
```

From /etc/*release* /etc/*version*

```
SuSE-release:
SUSE Linux Enterprise Server 12 (x86_64)
VERSION = 12
PATCHLEVEL = 2
# This file is deprecated and will be removed in a future service pack or release.
# Please check /etc/os-release for details about this release.
os-release:
NAME="SLES"
VERSION="12-SP2"
VERSION_ID="12.2"
PRETTY_NAME="SUSE Linux Enterprise Server 12 SP2"
```

(Continued on next page)



SPEC CPU®2017 Floating Point Speed Result

Copyright 2017-2019 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS B200 M5 (Intel Xeon Gold 6130, 2.10 GHz)

SPECspeed®2017_fp_base = 105

SPECspeed®2017_fp_peak = 106

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Jun-2018
Hardware Availability: Aug-2017
Software Availability: Mar-2018

Platform Notes (Continued)

```
ID="sles"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:12:sp2"
```

```
uname -a:
Linux linux-qc7k 4.4.103-92.56-default #1 SMP Wed Dec 27 16:24:31 UTC 2017 (2fd2155)
x86_64 x86_64 x86_64 GNU/Linux
```

```
run-level 3 Jan 1 03:43
```

```
SPEC is set to: /home/cpu2017
Filesystem      Type  Size  Used Avail Use% Mounted on
/dev/sdal        xfs   224G   64G  160G  29% /
```

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

```
BIOS Cisco Systems, Inc. B200M5.3.2.3c.0.0307181316 03/07/2018
Memory:
24x 0xCE00 M393A2G40EB2-CTD 16 GB 2 rank 2666
```

(End of data from sysinfo program)

Compiler Version Notes

```
=====
C | 619.lbm_s(base, peak) 638.imagick_s(base, peak)
  | 644.nab_s(base, peak)
-----
```

```
icc (ICC) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
-----
```

```
=====
C++, C, Fortran | 607.cactuBSSN_s(base, peak)
-----
```

```
icpc (ICC) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
icc (ICC) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
ifort (IFORT) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
-----
=====
```

(Continued on next page)



SPEC CPU®2017 Floating Point Speed Result

Copyright 2017-2019 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS B200 M5 (Intel Xeon Gold 6130, 2.10 GHz)

SPECspeed®2017_fp_base = 105

SPECspeed®2017_fp_peak = 106

CPU2017 License: 9019

Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Jun-2018

Hardware Availability: Aug-2017

Software Availability: Mar-2018

Compiler Version Notes (Continued)

```
Fortran          | 603.bwaves_s(base, peak) 649.fotonik3d_s(base, peak)
                  | 654.roms_s(base, peak)
```

```
-----
ifort (IFORT) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
```

```
=====
Fortran, C      | 621.wrf_s(base, peak) 627.cam4_s(base, peak)
                  | 628.pop2_s(base, peak)
```

```
-----
ifort (IFORT) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
icc (ICC) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
```

Base Compiler Invocation

C benchmarks:

```
icc -m64 -std=c11
```

Fortran benchmarks:

```
ifort -m64
```

Benchmarks using both Fortran and C:

```
ifort -m64 icc -m64 -std=c11
```

Benchmarks using Fortran, C, and C++:

```
icpc -m64 icc -m64 -std=c11 ifort -m64
```

Base Portability Flags

```
603.bwaves_s: -DSPEC_LP64
607.cactuBSSN_s: -DSPEC_LP64
619.lbm_s: -DSPEC_LP64
621.wrf_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
627.cam4_s: -DSPEC_LP64 -DSPEC_CASE_FLAG
628.pop2_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
-assume byterecl
638.imagick_s: -DSPEC_LP64
644.nab_s: -DSPEC_LP64
649.fotonik3d_s: -DSPEC_LP64
```

(Continued on next page)



SPEC CPU®2017 Floating Point Speed Result

Copyright 2017-2019 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS B200 M5 (Intel Xeon Gold 6130,
2.10 GHz)

SPECspeed®2017_fp_base = 105

SPECspeed®2017_fp_peak = 106

CPU2017 License: 9019

Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Jun-2018

Hardware Availability: Aug-2017

Software Availability: Mar-2018

Base Portability Flags (Continued)

654.roms_s: -DSPEC_LP64

Base Optimization Flags

C benchmarks:

-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp -DSPEC_OPENMP

Fortran benchmarks:

-DSPEC_OPENMP -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp
-nostandard-realloc-lhs -align array32byte

Benchmarks using both Fortran and C:

-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp -DSPEC_OPENMP
-nostandard-realloc-lhs -align array32byte

Benchmarks using Fortran, C, and C++:

-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp -DSPEC_OPENMP
-nostandard-realloc-lhs -align array32byte

Peak Compiler Invocation

C benchmarks:

icc -m64 -std=c11

Fortran benchmarks:

ifort -m64

Benchmarks using both Fortran and C:

ifort -m64 icc -m64 -std=c11

Benchmarks using Fortran, C, and C++:

icpc -m64 icc -m64 -std=c11 ifort -m64



SPEC CPU®2017 Floating Point Speed Result

Copyright 2017-2019 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS B200 M5 (Intel Xeon Gold 6130, 2.10 GHz)

SPECspeed®2017_fp_base = 105

SPECspeed®2017_fp_peak = 106

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Jun-2018
Hardware Availability: Aug-2017
Software Availability: Mar-2018

Peak Portability Flags

Same as Base Portability Flags

Peak Optimization Flags

C benchmarks:

```
619.lbm_s: -prof-gen(pass 1) -prof-use(pass 2) -O2 -xCORE-AVX512  
-qopt-prefetch -ipo -O3 -ffinite-math-only -no-prec-div  
-qopt-mem-layout-trans=3 -DSPEC_SUPPRESS_OPENMP -qopenmp  
-DSPEC_OPENMP
```

```
638.imagick_s: -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch  
-ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp  
-DSPEC_OPENMP
```

644.nab_s: Same as 638.imagick_s

Fortran benchmarks:

```
-prof-gen(pass 1) -prof-use(pass 2) -DSPEC_SUPPRESS_OPENMP  
-DSPEC_OPENMP -O2 -xCORE-AVX512 -qopt-prefetch -ipo -O3  
-ffinite-math-only -no-prec-div -qopt-mem-layout-trans=3 -qopenmp  
-nostandard-realloc-lhs -align array32byte
```

Benchmarks using both Fortran and C:

```
621.wrf_s: -prof-gen(pass 1) -prof-use(pass 2) -O2 -xCORE-AVX512  
-qopt-prefetch -ipo -O3 -ffinite-math-only -no-prec-div  
-qopt-mem-layout-trans=3 -DSPEC_SUPPRESS_OPENMP -qopenmp  
-DSPEC_OPENMP -nostandard-realloc-lhs -align array32byte
```

```
627.cam4_s: -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch  
-ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp  
-DSPEC_OPENMP -nostandard-realloc-lhs -align array32byte
```

628.pop2_s: Same as 621.wrf_s

Benchmarks using Fortran, C, and C++:

```
-prof-gen(pass 1) -prof-use(pass 2) -O2 -xCORE-AVX512 -qopt-prefetch  
-ipo -O3 -ffinite-math-only -no-prec-div -qopt-mem-layout-trans=3  
-DSPEC_SUPPRESS_OPENMP -qopenmp -DSPEC_OPENMP -nostandard-realloc-lhs  
-align array32byte
```




SPEC CPU®2017 Floating Point Speed Result

Copyright 2017-2019 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS B200 M5 (Intel Xeon Gold 6130, 2.10 GHz)

SPECspeed®2017_fp_base = 105

SPECspeed®2017_fp_peak = 106

CPU2017 License: 9019

Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Jun-2018

Hardware Availability: Aug-2017

Software Availability: Mar-2018

The flags files that were used to format this result can be browsed at

<http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.2018-06-13.html>

<http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revH.html>

You can also download the XML flags sources by saving the following links:

<http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.2018-06-13.xml>

<http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revH.xml>

SPEC CPU and SPECspeed are registered trademarks of the Standard Performance Evaluation Corporation. All other brand and product names appearing in this result are trademarks or registered trademarks of their respective holders.

For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.0.2 on 2018-06-07 01:32:37-0400.

Report generated on 2019-12-13 18:56:33 by CPU2017 PDF formatter v6255.

Originally published on 2018-06-26.