



# SPEC CPU®2017 Floating Point Rate Result

Copyright 2017-2019 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS B200 M5 (Intel Xeon Gold 6148, 2.40 GHz)

SPECrate®2017\_fp\_base = 204

SPECrate®2017\_fp\_peak = 206

CPU2017 License: 9019

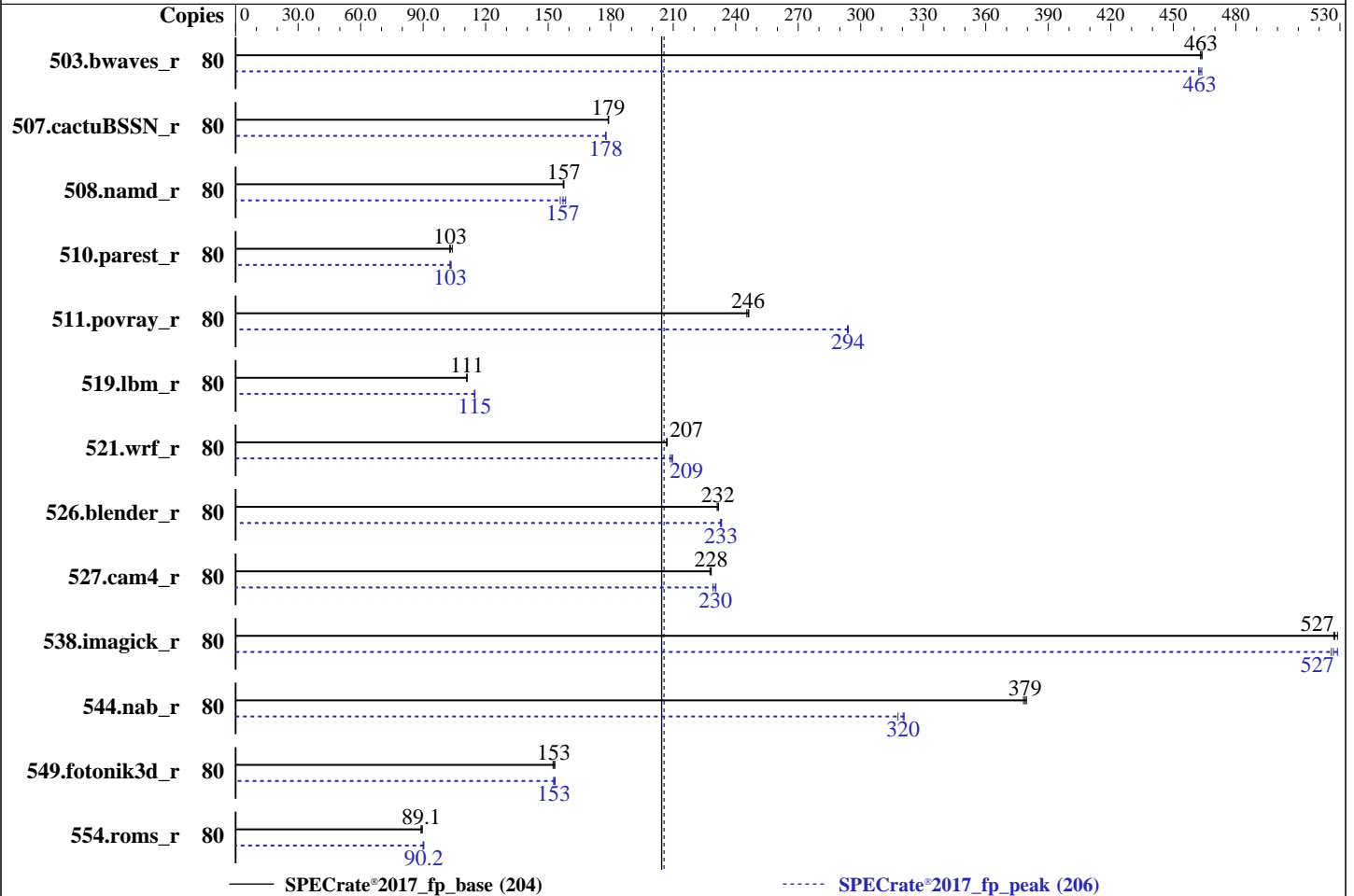
Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: May-2018

Hardware Availability: Aug-2017

Software Availability: Mar-2018



### Hardware

CPU Name: Intel Xeon Gold 6148  
 Max MHz: 3700  
 Nominal: 2400  
 Enabled: 40 cores, 2 chips, 2 threads/core  
 Orderable: 1,2 Chips  
 Cache L1: 32 KB I + 32 KB D on chip per core  
 L2: 1 MB I+D on chip per core  
 L3: 27.5 MB I+D on chip per chip  
 Other: None  
 Memory: 384 GB (24 x 16 GB 2Rx4 PC4-2666V-R)  
 Storage: 1 x 240 GB M.2 SATA SSD  
 Other: None

### Software

OS: SUSE Linux Enterprise Server 12 SP2 (x86\_64) 4.4.103-92.56-default  
 Compiler: C/C++: Version 18.0.2.199 of Intel C/C++ Compiler for Linux;  
 Fortran: Version 18.0.2.199 of Intel Fortran Compiler for Linux  
 Parallel: No  
 Firmware: Version 3.2.3c released Mar-2018  
 File System: xfs  
 System State: Run level 3 (multi-user)  
 Base Pointers: 64-bit  
 Peak Pointers: 64-bit  
 Other: None  
 Power Management: --



# SPEC CPU®2017 Floating Point Rate Result

Copyright 2017-2019 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS B200 M5 (Intel Xeon Gold 6148, 2.40 GHz)

SPECrate®2017\_fp\_base = 204

SPECrate®2017\_fp\_peak = 206

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems

**Test Date:** May-2018  
**Hardware Availability:** Aug-2017  
**Software Availability:** Mar-2018

## Results Table

Benchmark	Base							Peak						
	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
503.bwaves_r	80	<b>1732</b>	<b>463</b>	1730	464	1732	463	80	<b>1734</b>	<b>463</b>	1730	464	1736	462
507.cactuBSSN_r	80	566	179	566	179	<b>566</b>	<b>179</b>	80	<b>570</b>	<b>178</b>	570	178	570	178
508.namd_r	80	483	157	<b>483</b>	<b>157</b>	482	158	80	<b>484</b>	<b>157</b>	480	158	488	156
510.parest_r	80	2013	104	2036	103	<b>2031</b>	<b>103</b>	80	2023	103	2034	103	<b>2031</b>	<b>103</b>
511.povray_r	80	<b>759</b>	<b>246</b>	761	245	758	246	80	<b>636</b>	<b>294</b>	636	294	635	294
519.lbm_r	80	759	111	760	111	<b>760</b>	<b>111</b>	80	736	115	734	115	<b>734</b>	<b>115</b>
521.wrf_r	80	865	207	<b>865</b>	<b>207</b>	867	207	80	855	210	859	209	<b>856</b>	<b>209</b>
526.blender_r	80	527	231	<b>526</b>	<b>232</b>	526	232	80	<b>523</b>	<b>233</b>	522	233	524	233
527.cam4_r	80	615	228	613	228	<b>613</b>	<b>228</b>	80	607	231	<b>608</b>	<b>230</b>	611	229
538.imagick_r	80	378	527	376	529	<b>377</b>	<b>527</b>	80	376	529	378	526	<b>378</b>	<b>527</b>
544.nab_r	80	356	378	355	380	<b>355</b>	<b>379</b>	80	420	321	424	318	<b>420</b>	<b>320</b>
549.fotonik3d_r	80	<b>2041</b>	<b>153</b>	2035	153	2047	152	80	2033	153	2042	153	<b>2041</b>	<b>153</b>
554.roms_r	80	1427	89.1	1419	89.6	<b>1427</b>	<b>89.1</b>	80	1413	89.9	<b>1409</b>	<b>90.2</b>	1408	90.3

SPECrate®2017\_fp\_base = 204

SPECrate®2017\_fp\_peak = 206

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

## Submit Notes

The taskset mechanism was used to bind copies to processors. The config file option 'submit' was used to generate taskset commands to bind each copy to a specific processor. For details, please see the config file.

## Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

## General Notes

Environment variables set by runcpu before the start of the run:

LD\_LIBRARY\_PATH = "/home/cpu2017/lib/ia32:/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-32:/home/cpu2017/je5.0.1-64"

Binaries compiled on a system with 1x Intel Core i7-4790 CPU + 32GB RAM

memory using Redhat Enterprise Linux 7.4

Transparent Huge Pages enabled by default

Prior to runcpu invocation

Filesystem page cache synced and cleared with:

```
sync; echo 3> /proc/sys/vm/drop_caches
```

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

(Continued on next page)



# SPEC CPU®2017 Floating Point Rate Result

Copyright 2017-2019 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS B200 M5 (Intel Xeon Gold 6148, 2.40 GHz)

SPECrate®2017\_fp\_base = 204

SPECrate®2017\_fp\_peak = 206

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems

**Test Date:** May-2018  
**Hardware Availability:** Aug-2017  
**Software Availability:** Mar-2018

### General Notes (Continued)

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

### Platform Notes

BIOS Settings:

Intel HyperThreading Technology set to Enabled  
CPU performance set to Enterprise  
Power Performance Tuning set to OS Controls  
SNC set to Enabled  
IMC Interleaving set to 1-way Interleave  
Patrol Scrub set to Disabled  
Sysinfo program /home/cpu2017/bin/sysinfo  
Rev: r5797 of 2017-06-14 96c45e4568ad54c135fd618bcc091c0f  
running on linux-mys2 Wed May 9 01:35:43 2018

SUT (System Under Test) info as seen by some common utilities.

For more information on this section, see  
<https://www.spec.org/cpu2017/Docs/config.html#sysinfo>

From /proc/cpuinfo

```
model name      : Intel(R) Xeon(R) Gold 6148 CPU @ 2.40GHz
 2 "physical id"s (chips)
 80 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following
excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores      : 20
siblings       : 40
physical 0:    cores 0 1 2 3 4 8 9 10 11 12 16 17 18 19 20 24 25 26 27 28
physical 1:    cores 0 1 2 3 4 8 9 10 11 12 16 17 18 19 20 24 25 26 27 28
```

From lscpu:

```
Architecture:    x86_64
CPU op-mode(s):  32-bit, 64-bit
Byte Order:      Little Endian
CPU(s):          80
On-line CPU(s) list:  0-79
Thread(s) per core:  2
Core(s) per socket:  20
Socket(s):       2
NUMA node(s):    4
Vendor ID:       GenuineIntel
CPU family:      6
Model:          85
Model name:      Intel(R) Xeon(R) Gold 6148 CPU @ 2.40GHz
```

(Continued on next page)



# SPEC CPU®2017 Floating Point Rate Result

Copyright 2017-2019 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS B200 M5 (Intel Xeon Gold 6148, 2.40 GHz)

SPECrate®2017\_fp\_base = 204

SPECrate®2017\_fp\_peak = 206

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems

**Test Date:** May-2018  
**Hardware Availability:** Aug-2017  
**Software Availability:** Mar-2018

### Platform Notes (Continued)

```
Stepping: 4
CPU MHz: 1000.000
CPU max MHz: 2401.0000
CPU min MHz: 1000.0000
BogoMIPS: 4800.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 28160K
NUMA node0 CPU(s): 0-2,5,6,10-12,15,16,40-42,45,46,50-52,55,56
NUMA node1 CPU(s): 3,4,7-9,13,14,17-19,43,44,47-49,53,54,57-59
NUMA node2 CPU(s): 20-22,25,26,30-32,35,36,60-62,65,66,70-72,75,76
NUMA node3 CPU(s): 23,24,27-29,33,34,37-39,63,64,67-69,73,74,77-79
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc
aperfmpperf eagerfpu pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg
fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes
xsave avx f16c rdrand lahf_lm abm 3dnowprefetch ida arat epb invpcid_single pln pts
dtherm intel_pt spec_ctrl kaiser tpr_shadow vnmi flexpriority ept vpid fsgsbase
tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm cqm mpx avx512f avx512dq rdseed
adx smap clflushopt clwb avx512cd avx512bw avx512vl xsaveopt xsavec xgetbv1 cqm_llc
cqm_occup_llc
```

```
/proc/cpuinfo cache data
cache size : 28160 KB
```

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.

```
available: 4 nodes (0-3)
node 0 cpus: 0 1 2 5 6 10 11 12 15 16 40 41 42 45 46 50 51 52 55 56
node 0 size: 95320 MB
node 0 free: 95139 MB
node 1 cpus: 3 4 7 8 9 13 14 17 18 19 43 44 47 48 49 53 54 57 58 59
node 1 size: 96753 MB
node 1 free: 96486 MB
node 2 cpus: 20 21 22 25 26 30 31 32 35 36 60 61 62 65 66 70 71 72 75 76
node 2 size: 96753 MB
node 2 free: 96579 MB
node 3 cpus: 23 24 27 28 29 33 34 37 38 39 63 64 67 68 69 73 74 77 78 79
node 3 size: 96750 MB
node 3 free: 96030 MB
node distances:
node 0 1 2 3
0: 10 11 21 21
1: 11 10 21 21
```

(Continued on next page)



# SPEC CPU®2017 Floating Point Rate Result

Copyright 2017-2019 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS B200 M5 (Intel Xeon Gold 6148, 2.40 GHz)

SPECrate®2017\_fp\_base = 204

SPECrate®2017\_fp\_peak = 206

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems

**Test Date:** May-2018  
**Hardware Availability:** Aug-2017  
**Software Availability:** Mar-2018

### Platform Notes (Continued)

```
2: 21 21 10 11
3: 21 21 11 10
```

```
From /proc/meminfo
MemTotal:      394831972 kB
HugePages_Total:      0
Hugepagesize:    2048 kB
```

```
/usr/bin/lsb_release -d
SUSE Linux Enterprise Server 12 SP2
```

```
From /etc/*release* /etc/*version*
SuSE-release:
  SUSE Linux Enterprise Server 12 (x86_64)
  VERSION = 12
  PATCHLEVEL = 2
  # This file is deprecated and will be removed in a future service pack or release.
  # Please check /etc/os-release for details about this release.
os-release:
  NAME="SLES"
  VERSION="12-SP2"
  VERSION_ID="12.2"
  PRETTY_NAME="SUSE Linux Enterprise Server 12 SP2"
  ID="sles"
  ANSI_COLOR="0;32"
  CPE_NAME="cpe:/o:suse:sles:12:sp2"
```

```
uname -a:
Linux linux-mys2 4.4.103-92.56-default #1 SMP Wed Dec 27 16:24:31 UTC 2017 (2fd2155)
x86_64 x86_64 x86_64 GNU/Linux
```

```
run-level 3 Jan 30 16:23
```

```
SPEC is set to: /home/cpu2017
Filesystem      Type  Size  Used Avail Use% Mounted on
/dev/sda3        xfs   182G  114G   69G  63% /home
```

Additional information from dmidecode follows. **WARNING:** Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

BIOS Cisco Systems, Inc. B200M5.3.2.3c.0.0307181316 03/07/2018

Memory:  
24x 0xCE00 M393A2G40EB2-CTD 16 GB 2 rank 2666

(End of data from sysinfo program)



# SPEC CPU®2017 Floating Point Rate Result

Copyright 2017-2019 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS B200 M5 (Intel Xeon Gold 6148, 2.40 GHz)

SPECrate®2017\_fp\_base = 204

SPECrate®2017\_fp\_peak = 206

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems

**Test Date:** May-2018  
**Hardware Availability:** Aug-2017  
**Software Availability:** Mar-2018

### Compiler Version Notes

=====  
C | 519.lbm\_r(base, peak) 538.imagick\_r(base, peak)  
544.nab\_r(base, peak)

icc (ICC) 18.0.2 20180210  
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.  
-----

=====  
C++ | 508.namd\_r(base, peak) 510.parest\_r(base, peak)  
-----

icpc (ICC) 18.0.2 20180210  
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.  
-----

=====  
C++, C | 511.povray\_r(base, peak) 526.blender\_r(base, peak)  
-----

icpc (ICC) 18.0.2 20180210  
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.  
icc (ICC) 18.0.2 20180210  
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.  
-----

=====  
C++, C, Fortran | 507.cactuBSSN\_r(base, peak)  
-----

icpc (ICC) 18.0.2 20180210  
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.  
icc (ICC) 18.0.2 20180210  
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.  
ifort (IFORT) 18.0.2 20180210  
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.  
-----

=====  
Fortran | 503.bwaves\_r(base, peak) 549.fotonik3d\_r(base, peak)  
554.roms\_r(base, peak)

ifort (IFORT) 18.0.2 20180210  
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.  
-----

=====  
Fortran, C | 521.wrf\_r(base, peak) 527.cam4\_r(base, peak)  
-----

ifort (IFORT) 18.0.2 20180210

(Continued on next page)



# SPEC CPU®2017 Floating Point Rate Result

Copyright 2017-2019 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS B200 M5 (Intel Xeon Gold 6148, 2.40 GHz)

SPECrate®2017\_fp\_base = 204

SPECrate®2017\_fp\_peak = 206

**CPU2017 License:** 9019

**Test Sponsor:** Cisco Systems

**Tested by:** Cisco Systems

**Test Date:** May-2018

**Hardware Availability:** Aug-2017

**Software Availability:** Mar-2018

## Compiler Version Notes (Continued)

Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

icc (ICC) 18.0.2 20180210

Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

## Base Compiler Invocation

C benchmarks:

```
icc -m64 -std=c11
```

C++ benchmarks:

```
icpc -m64
```

Fortran benchmarks:

```
ifort -m64
```

Benchmarks using both Fortran and C:

```
ifort -m64 icc -m64 -std=c11
```

Benchmarks using both C and C++:

```
icpc -m64 icc -m64 -std=c11
```

Benchmarks using Fortran, C, and C++:

```
icpc -m64 icc -m64 -std=c11 ifort -m64
```

## Base Portability Flags

```
503.bwaves_r: -DSPEC_LP64
```

```
507.cactuBSSN_r: -DSPEC_LP64
```

```
508.namd_r: -DSPEC_LP64
```

```
510.parest_r: -DSPEC_LP64
```

```
511.povray_r: -DSPEC_LP64
```

```
519.lbm_r: -DSPEC_LP64
```

```
521.wrf_r: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
```

```
526.blender_r: -DSPEC_LP64 -DSPEC_LINUX -funsigned-char
```

```
527.cam4_r: -DSPEC_LP64 -DSPEC_CASE_FLAG
```

```
538.imagick_r: -DSPEC_LP64
```

```
544.nab_r: -DSPEC_LP64
```

```
549.fotonik3d_r: -DSPEC_LP64
```

```
554.roms_r: -DSPEC_LP64
```



# SPEC CPU®2017 Floating Point Rate Result

Copyright 2017-2019 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS B200 M5 (Intel Xeon Gold 6148, 2.40 GHz)

SPECrate®2017\_fp\_base = 204

SPECrate®2017\_fp\_peak = 206

**CPU2017 License:** 9019

**Test Sponsor:** Cisco Systems

**Tested by:** Cisco Systems

**Test Date:** May-2018

**Hardware Availability:** Aug-2017

**Software Availability:** Mar-2018

## Base Optimization Flags

C benchmarks:

```
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only  
-qopt-mem-layout-trans=3
```

C++ benchmarks:

```
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only  
-qopt-mem-layout-trans=3
```

Fortran benchmarks:

```
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only  
-qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte
```

Benchmarks using both Fortran and C:

```
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only  
-qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte
```

Benchmarks using both C and C++:

```
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only  
-qopt-mem-layout-trans=3
```

Benchmarks using Fortran, C, and C++:

```
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only  
-qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte
```

## Peak Compiler Invocation

C benchmarks:

```
icc -m64 -std=c11
```

C++ benchmarks:

```
icpc -m64
```

Fortran benchmarks:

```
ifort -m64
```

Benchmarks using both Fortran and C:

```
ifort -m64 icc -m64 -std=c11
```

Benchmarks using both C and C++:

```
icpc -m64 icc -m64 -std=c11
```

Benchmarks using Fortran, C, and C++:

```
icpc -m64 icc -m64 -std=c11 ifort -m64
```





# SPEC CPU®2017 Floating Point Rate Result

Copyright 2017-2019 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS B200 M5 (Intel Xeon Gold 6148, 2.40 GHz)

SPECrate®2017\_fp\_base = 204

SPECrate®2017\_fp\_peak = 206

**CPU2017 License:** 9019

**Test Sponsor:** Cisco Systems

**Tested by:** Cisco Systems

**Test Date:** May-2018

**Hardware Availability:** Aug-2017

**Software Availability:** Mar-2018

## Peak Portability Flags

Same as Base Portability Flags

## Peak Optimization Flags

C benchmarks:

```
519.lbm_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -O3  
-no-prec-div -qopt-prefetch -ffinite-math-only  
-qopt-mem-layout-trans=3
```

```
538.imagick_r: -xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch  
-ffinite-math-only -qopt-mem-layout-trans=3
```

544.nab\_r: Same as 519.lbm\_r

C++ benchmarks:

```
-prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -O3  
-no-prec-div -qopt-prefetch -ffinite-math-only  
-qopt-mem-layout-trans=3
```

Fortran benchmarks:

```
503.bwaves_r: -xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch  
-ffinite-math-only -qopt-mem-layout-trans=3  
-nostandard-realloc-lhs -align array32byte
```

549.fotonik3d\_r: Same as 503.bwaves\_r

```
554.roms_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -O3  
-no-prec-div -qopt-prefetch -ffinite-math-only  
-qopt-mem-layout-trans=3 -nostandard-realloc-lhs  
-align array32byte
```

Benchmarks using both Fortran and C:

```
-prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -O3  
-no-prec-div -qopt-prefetch -ffinite-math-only  
-qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte
```

Benchmarks using both C and C++:

```
-prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -O3  
-no-prec-div -qopt-prefetch -ffinite-math-only  
-qopt-mem-layout-trans=3
```

(Continued on next page)



# SPEC CPU®2017 Floating Point Rate Result

Copyright 2017-2019 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS B200 M5 (Intel Xeon Gold 6148, 2.40 GHz)

SPECrate®2017\_fp\_base = 204

SPECrate®2017\_fp\_peak = 206

**CPU2017 License:** 9019

**Test Sponsor:** Cisco Systems

**Tested by:** Cisco Systems

**Test Date:** May-2018

**Hardware Availability:** Aug-2017

**Software Availability:** Mar-2018

## Peak Optimization Flags (Continued)

Benchmarks using Fortran, C, and C++:

```
-prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -O3  
-no-prec-div -qopt-prefetch -ffinite-math-only  
-qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte
```

The flags files that were used to format this result can be browsed at

<http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.2018-06-13.html>  
<http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revH.html>

You can also download the XML flags sources by saving the following links:

<http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.2018-06-13.xml>  
<http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revH.xml>

SPEC CPU and SPECrate are registered trademarks of the Standard Performance Evaluation Corporation. All other brand and product names appearing in this result are trademarks or registered trademarks of their respective holders.

For questions about this result, please contact the tester. For other inquiries, please contact [info@spec.org](mailto:info@spec.org).

Tested with SPEC CPU®2017 v1.0.2 on 2018-05-09 04:35:42-0400.

Report generated on 2019-12-13 18:12:43 by CPU2017 PDF formatter v6255.

Originally published on 2018-06-13.