



SPEC® CINT2006 Result

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Bull SAS

SPECint®_rate2006 = 189

NovaScale R460 F2 (Intel Xeon L5630, 2.13 GHz)

SPECint_rate_base2006 = 176

CPU2006 license: 20

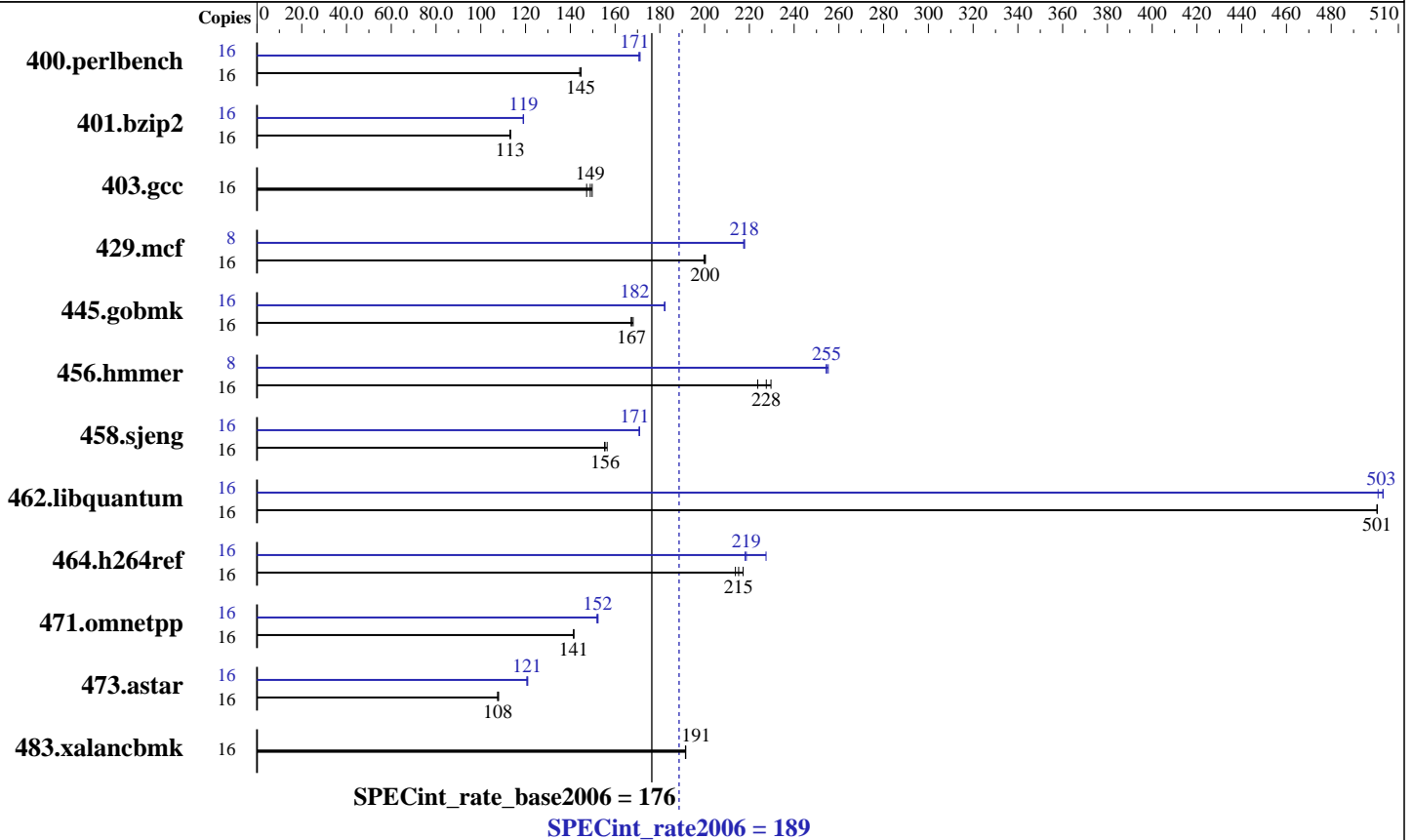
Test date: May-2010

Test sponsor: Bull SAS

Hardware Availability: Mar-2010

Tested by: Dell Inc.

Software Availability: Dec-2009



Hardware

CPU Name: Intel Xeon L5630
 CPU Characteristics: Intel Turbo Boost Technology up to 2.40 GHz
 CPU MHz: 2133
 FPU: Integrated
 CPU(s) enabled: 8 cores, 2 chips, 4 cores/chip, 2 threads/core
 CPU(s) orderable: 1,2 chips
 Primary Cache: 32 KB I + 32 KB D on chip per core
 Secondary Cache: 256 KB I+D on chip per core
 L3 Cache: 12 MB I+D on chip per chip
 Other Cache: None
 Memory: 48 GB (12 x 4 GB DDR3-1333 DR RDIMM, CL9, ECC, downclocked to 1066 MHz)
 Disk Subsystem: 1 x 146 GB 15000 RPM SAS
 Other Hardware: None

Software

Operating System: SUSE Linux Enterprise Server 11 (x86_64), Kernel 2.6.27.19-5-smp
 Compiler: Intel C++ Professional Compiler for IA32 and Intel 64, Version 11.1
 Build 20091130 Package ID: l_cproc_p_11.1.064
 Auto Parallel: No
 File System: ext3
 System State: Run level 3 (multi-user)
 Base Pointers: 32-bit
 Peak Pointers: 32/64-bit
 Other Software: Microquill SmartHeap V8.1



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Results Table

Benchmark	Base							Peak						
	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
400.perlbench	16	1084	144	1080	145	1080	145	16	913	171	915	171	916	171
401.bzip2	16	1365	113	1363	113	1365	113	16	1297	119	1296	119	1298	119
403.gcc	16	860	150	865	149	874	147	16	860	150	865	149	874	147
429.mcf	16	731	200	729	200	728	200	8	335	218	335	218	336	217
445.gobmk	16	1003	167	999	168	1004	167	16	921	182	922	182	921	182
456.hammer	16	667	224	656	228	650	230	8	293	255	293	254	292	255
458.sjeng	16	1245	156	1237	156	1247	155	16	1133	171	1133	171	1134	171
462.libquantum	16	662	500	662	501	662	501	16	662	501	659	503	659	503
464.h264ref	16	1656	214	1630	217	1645	215	16	1619	219	1624	218	1557	227
471.omnetpp	16	707	141	706	142	707	141	16	657	152	656	152	658	152
473.astar	16	1040	108	1045	108	1043	108	16	928	121	931	121	931	121
483.xalancbmk	16	577	191	577	191	576	192	16	577	191	577	191	576	192

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes

The config file option 'submit' was used.
numactl was used to bind copies to the cores

Operating System Notes

'ulimit -s unlimited' was used to set the stacksize to unlimited prior to run

Platform Notes

BIOS Settings:
Power Management = Maximum Performance (Default = Active Power Controller)
Data Reuse = Disabled (Default = Enabled)

General Notes

Binaries were compiled on SLES 10 with Binutils 2.18.50.0.7.20080502
The Dell PowerEdge R710 and
the Bull NovaScale R460 F2 models are electronically equivalent.
The results have been measured on a Dell PowerEdge R710 model.

Base Compiler Invocation

C benchmarks:
icc -m32

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Base Compiler Invocation (Continued)

C++ benchmarks:
icpc -m32

Base Portability Flags

400.perlbench: -DSPEC_CPU_LINUX_IA32
462.libquantum: -DSPEC_CPU_LINUX
483.xalancbmk: -DSPEC_CPU_LINUX

Base Optimization Flags

C benchmarks:
-xSSE4.2 -ipo -O3 -no-prec-div -static -opt-prefetch

C++ benchmarks:
-xSSE4.2 -ipo -O3 -no-prec-div -opt-prefetch -Wl,-z,muldefs
-L/home/cmplr/usr3/alrahate/cpu2006.1.1.icl1.1/libicl1.1-32bit -lsmarheap

Base Other Flags

C benchmarks:
403.gcc: -Dalloca=_alloca

Peak Compiler Invocation

C benchmarks (except as noted below):
icc -m32

401.bzip2: icc -m64

456.hmmer: icc -m64

458.sjeng: icc -m64

462.libquantum: icc -m64

C++ benchmarks (except as noted below):
icpc -m32

473.astar: icpc -m64



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Peak Portability Flags

```

400.perlbench: -DSPEC_CPU_LINUX_IA32
401.bzip2: -DSPEC_CPU_LP64
456.hmmer: -DSPEC_CPU_LP64
458.sjeng: -DSPEC_CPU_LP64
462.libquantum: -DSPEC_CPU_LP64 -DSPEC_CPU_LINUX
473.astar: -DSPEC_CPU_LP64
483.xalancbmk: -DSPEC_CPU_LINUX

```

Peak Optimization Flags

C benchmarks:

```

400.perlbench: -xSSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2)
               -O3(pass 2) -no-prec-div(pass 2) -static(pass 2)
               -prof-use(pass 2) -ansi-alias

401.bzip2: -xSSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2)
            -O3(pass 2) -no-prec-div(pass 2) -static(pass 2)
            -prof-use(pass 2) -opt-prefetch -ansi-alias -auto-ilp32

403.gcc: basepeak = yes

429.mcf: -xSSE4.2 -ipo -O3 -no-prec-div -static -opt-prefetch

445.gobmk: -xSSE4.2(pass 2) -prof-gen(pass 1) -prof-use(pass 2) -O2
            -ipo -no-prec-div -ansi-alias

456.hmmer: -xSSE4.2 -ipo -O3 -no-prec-div -static -unroll2
            -ansi-alias -auto-ilp32

458.sjeng: -xSSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2)
            -O3(pass 2) -no-prec-div(pass 2) -static(pass 2)
            -prof-use(pass 2) -unroll4 -auto-ilp32

462.libquantum: -xSSE4.2 -ipo -O3 -no-prec-div -static -auto-ilp32
                -opt-prefetch

464.h264ref: -xSSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2)
              -O3(pass 2) -no-prec-div(pass 2) -static(pass 2)
              -prof-use(pass 2) -unroll2 -ansi-alias

```

C++ benchmarks:

```

471.omnetpp: -xSSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2)
              -O3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2)
              -ansi-alias -opt-ra-region-strategy=block -Wl,-z,muldefs
              -L/home/cmplr/usr3/alrahate/cpu2006.1.1.ic11.1/libic11.1-32bit -lsmartheap

```

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Peak Optimization Flags (Continued)

```

473.astar: -xSSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2)
          -O3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2)
          -ansi-alias -opt-ra-region-strategy=routine -Wl,-z,muldefs
          -L/home/cmplr/usr3/alrahate/cpu2006.1.1.ic11.1/libic11.1-64bit -lsmartheap64

```

483.xalancbmk: basepeak = yes

Peak Other Flags

C benchmarks:

403.gcc: -Dalloca=_alloca

The flags file that was used to format this result can be browsed at

<http://www.spec.org/cpu2006/flags/Intel-ic11.1-linux64-revE.20100330.html>

You can also download the XML flags source by saving the following link:

<http://www.spec.org/cpu2006/flags/Intel-ic11.1-linux64-revE.20100330.xml>

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For other inquiries, please contact webmaster@spec.org.

Tested with SPEC CPU2006 v1.1.
Report generated on Wed Jul 23 09:10:33 2014 by SPEC CPU2006 PS/PDF formatter v6932.
Originally published on 9 June 2010.