



# SPEC CPU®2017 Floating Point Rate Result

Copyright 2017-2023 Standard Performance Evaluation Corporation

## Lenovo Global Technology

SPECrate®2017\_fp\_base = 521

ThinkSystem SR630 V3  
(2.10 GHz, Intel Xeon Gold 6418H)

SPECrate®2017\_fp\_peak = Not Run

CPU2017 License: 9017

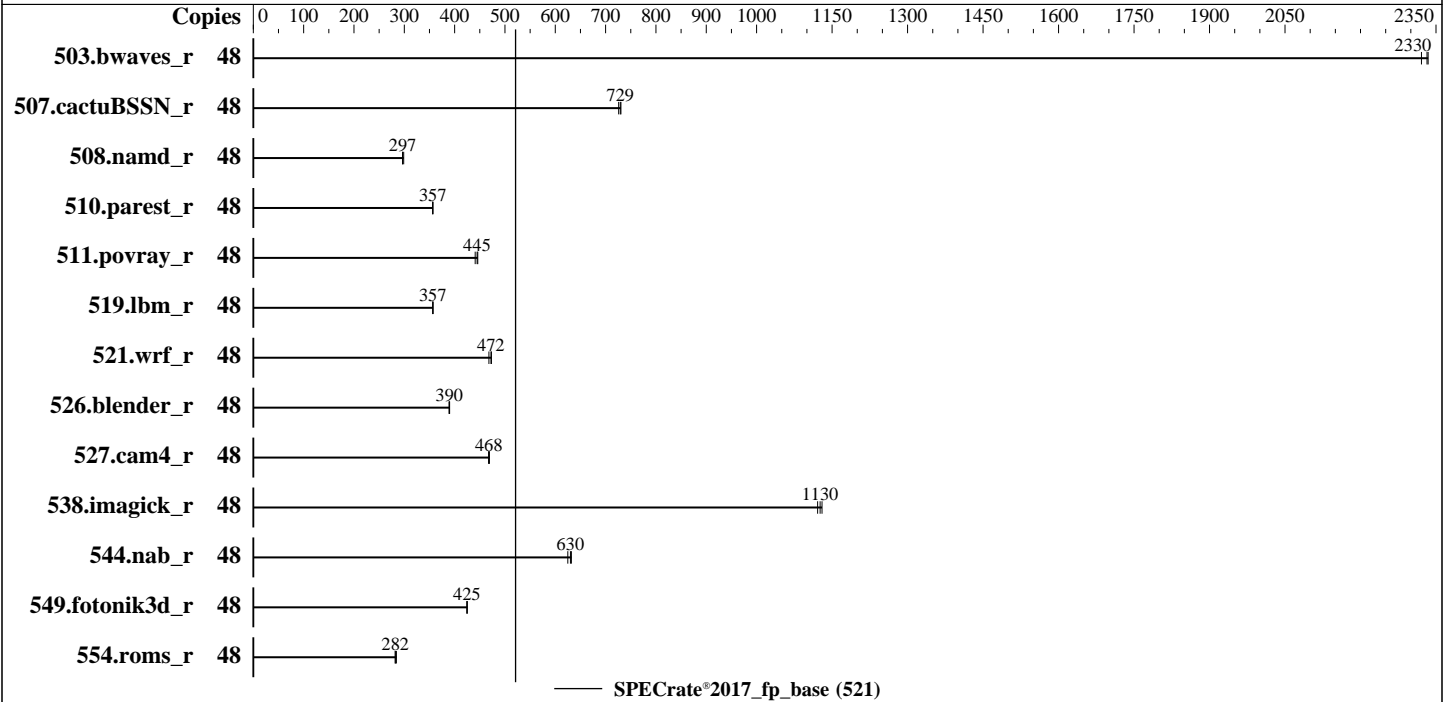
Test Date: Dec-2022

Test Sponsor: Lenovo Global Technology

Hardware Availability: Feb-2023

Tested by: Lenovo Global Technology

Software Availability: Jun-2022



### Hardware

CPU Name: Intel Xeon Gold 6418H  
 Max MHz: 4000  
 Nominal: 2100  
 Enabled: 48 cores, 2 chips  
 Orderable: 1,2 chips  
 Cache L1: 32 KB I + 48 KB D on chip per core  
 L2: 2 MB I+D on chip per core  
 L3: 60 MB I+D on chip per chip  
 Other: None  
 Memory: 512 GB (16 x 32 GB 2Rx8 PC5-4800B-R)  
 Storage: 1 x 960 GB SATA SSD  
 Other: None

### Software

OS: SUSE Linux Enterprise Server 15 SP4 (x86\_64)  
 Kernel 5.14.21-150400.22-default  
 Compiler: C/C++: Version 2022.1 of Intel oneAPI DPC++/C++ Compiler for Linux;  
 Fortran: Version 2022.1 of Intel Fortran Compiler for Linux;  
 Parallel: No  
 Firmware: Lenovo BIOS Version ESE109G 0.83 released Dec-2022  
 File System: xfs  
 System State: Run level 3 (multi-user)  
 Base Pointers: 64-bit  
 Peak Pointers: Not Applicable  
 Other: jemalloc memory allocator V5.0.1  
 Power Management: BIOS and OS set to prefer performance at the cost of additional power usage



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## Results Table

Benchmark	Base							Peak						
	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
503.bwaves_r	48	206	2330	207	2320	<u>206</u>	<u>2330</u>							
507.cactuBSSN_r	48	83.7	726	<u>83.3</u>	<u>729</u>	83.2	730							
508.namd_r	48	153	299	154	297	<u>154</u>	<u>297</u>							
510.parest_r	48	<u>352</u>	<u>357</u>	352	357	352	356							
511.povray_r	48	251	446	<u>252</u>	<u>445</u>	254	441							
519.lbm_r	48	142	357	<u>142</u>	<u>357</u>	142	357							
521.wrf_r	48	230	468	<u>228</u>	<u>472</u>	227	473							
526.blender_r	48	188	389	187	390	<u>188</u>	<u>390</u>							
527.cam4_r	48	180	468	179	469	<u>179</u>	<u>468</u>							
538.imagick_r	48	106	1120	<u>106</u>	<u>1130</u>	106	1130							
544.nab_r	48	129	625	<u>128</u>	<u>630</u>	128	632							
549.fotonik3d_r	48	441	425	<u>440</u>	<u>425</u>	440	425							
554.roms_r	48	268	284	<u>270</u>	<u>282</u>	271	282							

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Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

## Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

## Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

## Environment Variables Notes

Environment variables set by runcpu before the start of the run:  
LD\_LIBRARY\_PATH =  
"/home/cpu2017-1.1.8-ic2022.1/lib/intel64:/home/cpu2017-1.1.8-ic2022.1/j  
e5.0.1-64"  
MALLOC\_CONF = "retain:true"

## General Notes

Binaries compiled on a system with 2x Intel Xeon Platinum 8280M CPU + 384GB RAM memory using Red Hat Enterprise Linux 8.4  
Transparent Huge Pages enabled by default

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## General Notes (Continued)

Prior to runcpu invocation  
Filesystem page cache synced and cleared with:  
sync; echo 3> /proc/sys/vm/drop\_caches  
runcpu command invoked through numactl i.e.:  
numactl --interleave=all runcpu <etc>

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

jemalloc, a general purpose malloc implementation  
built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5  
sources available from jemalloc.net or <https://github.com/jemalloc/jemalloc/releases>

## Platform Notes

BIOS configuration:

Choose Operating Mode set to Maximum Performance and then set it to Custom Mode

Hyper-Threading set to Disabled

SNC set to SNC2

LLC Prefetch set to Disabled

Sysinfo program /home/cpu2017-1.1.8-ic2022.1/bin/sysinfo  
Rev: r6622 of 2021-04-07 982a61ec0915b55891ef0e16acafc64d  
running on test1 Tue Dec 27 18:31:09 2022

SUT (System Under Test) info as seen by some common utilities.

For more information on this section, see

<https://www.spec.org/cpu2017/Docs/config.html#sysinfo>

From /proc/cpuinfo

model name : Intel(R) Xeon(R) Gold 6418H

2 "physical id"s (chips)

48 "processors"

cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)

cpu cores : 24

siblings : 24

physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23

physical 1: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23

From lscpu from util-linux 2.37.2:

Architecture: x86\_64

CPU op-mode(s): 32-bit, 64-bit

Address sizes: 46 bits physical, 57 bits virtual

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### Platform Notes (Continued)

```

Byte Order:                Little Endian
CPU(s):                    48
On-line CPU(s) list:      0-47
Vendor ID:                 GenuineIntel
Model name:               Intel(R) Xeon(R) Gold 6418H
CPU family:               6
Model:                    143
Thread(s) per core:      1
Core(s) per socket:      24
Socket(s):                2
Stepping:                 8
BogoMIPS:                 4200.00
Flags:                    fpu vme de pse tsc msr pae mce cx8 apic sep mtrr
pge mca cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx
pdpelgb rdtscp lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology
nonstop_tsc cpuid aperfmperf tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl vmx
smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt
tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault
epb cat_l3 cat_l2 cdp_l3 invpcid_single intel_ppin cdp_l2 ssbd mba ibrs ibpb stibp
ibrs_enhanced tpr_shadow vnmi flexpriority ept vpid ept_ad fsgsbase tsc_adjust bmil
hle avx2 smep bmi2 erms invpcid rtm cqm rdt_a avx512f avx512dq rdseed adx smap
avx512ifma clflushopt clwb intel_pt avx512cd sha_ni avx512bw avx512vl xsaveopt
xsavec xgetbv1 xsaves cqm_llc cqm_occup_llc cqm_mbm_total cqm_mbm_local
split_lock_detect avx_vnni avx512_bf16 wbnoinvd dtherm ida arat pln pts avx512vbmi
umip pku ospke waitpkg avx512_vbmi2 gfni vaes vpclmulqdq avx512_vnni avx512_bitalg
tme avx512_vpopcntdq la57 rdpid bus_lock_detect cldemote movdiri movdir64b enqcmd
fsrm md_clear serialize tsxldtrk pconfig arch_lbr avx512_fp16 amx_tile flush_lld
arch_capabilities
Virtualization:           VT-x
L1d cache:               2.3 MiB (48 instances)
L1i cache:               1.5 MiB (48 instances)
L2 cache:                 96 MiB (48 instances)
L3 cache:                 120 MiB (2 instances)
NUMA node(s):            4
NUMA node0 CPU(s):       0-11
NUMA node1 CPU(s):       12-23
NUMA node2 CPU(s):       24-35
NUMA node3 CPU(s):       36-47
Vulnerability Itlb multihit: Not affected
Vulnerability L1tf:      Not affected
Vulnerability Mds:       Not affected
Vulnerability Meltdown:  Not affected
Vulnerability Spec store bypass: Mitigation; Speculative Store Bypass disabled via
prctl and seccomp
Vulnerability Spectre v1: Mitigation; usercopy/swapgs barriers and __user
pointer sanitization
Vulnerability Spectre v2: Mitigation; Enhanced IBRS, IBPB conditional, RSB

```

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### Platform Notes (Continued)

filling

Vulnerability Srbds: Not affected

Vulnerability Tsx async abort: Not affected

From lscpu --cache:

NAME	ONE-SIZE	ALL-SIZE	WAYS	TYPE	LEVEL	SETS	PHY-LINE	COHERENCY-SIZE
L1d	48K	2.3M	12	Data	1	64	1	64
L1i	32K	1.5M	8	Instruction	1	64	1	64
L2	2M	96M	16	Unified	2	2048	1	64
L3	60M	120M	15	Unified	3	65536	1	64

/proc/cpuinfo cache data  
cache size : 61440 KB

From numactl --hardware

WARNING: a numactl 'node' might or might not correspond to a physical chip.

available: 4 nodes (0-3)

node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11

node 0 size: 128684 MB

node 0 free: 128103 MB

node 1 cpus: 12 13 14 15 16 17 18 19 20 21 22 23

node 1 size: 129020 MB

node 1 free: 128708 MB

node 2 cpus: 24 25 26 27 28 29 30 31 32 33 34 35

node 2 size: 128986 MB

node 2 free: 128707 MB

node 3 cpus: 36 37 38 39 40 41 42 43 44 45 46 47

node 3 size: 129001 MB

node 3 free: 128675 MB

node distances:

node 0 1 2 3

0: 10 12 21 21

1: 12 10 21 21

2: 21 21 10 12

3: 21 21 12 10

From /proc/meminfo

MemTotal: 528069420 kB

HugePages\_Total: 0

Hugepagesize: 2048 kB

From /etc/\*release\* /etc/\*version\*

os-release:

NAME="SLES"

VERSION="15-SP4"

VERSION\_ID="15.4"

PRETTY\_NAME="SUSE Linux Enterprise Server 15 SP4"

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### Platform Notes (Continued)

```
ID="sles"
ID_LIKE="suse"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15:sp4"
```

```
uname -a:
Linux test1 5.14.21-150400.22-default #1 SMP PREEMPT_DYNAMIC Wed May 11 06:57:18 UTC
2022 (49db222) x86_64 x86_64 x86_64 GNU/Linux
```

Kernel self-reported vulnerability status:

CVE-2018-12207 (iTLB Multihit):	Not affected
CVE-2018-3620 (L1 Terminal Fault):	Not affected
Microarchitectural Data Sampling:	Not affected
CVE-2017-5754 (Meltdown):	Not affected
CVE-2018-3639 (Speculative Store Bypass):	Mitigation: Speculative Store Bypass disabled via prctl and seccomp
CVE-2017-5753 (Spectre variant 1):	Mitigation: usercopy/swapgs barriers and __user pointer sanitization
CVE-2017-5715 (Spectre variant 2):	Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling
CVE-2020-0543 (Special Register Buffer Data Sampling):	Not affected
CVE-2019-11135 (TSX Asynchronous Abort):	Not affected

run-level 3 Dec 27 18:28

```
SPEC is set to: /home/cpu2017-1.1.8-ic2022.1
Filesystem      Type  Size  Used Avail Use% Mounted on
/dev/sda2       xfs   894G  55G  840G   7% /
```

```
From /sys/devices/virtual/dmi/id
Vendor:          Lenovo
Product:         ThinkSystem SR630 V3
Product Family: ThinkSystem
Serial:          1234567890
```

Additional information from dmidecode 3.2 follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

```
Memory:
1x Samsung M321R4GA3BB0-CQKEG 32 GB 2 rank 4800
5x Samsung M321R4GA3BB0-CQKMG 32 GB 2 rank 4800
10x Samsung M321R4GA3BB0-CQKVG 32 GB 2 rank 4800
```

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### Platform Notes (Continued)

BIOS:

BIOS Vendor: Lenovo  
BIOS Version: ESE109G-0.83  
BIOS Date: 12/20/2022  
BIOS Revision: 0.83  
Firmware Revision: 0.75

(End of data from sysinfo program)

### Compiler Version Notes

=====  
C | 519.lbm\_r(base) 538.imagick\_r(base) 544.nab\_r(base)  
=====

Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,  
Version 2022.1.0 Build 20220316  
Copyright (C) 1985-2022 Intel Corporation. All rights reserved.  
=====

=====  
C++ | 508.namd\_r(base) 510.parest\_r(base)  
=====

Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,  
Version 2022.1.0 Build 20220316  
Copyright (C) 1985-2022 Intel Corporation. All rights reserved.  
=====

=====  
C++, C | 511.povray\_r(base) 526.blender\_r(base)  
=====

Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,  
Version 2022.1.0 Build 20220316  
Copyright (C) 1985-2022 Intel Corporation. All rights reserved.  
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,  
Version 2022.1.0 Build 20220316  
Copyright (C) 1985-2022 Intel Corporation. All rights reserved.  
=====

=====  
C++, C, Fortran | 507.cactuBSSN\_r(base)  
=====

Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,  
Version 2022.1.0 Build 20220316  
Copyright (C) 1985-2022 Intel Corporation. All rights reserved.  
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### Compiler Version Notes (Continued)

Copyright (C) 1985-2022 Intel Corporation. All rights reserved.  
Intel(R) Fortran Compiler for applications running on Intel(R) 64, Version  
2022.1.0 Build 20220316

Copyright (C) 1985-2022 Intel Corporation. All rights reserved.

=====  
Fortran | 503.bwaves\_r(base) 549.fotonik3d\_r(base) 554.roms\_r(base)

-----  
Intel(R) Fortran Compiler for applications running on Intel(R) 64, Version  
2022.1.0 Build 20220316

Copyright (C) 1985-2022 Intel Corporation. All rights reserved.

=====  
Fortran, C | 521.wrf\_r(base) 527.cam4\_r(base)

-----  
Intel(R) Fortran Compiler for applications running on Intel(R) 64, Version  
2022.1.0 Build 20220316

Copyright (C) 1985-2022 Intel Corporation. All rights reserved.

Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,  
Version 2022.1.0 Build 20220316

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### Base Compiler Invocation

C benchmarks:

icx

C++ benchmarks:

icpx

Fortran benchmarks:

ifx

Benchmarks using both Fortran and C:

ifx icx

Benchmarks using both C and C++:

icpx icx

Benchmarks using Fortran, C, and C++:

icpx icx ifx





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## Base Portability Flags

```
503.bwaves_r: -DSPEC_LP64
507.cactuBSSN_r: -DSPEC_LP64
508.namd_r: -DSPEC_LP64
510.parest_r: -DSPEC_LP64
511.povray_r: -DSPEC_LP64
519.lbm_r: -DSPEC_LP64
521.wrf_r: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
526.blender_r: -DSPEC_LP64 -DSPEC_LINUX -funsigned-char
527.cam4_r: -DSPEC_LP64 -DSPEC_CASE_FLAG
538.imagick_r: -DSPEC_LP64
544.nab_r: -DSPEC_LP64
549.fotonik3d_r: -DSPEC_LP64
554.roms_r: -DSPEC_LP64
```

## Base Optimization Flags

### C benchmarks:

```
-w -std=c11 -m64 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4 -ljemalloc
-L/usr/local/jemalloc64-5.0.1/lib
```

### C++ benchmarks:

```
-w -m64 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math -flto
-mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4 -ljemalloc
-L/usr/local/jemalloc64-5.0.1/lib
```

### Fortran benchmarks:

```
-w -m64 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math -flto
-mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-nostandard-realloc-lhs -align array32byte -auto -ljemalloc
-L/usr/local/jemalloc64-5.0.1/lib
```

### Benchmarks using both Fortran and C:

```
-w -m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-nostandard-realloc-lhs -align array32byte -auto -ljemalloc
-L/usr/local/jemalloc64-5.0.1/lib
```

### Benchmarks using both C and C++:

```
-w -m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4 -ljemalloc
-L/usr/local/jemalloc64-5.0.1/lib
```

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## Base Optimization Flags (Continued)

Benchmarks using Fortran, C, and C++:

```
-w -m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-nostandard-realloc-lhs -align array32byte -auto -ljemalloc
-L/usr/local/jemalloc64-5.0.1/lib
```

The flags files that were used to format this result can be browsed at

<http://www.spec.org/cpu2017/flags/Lenovo-Platform-SPECcpu2017-Flags-V1.2-Eaglestream-N.html>

[http://www.spec.org/cpu2017/flags/Intel-ic2022-official-linux64\\_revA.html](http://www.spec.org/cpu2017/flags/Intel-ic2022-official-linux64_revA.html)

You can also download the XML flags sources by saving the following links:

<http://www.spec.org/cpu2017/flags/Lenovo-Platform-SPECcpu2017-Flags-V1.2-Eaglestream-N.xml>

[http://www.spec.org/cpu2017/flags/Intel-ic2022-official-linux64\\_revA.xml](http://www.spec.org/cpu2017/flags/Intel-ic2022-official-linux64_revA.xml)

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For questions about this result, please contact the tester. For other inquiries, please contact [info@spec.org](mailto:info@spec.org).

Tested with SPEC CPU®2017 v1.1.8 on 2022-12-27 05:31:09-0500.

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