SPEC CPU®2017 Integer Rate Result

Hewlett Packard Enterprise

(Test Sponsor: HPE)

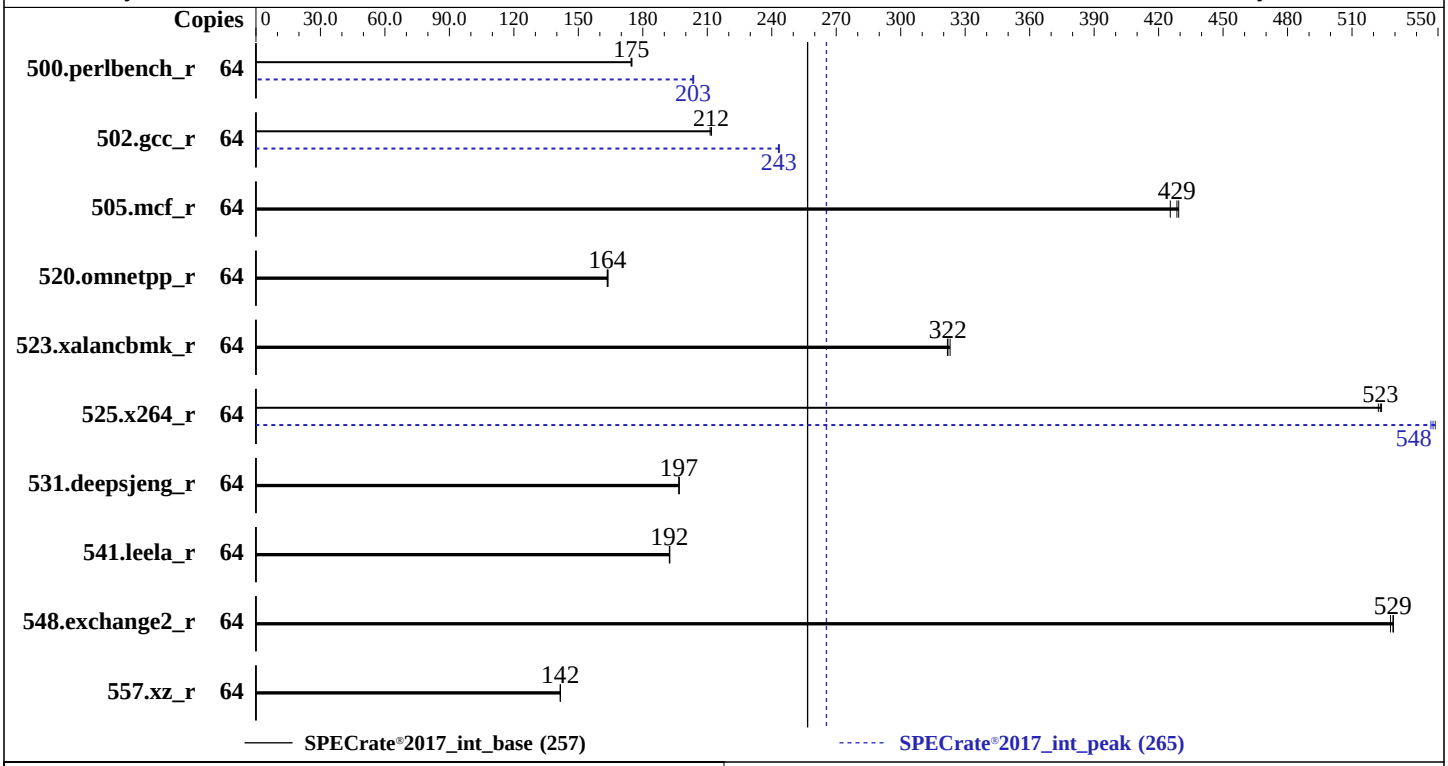
Synergy 480 Gen10 Plus
(2.90 GHz, Intel Xeon Gold 6326)

SPECrate®2017_int_base = 257

SPECrate®2017_int_peak = 265

CPU2017 License: 3
Test Sponsor: HPE
Tested by: HPE

Test Date: Dec-2021
Hardware Availability: Nov-2021
Software Availability: Dec-2020



Hardware

CPU Name:	Intel Xeon Gold 6326
Max MHz:	3500
Nominal:	2900
Enabled:	32 cores, 2 chips, 2 threads/core
Orderable:	1, 2 chip(s)
Cache L1:	32 KB I + 48 KB D on chip per core
L2:	1.25 MB I+D on chip per core
L3:	24 MB I+D on chip per chip
Other:	None
Memory:	2 TB (32 x 64 GB 2Rx4 PC4-3200AA-R)
Storage:	1 x 800 GB SAS SSD, RAID 0
Other:	None

Software

OS:	Red Hat Enterprise Linux 8.3 (Ootpa) Kernel 4.18.0-240.el8.x86_64
Compiler:	C/C++: Version 2021.1 of Intel oneAPI DPC++/C++ Compiler Build 20201113 for Linux; Fortran: Version 2021.1 of Intel Fortran Compiler Classic Build 20201112 for Linux; C/C++: Version 2021.1 of Intel C/C++ Compiler Classic Build 20201112 for Linux
Parallel:	No
Firmware:	HPE BIOS Version I44 v1.54 11/03/2021 released Nov-2021
File System:	xfs
System State:	Run level 3 (multi-user)
Base Pointers:	64-bit
Peak Pointers:	32/64-bit
Other:	jemalloc memory allocator V5.0.1
Power Management:	BIOS and OS set to prefer performance at the cost of additional power usage

Results Table

Benchmark	Base							Peak						
	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
500.perlbench_r	64	584	175	582	175	**583**	**175**	64	500	204	501	203	**501**	**203**
502.gcc_r	64	428	212	**428**	**212**	429	211	64	**373**	**243**	373	243	372	244
505.mcf_r	64	**241**	**429**	241	429	243	425	64	**241**	**429**	241	429	243	425
520.omnetpp_r	64	**513**	**164**	513	164	514	163	64	**513**	**164**	513	164	514	163
523.xalancbmk_r	64	209	323	**210**	**322**	210	322	64	209	323	**210**	**322**	210	322
525.x264_r	64	214	524	**214**	**523**	215	522	64	**205**	**548**	204	549	205	547
531.deepsjeng_r	64	373	197	**373**	**197**	373	197	64	373	197	**373**	**197**	373	197
541.leela_r	64	551	192	550	193	**551**	**192**	64	551	192	550	193	**551**	**192**
548.exchange2_r	64	318	528	317	529	**317**	**529**	64	318	528	317	529	**317**	**529**
557.xz_r	64	**488**	**142**	488	142	488	142	64	**488**	**142**	488	142	488	142

SPECrate®2017_int_base = 257

SPECrate®2017_int_peak = 265

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes

```
The numactl mechanism was used to bind copies to processors. The config file option 'submit'
was used to generate numactl commands to bind each copy to a specific processor.
For details, please see the config file.
```

Operating System Notes

```
Stack size set to unlimited using "ulimit -s unlimited"
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3 >       /proc/sys/vm/drop_caches
Tuned-adm profile was set to throughput-performance using "tuned-adm profile throughput-performance"
Cpupower Frequency was set to performance using "cpupower frequency-set -g performance"
```

Environment Variables Notes

```
Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH =
     "/home/cpu2017/lib/intel64:/home/cpu2017/lib/ia32:/home/cpu2017/je5.0.1-
     32"
MALLOC_CONF = "retain:true"
```

General Notes

```
 Binaries compiled on a system with 1x Intel Core i9-7980XE CPU + 64GB RAM
 memory using Red Hat Enterprise Linux 8.1
 runcpu command invoked through numactl i.e.:
 numactl --interleave=all runcpu <etc>
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2)
is mitigated in the system as tested and documented.
 jemalloc, a general purpose malloc implementation
 built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5
 sources available from jemalloc.net or https://github.com/jemalloc/jemalloc/releases

Submitted_by: "Bucek, James" <james.bucek@hpe.com>
Submitted: Wed Jan 12 10:02:54 EST 2022
Submission: cpu2017-20220103-30736.sub
```

Platform Notes

```
  BIOS Configuration:
  Workload Profile set to General Throughput Compute
  Memory Patrol Scrubbing set to Disabled
  Advanced Memory Protection set to Advanced ECC
  XPT Remote Prefetcher set to Enabled
  Last Level Cache (LLC) Dead Line Allocation set to Disabled
  Enhanced Processor Performance set to Enabled
  Thermal Configuration set to Maximum Cooling
  Intel UPI Link Frequency set to Min UPI Speed
  Intel UPI Link Enablement set to Single Link
  D2K set to Disabled
  Workload Profile set to Custom
    DCU Stream Prefetcher set to Disabled
    Energy Efficient Turbo set to Enabled
    Adjacent Sector Prefetcher set to Disabled
    Intel UPI Link Power Management set to Enabled

 Sysinfo program /home/cpu2017/bin/sysinfo
 Rev: r6622 of 2021-04-07 982a61ec0915b55891ef0e16acafc64d
 running on localhost.localdomain Thu Dec 16 23:43:08 2021

 SUT (System Under Test) info as seen by some common utilities.
 For more information on this section, see
    https://www.spec.org/cpu2017/Docs/config.html#sysinfo

 From /proc/cpuinfo
```

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Platform Notes (Continued)

```
    model name : Intel(R) Xeon(R) Gold 6326 CPU @ 2.90GHz
       2  "physical id"s (chips)
       64 "processors"
    cores, siblings (Caution: counting these is hw and system dependent. The following
    excerpts from /proc/cpuinfo might not be reliable.  Use with caution.)
       cpu cores : 16
       siblings  : 32
       physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
       physical 1: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

  From lscpu from util-linux 2.32.1:
       Architecture:        x86_64
       CPU op-mode(s):      32-bit, 64-bit
       Byte Order:          Little Endian
       CPU(s):              64
       On-line CPU(s) list: 0-63
       Thread(s) per core:  2
       Core(s) per socket:  16
       Socket(s):           2
       NUMA node(s):        2
       Vendor ID:           GenuineIntel
       CPU family:          6
       Model:               106
       Model name:          Intel(R) Xeon(R) Gold 6326 CPU @ 2.90GHz
       Stepping:            6
       CPU MHz:             1268.597
       CPU max MHz:         3500.0000
       CPU min MHz:         800.0000
       BogoMIPS:            5800.00
       Virtualization:      VT-x
       L1d cache:           48K
       L1i cache:           32K
       L2 cache:            1280K
       L3 cache:            24576K
       NUMA node0 CPU(s):   0-15,32-47
       NUMA node1 CPU(s):   16-31,48-63
       Flags:               fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
       pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
       lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
       aperfmperf pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16
       xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave
       avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_l3 invpcid_single ssbd
       mba ibrs ibpb stibp ibrs_enhanced tpr_shadow vnmi flexpriority ept vpid ept_ad
       fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid cqm rdt_a avx512f avx512dq
       rdseed adx smap avx512ifma clflushopt clwb intel_pt avx512cd sha_ni avx512bw
       avx512vl xsaveopt xsavec xgetbv1 xsaves cqm_llc cqm_occup_llc cqm_mbm_total
       cqm_mbm_local split_lock_detect wbnoinvd dtherm ida arat pln pts hwp hwp_act_window
```

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Platform Notes (Continued)

```
      hwp_pkg_req avx512vbmi umip pku ospke avx512_vbmi2 gfni vaes vpclmulqdq avx512_vnni
      avx512_bitalg tme avx512_vpopcntdq la57 rdpid md_clear pconfig flush_l1d
      arch_capabilities

 /proc/cpuinfo cache data
    cache size : 24576 KB

 From numactl --hardware
 WARNING: a numactl 'node' might or might not correspond to a physical chip.
   available: 2 nodes (0-1)
   node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 32 33 34 35 36 37 38 39 40 41 42 43
   44 45 46 47
   node 0 size: 984771 MB
   node 0 free: 1031036 MB
   node 1 cpus: 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 48 49 50 51 52 53 54 55 56
   57 58 59 60 61 62 63
   node 1 size: 986659 MB
   node 1 free: 1031309 MB
   node distances:
   node   0   1
     0:  10  20
     1:  20  10

 From /proc/meminfo
    MemTotal:       2113488392 kB
    HugePages_Total:       0
    Hugepagesize:       2048 kB

 /sbin/tuned-adm active
     Current active profile: throughput-performance

 /sys/devices/system/cpu/cpu*/cpufreq/scaling_governor has
    performance

 From /etc/*release* /etc/*version*
    os-release:
       NAME="Red Hat Enterprise Linux"
       VERSION="8.3 (Ootpa)"
       ID="rhel"
       ID_LIKE="fedora"
       VERSION_ID="8.3"
       PLATFORM_ID="platform:el8"
       PRETTY_NAME="Red Hat Enterprise Linux 8.3 (Ootpa)"
       ANSI_COLOR="0;31"
    redhat-release: Red Hat Enterprise Linux release 8.3 (Ootpa)
    system-release: Red Hat Enterprise Linux release 8.3 (Ootpa)
    system-release-cpe: cpe:/o:redhat:enterprise_linux:8.3:ga
```

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Platform Notes (Continued)

```
uname -a:
   Linux localhost.localdomain 4.18.0-240.el8.x86_64 #1 SMP Wed Sep 23 05:13:10 EDT 2020
   x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2018-12207 (iTLB Multihit):                          Not affected
CVE-2018-3620 (L1 Terminal Fault):                       Not affected
Microarchitectural Data Sampling:                        Not affected
CVE-2017-5754 (Meltdown):                                Not affected
CVE-2018-3639 (Speculative Store Bypass):                Mitigation: Speculative Store
                                                         Bypass disabled via prctl and
                                                         seccomp
CVE-2017-5753 (Spectre variant 1):                       Mitigation: usercopy/swapgs
                                                         barriers and __user pointer
                                                         sanitization
CVE-2017-5715 (Spectre variant 2):                      Mitigation: Enhanced IBRS, IBPB:
                                                         conditional, RSB filling
CVE-2020-0543 (Special Register Buffer Data Sampling): Not affected
CVE-2019-11135 (TSX Asynchronous Abort):                 Not affected

run-level 3 Dec 16 23:39

SPEC is set to: /home/cpu2017
   Filesystem            Type  Size  Used Avail Use% Mounted on
   /dev/mapper/rhel-home xfs   670G  112G  559G  17% /home

From /sys/devices/virtual/dmi/id
    Vendor:         HPE
    Product:        Synergy 480 Gen10 Plus
    Product Family: Synergy
    Serial:         CN70330Q5F

Additional information from dmidecode 3.2 follows.  WARNING: Use caution when you
interpret this section. The 'dmidecode' program reads system data which is "intended to
allow hardware to be accurately determined", but the intent may not be met, as there are
frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
  Memory:
    32x Micron 36ASF8G72PZ-3G2B2 64 GB 2 rank 3200

BIOS:
   BIOS Vendor:       HPE
   BIOS Version:      I44
   BIOS Date:         11/03/2021
   BIOS Revision:     1.54
   Firmware Revision: 2.50
```

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Platform Notes (Continued)

```
 (End of data from sysinfo program)
```

Compiler Version Notes

```
==============================================================================
C       | 500.perlbench_r(peak)
------------------------------------------------------------------------------
Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R)
  64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation.  All rights reserved.
------------------------------------------------------------------------------

==============================================================================
C       | 502.gcc_r(peak)
------------------------------------------------------------------------------
Intel(R) oneAPI DPC++/C++ Compiler for applications running on IA-32, Version
  2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

==============================================================================
C       | 500.perlbench_r(base) 502.gcc_r(base) 505.mcf_r(base, peak)
        | 525.x264_r(base, peak) 557.xz_r(base, peak)
------------------------------------------------------------------------------
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
  Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

==============================================================================
C       | 500.perlbench_r(peak)
------------------------------------------------------------------------------
Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R)
  64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation.  All rights reserved.
------------------------------------------------------------------------------

==============================================================================
C       | 502.gcc_r(peak)
------------------------------------------------------------------------------
Intel(R) oneAPI DPC++/C++ Compiler for applications running on IA-32, Version
  2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------
```


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Compiler Version Notes (Continued)

```
==============================================================================
C       | 500.perlbench_r(base) 502.gcc_r(base) 505.mcf_r(base, peak)
        | 525.x264_r(base, peak) 557.xz_r(base, peak)
------------------------------------------------------------------------------
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
  Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

==============================================================================
C       | 500.perlbench_r(peak)
------------------------------------------------------------------------------
Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R)
  64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation.  All rights reserved.
------------------------------------------------------------------------------

==============================================================================
C       | 502.gcc_r(peak)
------------------------------------------------------------------------------
Intel(R) oneAPI DPC++/C++ Compiler for applications running on IA-32, Version
  2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

==============================================================================
C       | 500.perlbench_r(base) 502.gcc_r(base) 505.mcf_r(base, peak)
        | 525.x264_r(base, peak) 557.xz_r(base, peak)
------------------------------------------------------------------------------
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
  Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

==============================================================================
C++     | 520.omnetpp_r(base, peak) 523.xalancbmk_r(base, peak)
        | 531.deepsjeng_r(base, peak) 541.leela_r(base, peak)
------------------------------------------------------------------------------
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
  Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

==============================================================================
Fortran | 548.exchange2_r(base, peak)
------------------------------------------------------------------------------
Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on
```

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Compiler Version Notes (Continued)

```
  Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation.  All rights reserved.
------------------------------------------------------------------------------
```

Base Compiler Invocation

C benchmarks:
icx

C++ benchmarks:
icpx

Fortran benchmarks:
ifort

Base Portability Flags

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -DSPEC_LP64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-w -std=c11 -m64 -Wl,-z,muldefs -xCORE-AVX512 -O3 -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries
-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin
-lqkmalloc

C++ benchmarks:
-w -m64 -Wl,-z,muldefs -xCORE-AVX512 -O3 -ffast-math -flto
-mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries

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Base Optimization Flags (Continued)

C++ benchmarks (continued):
-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin
-lqkmalloc

Fortran benchmarks:
-w -m64 -Wl,-z,muldefs -xCORE-AVX512 -O3 -ipo -no-prec-div
-qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte
-auto -mbranches-within-32B-boundaries
-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin
-lqkmalloc

Peak Compiler Invocation

C benchmarks (except as noted below):
icx

500.perlbench_r: icc

C++ benchmarks:
icpx

Fortran benchmarks:
ifort

Peak Portability Flags

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -D_FILE_OFFSET_BITS=64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64

Peak Optimization Flags

C benchmarks:

500.perlbench_r: `-Wl,-z,muldefs -prof-gen`(pass 1) `-prof-use`(pass 2)
`-xCORE-AVX512 -ipo -O3 -no-prec-div`
`-qopt-mem-layout-trans=4 -fno-strict-overflow`
`-mbranches-within-32B-boundaries`
`-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin`
`-lqkmalloc`

502.gcc_r: `-m32`
`-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/ia32_lin`
`-std=gnu89 -Wl,-z,muldefs -fprofile-generate`(pass 1)
`-fprofile-use=default.profdata`(pass 2) `-xCORE-AVX512 -flto`
`-Ofast`(pass 1) `-O3 -ffast-math -qopt-mem-layout-trans=4`
`-mbranches-within-32B-boundaries`
`-L/usr/local/jemalloc32-5.0.1/lib -ljemalloc`

505.mcf_r: `basepeak = yes`

525.x264_r: `-w -std=c11 -m64 -Wl,-z,muldefs -xCORE-AVX512 -flto`
`-O3 -ffast-math -qopt-mem-layout-trans=4 -fno-alias`
`-mbranches-within-32B-boundaries`
`-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin`
`-lqkmalloc`

557.xz_r: `basepeak = yes`

C++ benchmarks:

520.omnetpp_r: `basepeak = yes`

523.xalancbmk_r: `basepeak = yes`

531.deepsjeng_r: `basepeak = yes`

541.leela_r: `basepeak = yes`

Fortran benchmarks:

548.exchange2_r: `basepeak = yes`

The flags files that were used to format this result can be browsed at
`http://www.spec.org/cpu2017/flags/Intel-ic2021-official-linux64_revA.html`
`http://www.spec.org/cpu2017/flags/HPE-Platform-Flags-Intel-V1.0-ICX-revG.html`

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Intel-ic2021-official-linux64_revA.xml
http://www.spec.org/cpu2017/flags/HPE-Platform-Flags-Intel-V1.0-ICX-revG.xml

For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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