



SPEC CPU®2017 Floating Point Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

Inspur Corporation

SPECrate®2017_fp_base = 248

Inspur NS5162M5 (Intel Xeon Gold 6240R)

SPECrate®2017_fp_peak = 264

CPU2017 License: 3358

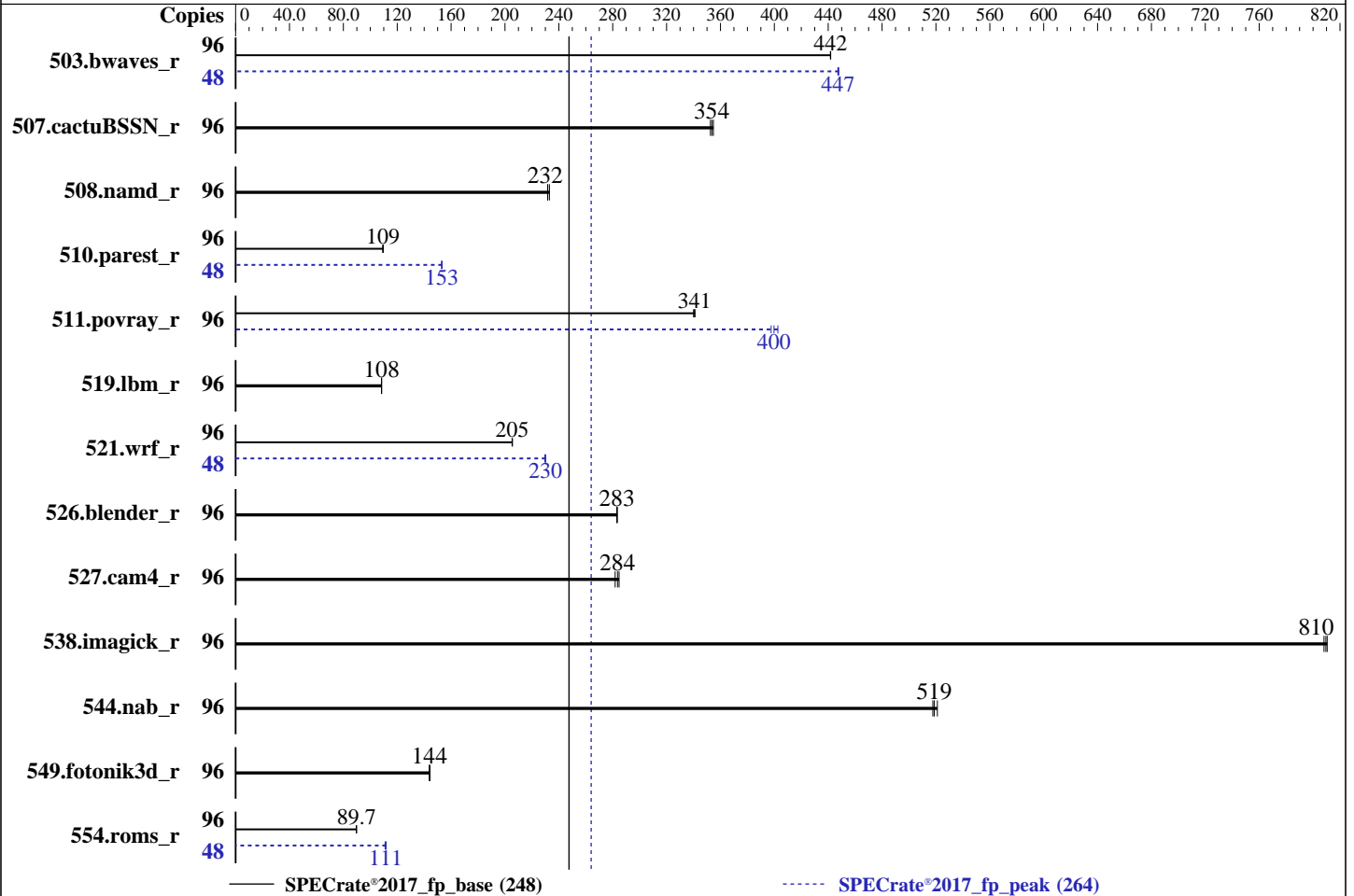
Test Sponsor: Inspur Corporation

Tested by: Inspur Corporation

Test Date: Aug-2020

Hardware Availability: Feb-2020

Software Availability: Apr-2020



Hardware

CPU Name: Intel Xeon Gold 6240R
 Max MHz: 4000
 Nominal: 2400
 Enabled: 48 cores, 2 chips, 2 threads/core
 Orderable: 1,2 chips
 Cache L1: 32 KB I + 32 KB D on chip per core
 L2: 1 MB I+D on chip per core
 L3: 35.75 MB I+D on chip per chip
 Other: None
 Memory: 384 GB (12 x 32 GB 2Rx4 PC4-2933Y-R)
 Storage: 1 x 1 TB SATA SSD
 Other: None

Software

OS: Red Hat Enterprise Linux release 8.1 (Ootpa) 4.18.0-147.el8.x86_64
 Compiler: C/C++: Version 19.1.1.217 of Intel C/C++ Compiler Build 20200306 for Linux; Fortran: Version 19.1.1.217 of Intel Fortran Compiler Build 20200306 for Linux
 Parallel: No
 Firmware: Version 4.1.6 released Jul-2019
 File System: xfs
 System State: Run level 3 (multi-user)
 Base Pointers: 64-bit
 Peak Pointers: 64-bit
 Other: jemalloc memory allocator V5.0.1
 Power Management: BIOS and OS set to prefer performance at the cost of additional power usage.



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Results Table

Benchmark	Base							Peak						
	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
503.bwaves_r	96	<u>2179</u>	<u>442</u>	2180	442	2179	442	48	<u>1076</u>	<u>447</u>	1076	447	1075	448
507.cactuBSSN_r	96	<u>344</u>	<u>354</u>	343	355	345	353	96	<u>344</u>	<u>354</u>	343	355	345	353
508.namd_r	96	394	232	391	233	<u>393</u>	<u>232</u>	96	394	232	391	233	<u>393</u>	<u>232</u>
510.parest_r	96	2291	110	2299	109	<u>2294</u>	<u>109</u>	48	<u>820</u>	<u>153</u>	819	153	821	153
511.povray_r	96	<u>658</u>	<u>341</u>	659	340	657	341	96	557	403	564	398	<u>561</u>	<u>400</u>
519.lbm_r	96	<u>934</u>	<u>108</u>	933	108	934	108	96	<u>934</u>	<u>108</u>	933	108	934	108
521.wrf_r	96	1046	206	1048	205	<u>1047</u>	<u>205</u>	48	467	230	<u>467</u>	<u>230</u>	468	230
526.blender_r	96	<u>516</u>	<u>283</u>	516	283	517	283	96	<u>516</u>	<u>283</u>	516	283	517	283
527.cam4_r	96	<u>592</u>	<u>284</u>	590	285	596	282	96	<u>592</u>	<u>284</u>	590	285	596	282
538.imagick_r	96	295	811	<u>295</u>	<u>810</u>	295	808	96	295	811	<u>295</u>	<u>810</u>	295	808
544.nab_r	96	310	521	312	518	<u>311</u>	<u>519</u>	96	310	521	312	518	<u>311</u>	<u>519</u>
549.fotonik3d_r	96	<u>2598</u>	<u>144</u>	2601	144	2593	144	96	<u>2598</u>	<u>144</u>	2601	144	2593	144
554.roms_r	96	1703	89.6	1700	89.8	<u>1700</u>	<u>89.7</u>	48	<u>684</u>	<u>111</u>	683	112	687	111

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Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Compiler Notes

The inconsistent Compiler version information under Compiler Version section is due to a discrepancy in Intel Compiler. The correct version of C/C++ compiler is: Version 19.1.1.217 Build 20200306 Compiler for Linux
The correct version of Fortran compiler is: Version 19.1.1.217 Build 20200306 Compiler for Linux

Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"
SCALING_GOVERNOR set to Performance

Environment Variables Notes

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/CPU2017/lib/intel64:/home/CPU2017/je5.0.1-64"
MALLOC_CONF = "retain:true"



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General Notes

Binaries compiled on a system with 1x Intel Core i9-7980XE CPU + 64GB RAM
memory using Redhat Enterprise Linux 8.0
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3> /proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:
numactl --interleave=all runcpu <etc>

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

jemalloc, a general purpose malloc implementation
built with the RedHat Enterprise 7.5,
and the system compiler gcc 4.8.5;
sources available from jemalloc.net or
<https://github.com/jemalloc/jemalloc/releases>

Platform Notes

BIOS configuration:
ENERGY_PERF_BIAS_CFG mode set to Performance
Hardware Prefetch set to Disable
VT Support set to Disable
C1E Support set to Disable
IMC (Integrated memory controller) Interleaving set to 1-way
Sub NUMA Cluster (SNC) set to Enable

Sysinfo program /home/CPU2017/bin/sysinfo
Rev: r6365 of 2019-08-21 295195f888a3d7edble6e46a485a0011
running on localhost.localdomain Sat Aug 15 03:59:26 2020

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
<https://www.spec.org/cpu2017/Docs/config.html#sysinfo>

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Gold 6240R CPU @ 2.40GHz
2 "physical id"s (chips)
96 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)

(Continued on next page)



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Platform Notes (Continued)

```
cpu cores : 24
siblings  : 48
physical 0: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 16 17 18 19 20 21 25 26 27 28 29
physical 1: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 16 17 18 19 20 21 25 26 27 28 29
```

```
From lscpu:
Architecture:          x86_64
CPU op-mode(s):        32-bit, 64-bit
Byte Order:             Little Endian
CPU(s):                 96
On-line CPU(s) list:   0-95
Thread(s) per core:    2
Core(s) per socket:    24
Socket(s):              2
NUMA node(s):          2
Vendor ID:              GenuineIntel
CPU family:             6
Model:                  85
Model name:             Intel(R) Xeon(R) Gold 6240R CPU @ 2.40GHz
Stepping:               7
CPU MHz:                3199.941
CPU max MHz:            4000.0000
CPU min MHz:            1000.0000
BogoMIPS:               4800.00
Virtualization:         VT-x
L1d cache:              32K
L1i cache:              32K
L2 cache:               1024K
L3 cache:               36608K
NUMA node0 CPU(s):     0-23,48-71
NUMA node1 CPU(s):     24-47,72-95
Flags:                  fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
aperfmpperf pni pclmulqdq dtes64 ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm
pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c
rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_l3 cdp_l3 invpcid_single
intel_ppin ssbd mba ibrs ibpb stibp ibrs_enhanced tpr_shadow vnmi flexpriority ept
vpid fsgsbase tsc_adjust bmil hle avx2 smep bmi2 erms invpcid rtm cqm mpx rdt_a
avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl
xsaveopt xsavec xgetbv1 xsaves cqm_llc cqm_occup_llc cqm_mbm_total cqm_mbm_local
dtherm ida arat pln pts hwp hwp_act_window hwp_epp hwp_pkg_req pku ospke avx512_vnni
md_clear flush_lld arch_capabilities
```

```
/proc/cpuinfo cache data
cache size : 36608 KB
```

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Platform Notes (Continued)

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.

```
available: 2 nodes (0-1)
node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 48 49 50 51
52 53 54 55 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 71
node 0 size: 192074 MB
node 0 free: 191510 MB
node 1 cpus: 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 72
73 74 75 76 77 78 79 80 81 82 83 84 85 86 87 88 89 90 91 92 93 94 95
node 1 size: 193526 MB
node 1 free: 193201 MB
node distances:
node  0  1
  0:  10  21
  1:  21  10
```

```
From /proc/meminfo
MemTotal:      394855356 kB
HugePages_Total:      0
Hugepagesize:    2048 kB
```

```
From /etc/*release* /etc/*version*
os-release:
NAME="Red Hat Enterprise Linux"
VERSION="8.1 (Ootpa)"
ID="rhel"
ID_LIKE="fedora"
VERSION_ID="8.1"
PLATFORM_ID="platform:el8"
PRETTY_NAME="Red Hat Enterprise Linux 8.1 (Ootpa)"
ANSI_COLOR="0;31"
redhat-release: Red Hat Enterprise Linux release 8.1 (Ootpa)
system-release: Red Hat Enterprise Linux release 8.1 (Ootpa)
system-release-cpe: cpe:/o:redhat:enterprise_linux:8.1:ga
```

```
uname -a:
Linux localhost.localdomain 4.18.0-147.el8.x86_64 #1 SMP Thu Sep 26 15:52:44 UTC 2019
x86_64 x86_64 x86_64 GNU/Linux
```

Kernel self-reported vulnerability status:

```
CVE-2018-3620 (L1 Terminal Fault):      Not affected
Microarchitectural Data Sampling:      Not affected
CVE-2017-5754 (Meltdown):               Not affected
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled
via prctl and seccomp
CVE-2017-5753 (Spectre variant 1):      Mitigation: usercopy/swapgs barriers and __user
```

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Platform Notes (Continued)

CVE-2017-5715 (Spectre variant 2):
pointer sanitization
Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling

run-level 3 Aug 15 03:58

SPEC is set to: /home/CPU2017

Filesystem	Type	Size	Used	Avail	Use%	Mounted on
/dev/mapper/rhel-home	xfs	876G	69G	808G	8%	/home

From /sys/devices/virtual/dmi/id

BIOS: American Megatrends Inc. 4.1.6 07/06/2019
Vendor: Inspur
Product: NS5162M5
Serial: 220826449

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

Memory:

4x NO DIMM NO DIMM
12x Samsung M393A4G43AB3-CVF 32 GB 2 rank 2933

(End of data from sysinfo program)

Compiler Version Notes

```
=====
C          | 519.lbm_r(base, peak) 538.imagick_r(base, peak)
          | 544.nab_r(base, peak)
-----
```

Intel(R) C Compiler for applications running on Intel(R) 64, Version 2021.1
NextGen Build 20200304
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

```
=====
C++       | 508.namd_r(base, peak) 510.parest_r(base, peak)
-----
```

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Compiler Version Notes (Continued)

C++, C | 511.povray_r(base) 526.blender_r(base, peak)

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NextGen Build 20200304
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Intel(R) C Compiler for applications running on Intel(R) 64, Version 2021.1
NextGen Build 20200304
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

=====
C++, C | 511.povray_r(peak)

Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.1.1.217 Build 20200306
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.1.1.217 Build 20200306
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

=====
C++, C | 511.povray_r(base) 526.blender_r(base, peak)

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=====
C++, C | 511.povray_r(peak)

Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.1.1.217 Build 20200306
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.1.1.217 Build 20200306
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

=====
C++, C, Fortran | 507.cactuBSSN_r(base, peak)

Intel(R) C++ Compiler for applications running on Intel(R) 64, Version 2021.1

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 Intel(R) C Compiler for applications running on Intel(R) 64, Version 2021.1
 NextGen Build 20200304
 Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
 Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
 64, Version 19.1.1.217 Build 20200306
 Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

```
=====
Fortran          | 503.bwaves_r(base, peak) 549.fotonik3d_r(base, peak)
                  | 554.roms_r(base, peak)
=====
```

Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
 64, Version 19.1.1.217 Build 20200306
 Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

```
=====
Fortran, C       | 521.wrf_r(base) 527.cam4_r(base, peak)
=====
```

Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
 64, Version 19.1.1.217 Build 20200306
 Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
 Intel(R) C Compiler for applications running on Intel(R) 64, Version 2021.1
 NextGen Build 20200304
 Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

```
=====
Fortran, C       | 521.wrf_r(peak)
=====
```

Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
 64, Version 19.1.1.217 Build 20200306
 Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
 Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
 Version 19.1.1.217 Build 20200306
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```
=====
Fortran, C       | 521.wrf_r(base) 527.cam4_r(base, peak)
=====
```

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Fortran, C | 521.wrf_r(peak)

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Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.1.1.217 Build 20200306
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Base Compiler Invocation

C benchmarks:

icc

C++ benchmarks:

icpc

Fortran benchmarks:

ifort

Benchmarks using both Fortran and C:

ifort icc

Benchmarks using both C and C++:

icpc icc

Benchmarks using Fortran, C, and C++:

icpc icc ifort

Base Portability Flags

503.bwaves_r: -DSPEC_LP64
507.cactuBSSN_r: -DSPEC_LP64
508.namd_r: -DSPEC_LP64
510.parest_r: -DSPEC_LP64
511.povray_r: -DSPEC_LP64

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Base Portability Flags (Continued)

```
519.lbm_r: -DSPEC_LP64
521.wrf_r: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
526.blender_r: -DSPEC_LP64 -DSPEC_LINUX -funsigned-char
527.cam4_r: -DSPEC_LP64 -DSPEC_CASE_FLAG
538.imagick_r: -DSPEC_LP64
544.nab_r: -DSPEC_LP64
549.fotonik3d_r: -DSPEC_LP64
554.roms_r: -DSPEC_LP64
```

Base Optimization Flags

C benchmarks:

```
-m64 -qnextgen -std=c11
-Wl,-plugin-opt=-x86-branches-within-32B-boundaries -Wl,-z,muldefs
-fuse-ld=gold -xCORE-AVX512 -Ofast -ffast-math -flto -mfpmath=sse
-funroll-loops -qopt-mem-layout-trans=4
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc
```

C++ benchmarks:

```
-m64 -qnextgen -Wl,-plugin-opt=-x86-branches-within-32B-boundaries
-Wl,-z,muldefs -fuse-ld=gold -xCORE-AVX512 -Ofast -ffast-math -flto
-mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc
```

Fortran benchmarks:

```
-m64 -Wl,-plugin-opt=-x86-branches-within-32B-boundaries -Wl,-z,muldefs
-fuse-ld=gold -xCORE-AVX512 -O3 -ipo -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-multiple-gather-scatter-by-shuffles
-qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte
-auto -mbranches-within-32B-boundaries
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc
```

Benchmarks using both Fortran and C:

```
-m64 -qnextgen -std=c11
-Wl,-plugin-opt=-x86-branches-within-32B-boundaries -Wl,-z,muldefs
-fuse-ld=gold -xCORE-AVX512 -Ofast -ffast-math -flto -mfpmath=sse
-funroll-loops -qopt-mem-layout-trans=4 -O3 -ipo -no-prec-div
-qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles -nostandard-realloc-lhs
-align array32byte -auto -mbranches-within-32B-boundaries
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc
```

Benchmarks using both C and C++:

```
-m64 -qnextgen -std=c11
```

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Base Optimization Flags (Continued)

Benchmarks using both C and C++ (continued):

```
-Wl,-plugin-opt=-x86-branches-within-32B-boundaries -Wl,-z,muldefs
-fuse-ld=gold -xCORE-AVX512 -Ofast -ffast-math -flto -mfpmath=sse
-funroll-loops -qopt-mem-layout-trans=4
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc
```

Benchmarks using Fortran, C, and C++:

```
-m64 -qnextgen -std=c11
-Wl,-plugin-opt=-x86-branches-within-32B-boundaries -Wl,-z,muldefs
-fuse-ld=gold -xCORE-AVX512 -Ofast -ffast-math -flto -mfpmath=sse
-funroll-loops -qopt-mem-layout-trans=4 -O3 -ipo -no-prec-div
-qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles -nostandard-realloc-lhs
-align array32byte -auto -mbranches-within-32B-boundaries
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc
```

Peak Compiler Invocation

C benchmarks:

icc

C++ benchmarks:

icpc

Fortran benchmarks:

ifort

Benchmarks using both Fortran and C:

ifort icc

Benchmarks using both C and C++:

icpc icc

Benchmarks using Fortran, C, and C++:

icpc icc ifort

Peak Portability Flags

Same as Base Portability Flags



SPEC CPU®2017 Floating Point Rate Result

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Inspur Corporation

SPECrate®2017_fp_base = 248

Inspur NS5162M5 (Intel Xeon Gold 6240R)

SPECrate®2017_fp_peak = 264

CPU2017 License: 3358

Test Sponsor: Inspur Corporation

Tested by: Inspur Corporation

Test Date: Aug-2020

Hardware Availability: Feb-2020

Software Availability: Apr-2020

Peak Optimization Flags

C benchmarks:

519.lbm_r: basepeak = yes

538.imagick_r: basepeak = yes

544.nab_r: basepeak = yes

C++ benchmarks:

508.namd_r: basepeak = yes

510.parest_r: -m64 -qnextgen

-Wl,-plugin-opt=-x86-branches-within-32B-boundaries
-Wl,-z,muldefs -fuse-ld=gold -xCORE-AVX512 -Ofast
-ffast-math -flto -mfpmath=sse -funroll-loops
-qopt-mem-layout-trans=4 -L/usr/local/jemalloc64-5.0.1/lib
-ljemalloc

Fortran benchmarks:

503.bwaves_r: -m64 -Wl,-plugin-opt=-x86-branches-within-32B-boundaries

-Wl,-z,muldefs -fuse-ld=gold -xCORE-AVX512 -O3 -ipo
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles
-qopt-mem-layout-trans=4 -nostandard-realloc-lhs
-align array32byte -auto -mbranches-within-32B-boundaries
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

549.fotonik3d_r: basepeak = yes

554.roms_r: Same as 503.bwaves_r

Benchmarks using both Fortran and C:

521.wrf_r: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX512 -O3

-ipo -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles
-qopt-mem-layout-trans=4 -mbranches-within-32B-boundaries
-nostandard-realloc-lhs -align array32byte -auto
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

527.cam4_r: basepeak = yes

Benchmarks using both C and C++:

(Continued on next page)



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Peak Optimization Flags (Continued)

```
511.povray_r: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX512 -O3
-ipo -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles
-qopt-mem-layout-trans=4 -mbranches-within-32B-boundaries
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc
```

526.blender_r: basepeak = yes

Benchmarks using Fortran, C, and C++:

507.cactuBSSN_r: basepeak = yes

The flags files that were used to format this result can be browsed at

http://www.spec.org/cpu2017/flags/Intel-ic19.1u1-official-linux64_revA.html

<http://www.spec.org/cpu2017/flags/Inspur-Platform-Settings-V1.9.html>

You can also download the XML flags sources by saving the following links:

http://www.spec.org/cpu2017/flags/Intel-ic19.1u1-official-linux64_revA.xml

<http://www.spec.org/cpu2017/flags/Inspur-Platform-Settings-V1.9.xml>

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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