



# SPEC CPU®2017 Integer Speed Result

Copyright 2017-2019 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS C480 M5 (Intel Xeon Platinum 8260Y, 2.40GHz)

SPECspeed®2017\_int\_base = 10.4

SPECspeed®2017\_int\_peak = Not Run

CPU2017 License: 9019

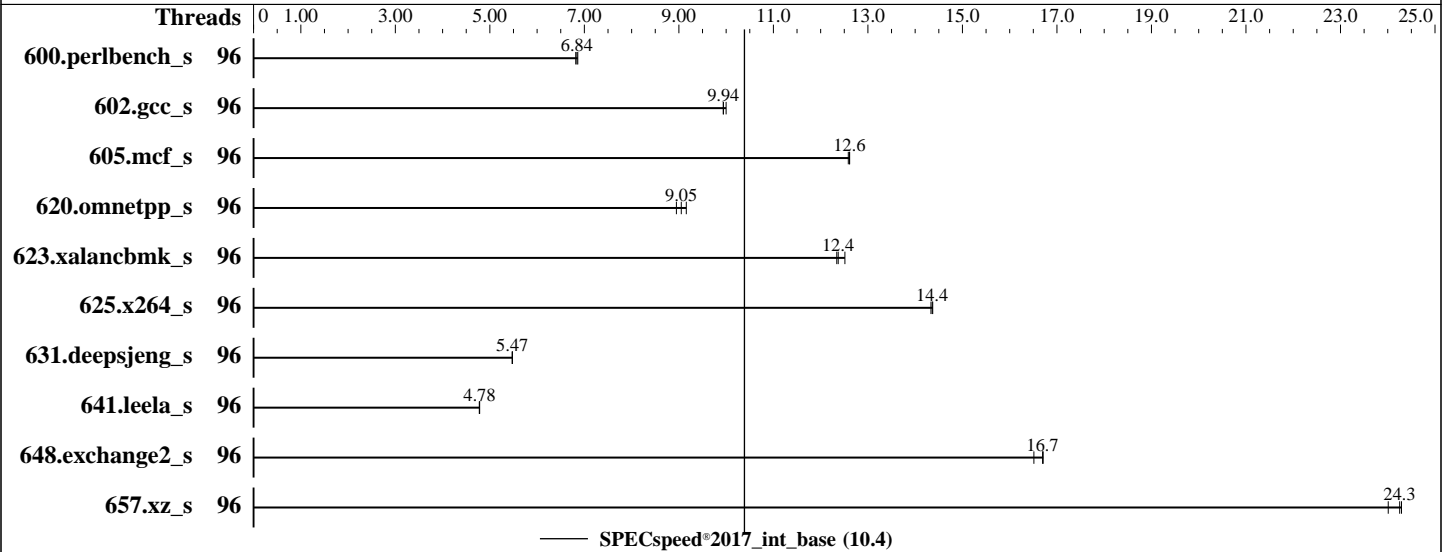
Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Nov-2019

Hardware Availability: Apr-2019

Software Availability: May-2019



### Hardware

CPU Name: Intel Xeon Platinum 8260Y  
 Max MHz: 3900  
 Nominal: 2400  
 Enabled: 96 cores, 4 chips  
 Orderable: 2,4 Chips  
 Cache L1: 32 KB I + 32 KB D on chip per core  
 L2: 1 MB I+D on chip per core  
 L3: 35.75 MB I+D on chip per chip  
 Other: None  
 Memory: 1536 GB (48 x 32 GB 2Rx4 PC4-2933V-R)  
 Storage: 1 x 1.9 TB SSD SAS  
 Other: None

### Software

OS: SUSE Linux Enterprise Server 15 (x86\_64) 4.12.14-23-default  
 Compiler: C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux;  
 Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux  
 Parallel: Yes  
 Firmware: Version 4.0.3 released Mar-2019  
 File System: xfs  
 System State: Run level 3 (multi-user)  
 Base Pointers: 64-bit  
 Peak Pointers: Not Applicable  
 Other: jemalloc memory allocator V5.0.1  
 Power Management: default



# SPEC CPU®2017 Integer Speed Result

Copyright 2017-2019 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS C480 M5 (Intel Xeon Platinum 8260Y, 2.40GHz)

SPECspeed®2017\_int\_base = 10.4

SPECspeed®2017\_int\_peak = Not Run

CPU2017 License: 9019  
Test Sponsor: Cisco Systems  
Tested by: Cisco Systems

Test Date: Nov-2019  
Hardware Availability: Apr-2019  
Software Availability: May-2019

## Results Table

Benchmark	Base							Peak						
	Threads	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Threads	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
600.perlbench_s	96	<b><u>259</u></b>	<b><u>6.84</u></b>	260	6.82	259	6.86							
602.gcc_s	96	398	10.0	401	9.94	<b><u>401</u></b>	<b><u>9.94</u></b>							
605.mcf_s	96	374	12.6	<b><u>374</u></b>	<b><u>12.6</u></b>	375	12.6							
620.omnetpp_s	96	178	9.16	<b><u>180</u></b>	<b><u>9.05</u></b>	182	8.95							
623.xalancbmk_s	96	<b><u>115</u></b>	<b><u>12.4</u></b>	115	12.3	113	12.5							
625.x264_s	96	123	14.4	123	14.3	<b><u>123</u></b>	<b><u>14.4</u></b>							
631.deepsjeng_s	96	<b><u>262</u></b>	<b><u>5.47</u></b>	262	5.47	262	5.48							
641.leela_s	96	357	4.78	<b><u>357</u></b>	<b><u>4.78</u></b>	357	4.78							
648.exchange2_s	96	<b><u>176</u></b>	<b><u>16.7</u></b>	176	16.7	178	16.5							
657.xz_s	96	257	24.0	<b><u>255</u></b>	<b><u>24.3</u></b>	254	24.3							

SPECspeed®2017\_int\_base = 10.4

SPECspeed®2017\_int\_peak = Not Run

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

## Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

## Environment Variables Notes

Environment variables set by runcpu before the start of the run:  
KMP\_AFFINITY = "granularity=fine,compact"  
LD\_LIBRARY\_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-64"  
OMP\_STACKSIZE = "192M"

## General Notes

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM memory using Redhat Enterprise Linux 7.5  
Transparent Huge Pages enabled by default  
Prior to runcpu invocation  
Filesystem page cache synced and cleared with:  
sync; echo 3> /proc/sys/vm/drop\_caches  
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.  
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.  
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.  
jemalloc, a general purpose malloc implementation built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5 sources available from jemalloc.net or <https://github.com/jemalloc/jemalloc/releases>



# SPEC CPU®2017 Integer Speed Result

Copyright 2017-2019 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS C480 M5 (Intel Xeon Platinum 8260Y, 2.40GHz)

SPECspeed®2017\_int\_base = 10.4

SPECspeed®2017\_int\_peak = Not Run

**CPU2017 License:** 9019

**Test Sponsor:** Cisco Systems

**Tested by:** Cisco Systems

**Test Date:** Nov-2019

**Hardware Availability:** Apr-2019

**Software Availability:** May-2019

## Platform Notes

### BIOS Settings:

Intel HyperThreading Technology set to Disabled  
CPU performance set to Enterprise  
Power Performance Tuning set to OS Controls  
SNC set to Disabled  
Patrol Scrub set to Disabled

sysinfo program /home/cpu2017/bin/sysinfo  
Rev: r6365 of 2019-08-21 295195f888a3d7edble6e46a485a0011  
running on linux-mz3p Sat Nov 9 19:29:18 2019

SUT (System Under Test) info as seen by some common utilities.  
For more information on this section, see  
<https://www.spec.org/cpu2017/Docs/config.html#sysinfo>

### From /proc/cpuinfo

```
model name      : Intel(R) Xeon(R) Platinum 8260C CPU @ 2.40GHz
 4 "physical id"s (chips)
 96 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following
excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores      : 24
siblings       : 24
physical 0:    : cores 0 1 2 3 4 5 6 8 9 10 11 12 13 16 17 18 19 20 21 25 26 27 28 29
physical 1:    : cores 0 1 2 3 4 5 6 9 10 11 12 13 16 17 18 19 20 21 24 25 26 27 28 29
physical 2:    : cores 0 1 2 3 4 5 6 8 9 10 11 12 13 16 17 18 19 20 21 25 26 27 28 29
physical 3:    : cores 0 1 2 3 4 5 6 8 10 11 12 13 16 17 18 19 20 21 24 25 26 27 28 29
```

### From lscpu:

```
Architecture:    x86_64
CPU op-mode(s):  32-bit, 64-bit
Byte Order:      Little Endian
CPU(s):          96
On-line CPU(s) list: 0-95
Thread(s) per core: 1
Core(s) per socket: 24
Socket(s):       4
NUMA node(s):   4
Vendor ID:      GenuineIntel
CPU family:     6
Model:          85
Model name:     Intel(R) Xeon(R) Platinum 8260C CPU @ 2.40GHz
Stepping:       6
CPU MHz:        2400.000
CPU max MHz:    3900.0000
CPU min MHz:    1000.0000
BogoMIPS:       4800.00
```

(Continued on next page)



# SPEC CPU®2017 Integer Speed Result

Copyright 2017-2019 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS C480 M5 (Intel Xeon Platinum 8260Y, 2.40GHz)

SPECspeed®2017\_int\_base = 10.4

SPECspeed®2017\_int\_peak = Not Run

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems

**Test Date:** Nov-2019  
**Hardware Availability:** Apr-2019  
**Software Availability:** May-2019

### Platform Notes (Continued)

```

Virtualization:      VT-x
L1d cache:          32K
L1i cache:          32K
L2 cache:           1024K
L3 cache:           36608K
NUMA node0 CPU(s): 0-23
NUMA node1 CPU(s): 24-47
NUMA node2 CPU(s): 48-71
NUMA node3 CPU(s): 72-95
Flags:              fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
aperfmpperf tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3
sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt
tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault
epb cat_l3 cdp_l3 invpcid_single mba tpr_shadow vnmi flexpriority ept vpid fsgsbase
tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm cqm mpx rdt_a avx512f avx512dq
rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl xsaveopt xsavec
xgetbv1 xsaves cqm_llc cqm_occup_llc cqm_mbm_total cqm_mbm_local ibpb ibrs stibp
dtherm ida arat pln pts hwp hwp_act_window hwp_epp hwp_pkg_req pku ospke avx512_vnmi
arch_capabilities ssbd

```

```

/proc/cpuinfo cache data
cache size : 36608 KB

```

```

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a
physical chip.
available: 4 nodes (0-3)
node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23
node 0 size: 385623 MB
node 0 free: 385243 MB
node 1 cpus: 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47
node 1 size: 387028 MB
node 1 free: 386594 MB
node 2 cpus: 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 71
node 2 size: 387056 MB
node 2 free: 386854 MB
node 3 cpus: 72 73 74 75 76 77 78 79 80 81 82 83 84 85 86 87 88 89 90 91 92 93 94 95
node 3 size: 387054 MB
node 3 free: 386694 MB
node distances:
node  0  1  2  3
0:  10  21  21  21
1:  21  10  21  21
2:  21  21  10  21
3:  21  21  21  10

```

(Continued on next page)



# SPEC CPU®2017 Integer Speed Result

Copyright 2017-2019 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS C480 M5 (Intel Xeon Platinum 8260Y, 2.40GHz)

SPECspeed®2017\_int\_base = 10.4

SPECspeed®2017\_int\_peak = Not Run

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems

**Test Date:** Nov-2019  
**Hardware Availability:** Apr-2019  
**Software Availability:** May-2019

### Platform Notes (Continued)

From /proc/meminfo

MemTotal: 1583884788 kB  
HugePages\_Total: 0  
Hugepagesize: 2048 kB

From /etc/\*release\* /etc/\*version\*

os-release:  
NAME="SLES"  
VERSION="15"  
VERSION\_ID="15"  
PRETTY\_NAME="SUSE Linux Enterprise Server 15"  
ID="sles"  
ID\_LIKE="suse"  
ANSI\_COLOR="0;32"  
CPE\_NAME="cpe:/o:suse:sles:15"

uname -a:

Linux linux-mz3p 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)  
x86\_64 x86\_64 x86\_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2018-3620 (L1 Terminal Fault): No status reported  
Microarchitectural Data Sampling: No status reported  
CVE-2017-5754 (Meltdown): Not affected  
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled via prctl and seccomp  
CVE-2017-5753 (Spectre variant 1): Mitigation: \_\_user pointer sanitization  
CVE-2017-5715 (Spectre variant 2): Mitigation: Indirect Branch Restricted Speculation, IBPB, IBRS\_FW

run-level 3 Nov 9 19:26

SPEC is set to: /home/cpu2017

Filesystem	Type	Size	Used	Avail	Use%	Mounted on
/dev/sdb2	xfs	549G	85G	465G	16%	/

From /sys/devices/virtual/dmi/id

BIOS: Cisco Systems, Inc. C480M5.4.0.3.32.0301190121 03/01/2019  
Vendor: Cisco  
Product: UCSC-C480-M5  
Serial: FCH2238W019

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

(Continued on next page)



# SPEC CPU®2017 Integer Speed Result

Copyright 2017-2019 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS C480 M5 (Intel Xeon Platinum 8260Y, 2.40GHz)

SPECspeed®2017\_int\_base = 10.4

SPECspeed®2017\_int\_peak = Not Run

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems

**Test Date:** Nov-2019  
**Hardware Availability:** Apr-2019  
**Software Availability:** May-2019

### Platform Notes (Continued)

Memory:

48x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2934

(End of data from sysinfo program)

The marketing name for the processor in this result, which appears in the CPU name and hardware model areas, is different from sysinfo because a pre-production processor was used. The pre-production processor differs from the production processor in name only.

### Compiler Version Notes

```
=====
C          | 600.perlbench_s(base) 602.gcc_s(base) 605.mcf_s(base)
          | 625.x264_s(base) 657.xz_s(base)
-----
```

```
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
-----
```

```
=====
C++       | 620.omnetpp_s(base) 623.xalanbmk_s(base) 631.deepsjeng_s(base)
          | 641.leela_s(base)
-----
```

```
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
-----
```

```
=====
Fortran   | 648.exchange2_s(base)
-----
```

```
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
-----
```

### Base Compiler Invocation

C benchmarks:

icc -m64 -std=c11

C++ benchmarks:

icpc -m64

(Continued on next page)



# SPEC CPU®2017 Integer Speed Result

Copyright 2017-2019 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS C480 M5 (Intel Xeon Platinum 8260Y, 2.40GHz)

SPECspeed®2017\_int\_base = 10.4

SPECspeed®2017\_int\_peak = Not Run

**CPU2017 License:** 9019

**Test Sponsor:** Cisco Systems

**Tested by:** Cisco Systems

**Test Date:** Nov-2019

**Hardware Availability:** Apr-2019

**Software Availability:** May-2019

## Base Compiler Invocation (Continued)

Fortran benchmarks:

```
ifort -m64
```

## Base Portability Flags

```
600.perlbench_s: -DSPEC_LP64 -DSPEC_LINUX_X64
602.gcc_s: -DSPEC_LP64
605.mcf_s: -DSPEC_LP64
620.omnetpp_s: -DSPEC_LP64
623.xalancbmk_s: -DSPEC_LP64 -DSPEC_LINUX
625.x264_s: -DSPEC_LP64
631.deepsjeng_s: -DSPEC_LP64
641.leela_s: -DSPEC_LP64
648.exchange2_s: -DSPEC_LP64
657.xz_s: -DSPEC_LP64
```

## Base Optimization Flags

C benchmarks:

```
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP
-L/usr/local/je5.0.1-64/lib -ljemalloc
```

C++ benchmarks:

```
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc
```

Fortran benchmarks:

```
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-mem-layout-trans=4
-nostandard-realloc-lhs
```

The flags files that were used to format this result can be browsed at

<http://www.spec.org/cpu2017/flags/Intel-ic19.0ul-official-linux64.2019-07-09.html>

<http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revJ.html>

You can also download the XML flags sources by saving the following links:

<http://www.spec.org/cpu2017/flags/Intel-ic19.0ul-official-linux64.2019-07-09.xml>

<http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revJ.xml>



# SPEC CPU®2017 Integer Speed Result

Copyright 2017-2019 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS C480 M5 (Intel Xeon Platinum 8260Y, 2.40GHz)

SPECspeed®2017\_int\_base = 10.4

SPECspeed®2017\_int\_peak = Not Run

**CPU2017 License:** 9019

**Test Sponsor:** Cisco Systems

**Tested by:** Cisco Systems

**Test Date:** Nov-2019

**Hardware Availability:** Apr-2019

**Software Availability:** May-2019

SPEC CPU and SPECspeed are registered trademarks of the Standard Performance Evaluation Corporation. All other brand and product names appearing in this result are trademarks or registered trademarks of their respective holders.

For questions about this result, please contact the tester. For other inquiries, please contact [info@spec.org](mailto:info@spec.org).

Tested with SPEC CPU®2017 v1.1.0 on 2019-11-09 22:29:17-0500.  
Report generated on 2019-12-17 17:45:45 by CPU2017 PDF formatter v6255.  
Originally published on 2019-12-17.