



# SPEC CPU®2017 Integer Speed Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS C480 M5 (Intel Xeon Gold 6242, 2.80GHz)

SPECspeed®2017\_int\_base = 10.1

SPECspeed®2017\_int\_peak = Not Run

CPU2017 License: 9019

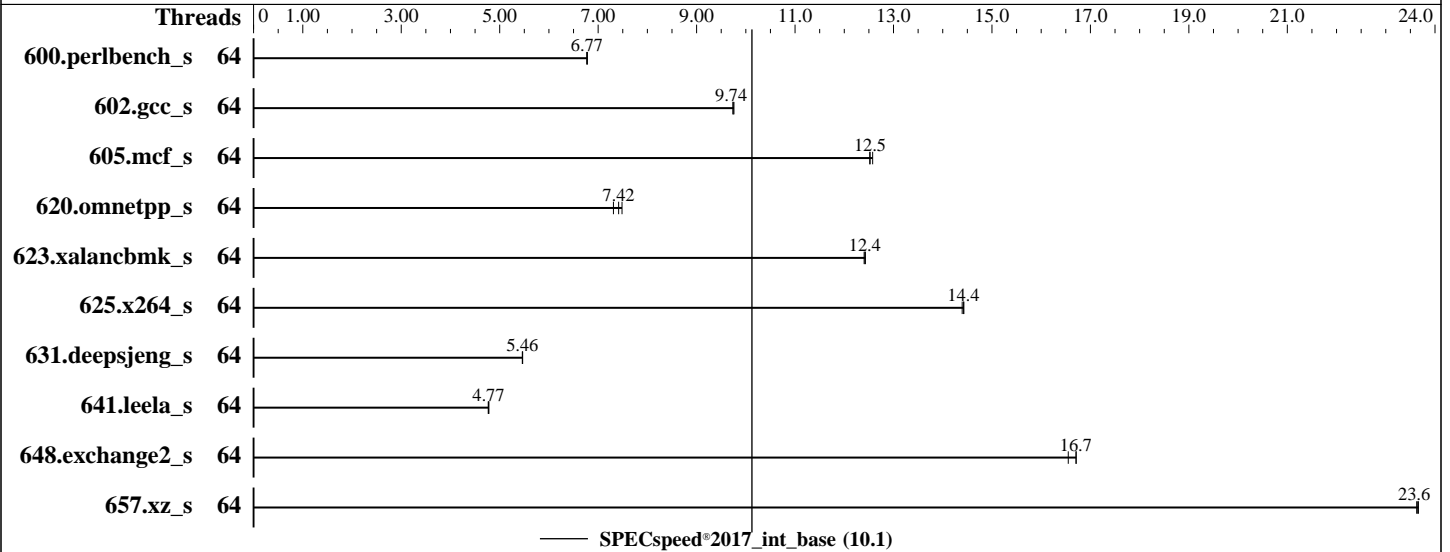
Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Oct-2019

Hardware Availability: Apr-2019

Software Availability: May-2019



### Hardware

CPU Name: Intel Xeon Gold 6242  
 Max MHz: 3900  
 Nominal: 2800  
 Enabled: 64 cores, 4 chips  
 Orderable: 2,4 Chips  
 Cache L1: 32 KB I + 32 KB D on chip per core  
 L2: 1 MB I+D on chip per core  
 L3: 22 MB I+D on chip per chip  
 Other: None  
 Memory: 1536 GB (48 x 32 GB 2Rx4 PC4-2933V-R)  
 Storage: 1 x 300 GB 15K RPM SAS HDD  
 Other: None

### Software

OS: SUSE Linux Enterprise Server 15 (x86\_64) 4.12.14-25.28-default  
 Compiler: C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux;  
 Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux  
 Parallel: Yes  
 Firmware: Version 4.0.4g released Jul-2019  
 File System: xfs  
 System State: Run level 3 (multi-user)  
 Base Pointers: 64-bit  
 Peak Pointers: Not Applicable  
 Other: jemalloc memory allocator V5.0.1  
 Power Management: default



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## Results Table

Benchmark	Base							Peak						
	Threads	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Threads	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
600.perlbench_s	64	<b><u>262</u></b>	<b><u>6.77</u></b>	262	6.77	262	6.78							
602.gcc_s	64	<b><u>409</u></b>	<b><u>9.74</u></b>	409	9.74	408	9.76							
605.mcf_s	64	375	12.6	<b><u>377</u></b>	<b><u>12.5</u></b>	377	12.5							
620.omnetpp_s	64	218	7.49	<b><u>220</u></b>	<b><u>7.42</u></b>	223	7.31							
623.xalancbmk_s	64	114	12.4	<b><u>114</u></b>	<b><u>12.4</u></b>	114	12.4							
625.x264_s	64	<b><u>122</u></b>	<b><u>14.4</u></b>	122	14.4	123	14.4							
631.deepsjeng_s	64	<b><u>262</u></b>	<b><u>5.46</u></b>	262	5.47	262	5.46							
641.leela_s	64	358	4.77	<b><u>357</u></b>	<b><u>4.77</u></b>	357	4.78							
648.exchange2_s	64	178	16.5	<b><u>176</u></b>	<b><u>16.7</u></b>	176	16.7							
657.xz_s	64	261	23.7	<b><u>261</u></b>	<b><u>23.6</u></b>	262	23.6							

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Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

## Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

## Environment Variables Notes

Environment variables set by runcpu before the start of the run:  
KMP\_AFFINITY = "granularity=fine,compact"  
LD\_LIBRARY\_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-64"  
OMP\_STACKSIZE = "192M"

## General Notes

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM memory using Redhat Enterprise Linux 7.5  
Transparent Huge Pages enabled by default  
Prior to runcpu invocation  
Filesystem page cache synced and cleared with:  
sync; echo 3> /proc/sys/vm/drop\_caches  
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.  
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.  
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.  
jemalloc, a general purpose malloc implementation built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5 sources available from jemalloc.net or <https://github.com/jemalloc/jemalloc/releases>



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## Platform Notes

BIOS Settings:

Intel HyperThreading Technology set to Disabled

CPU performance set to Enterprise

Power Performance Tuning set to OS Controls

SNC set to Disabled

Patrol Scrub set to Disabled

Sysinfo program /home/cpu2017/bin/sysinfo

Rev: r6365 of 2019-08-21 295195f888a3d7edble6e46a485a0011

running on linux-75co Sun Oct 6 12:51:08 2019

SUT (System Under Test) info as seen by some common utilities.

For more information on this section, see

<https://www.spec.org/cpu2017/Docs/config.html#sysinfo>

From /proc/cpuinfo

model name : Intel(R) Xeon(R) Gold 6242 CPU @ 2.80GHz

4 "physical id"s (chips)

64 "processors"

cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)

cpu cores : 16

siblings : 16

physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

physical 1: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

physical 2: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

physical 3: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

From lscpu:

Architecture: x86\_64

CPU op-mode(s): 32-bit, 64-bit

Byte Order: Little Endian

CPU(s): 64

On-line CPU(s) list: 0-63

Thread(s) per core: 1

Core(s) per socket: 16

Socket(s): 4

NUMA node(s): 4

Vendor ID: GenuineIntel

CPU family: 6

Model: 85

Model name: Intel(R) Xeon(R) Gold 6242 CPU @ 2.80GHz

Stepping: 6

CPU MHz: 2800.000

CPU max MHz: 3900.0000

CPU min MHz: 1200.0000

BogoMIPS: 5600.00

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### Platform Notes (Continued)

```

Virtualization:      VT-x
L1d cache:          32K
L1i cache:          32K
L2 cache:           1024K
L3 cache:           22528K
NUMA node0 CPU(s): 0-15
NUMA node1 CPU(s): 16-31
NUMA node2 CPU(s): 32-47
NUMA node3 CPU(s): 48-63
Flags:              fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
aperfmpperf pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16
xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave
avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_l3 cdp_l3
invpcid_single intel_ppin ssbd mba ibrs ibpb stibp ibrs_enhanced tpr_shadow vnmi
flexpriority ept vpid fsgsbase tsc_adjust bml hle avx2 smep bmi2 erms invpcid rtm
cqm mpx rdt_a avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd
avx512bw avx512vl xsaveopt xsavec xgetbv1 xsaves cqm_llc cqm_occup_llc cqm_mbm_total
cqm_mbm_local dtherm ida arat pln pts hwp hwp_act_window hwp_epp hwp_pkg_req pku
ospke avx512_vnni flush_l1d arch_capabilities

```

```

/proc/cpuinfo cache data
cache size : 22528 KB

```

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.

```

available: 4 nodes (0-3)
node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
node 0 size: 385637 MB
node 0 free: 385342 MB
node 1 cpus: 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31
node 1 size: 387068 MB
node 1 free: 386512 MB
node 2 cpus: 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47
node 2 size: 387068 MB
node 2 free: 386899 MB
node 3 cpus: 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63
node 3 size: 387038 MB
node 3 free: 386846 MB
node distances:
node  0  1  2  3
 0:  10  21  21  21
 1:  21  10  21  21
 2:  21  21  10  21
 3:  21  21  21  10

```

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### Platform Notes (Continued)

From /proc/meminfo

MemTotal: 1583936776 kB  
HugePages\_Total: 0  
Hugepagesize: 2048 kB

From /etc/\*release\* /etc/\*version\*

os-release:  
NAME="SLES"  
VERSION="15"  
VERSION\_ID="15"  
PRETTY\_NAME="SUSE Linux Enterprise Server 15"  
ID="sles"  
ID\_LIKE="suse"  
ANSI\_COLOR="0;32"  
CPE\_NAME="cpe:/o:suse:sles:15"

uname -a:

Linux linux-75co 4.12.14-25.28-default #1 SMP Wed Jan 16 20:00:47 UTC 2019 (dd6077c)  
x86\_64 x86\_64 x86\_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2018-3620 (L1 Terminal Fault): Not affected  
Microarchitectural Data Sampling: No status reported  
CVE-2017-5754 (Meltdown): Not affected  
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled via prctl and seccomp  
CVE-2017-5753 (Spectre variant 1): Mitigation: \_\_user pointer sanitization  
CVE-2017-5715 (Spectre variant 2): Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling

run-level 3 Oct 6 12:43

SPEC is set to: /home/cpu2017

Filesystem	Type	Size	Used	Avail	Use%	Mounted on
/dev/sda3	xfs	177G	69G	109G	39%	/home

From /sys/devices/virtual/dmi/id

BIOS: Cisco Systems, Inc. C480M5.4.0.4g.0.0712190013 07/12/2019  
Vendor: Cisco Systems Inc  
Product: UCSC-C480-M5  
Serial: FCH2223W00A

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

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### Platform Notes (Continued)

Memory:

48x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2934

(End of data from sysinfo program)

### Compiler Version Notes

```
=====  
C          | 600.perlbench_s(base) 602.gcc_s(base) 605.mcf_s(base)  
          | 625.x264_s(base) 657.xz_s(base)  
=====
```

```
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,  
Version 19.0.4.227 Build 20190416  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.  
=====
```

```
=====  
C++       | 620.omnetpp_s(base) 623.xalancbmk_s(base) 631.deepsjeng_s(base)  
         | 641.leela_s(base)  
=====
```

```
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,  
Version 19.0.4.227 Build 20190416  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.  
=====
```

```
=====  
Fortran   | 648.exchange2_s(base)  
=====
```

```
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)  
64, Version 19.0.4.227 Build 20190416  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.  
=====
```

### Base Compiler Invocation

C benchmarks:

icc -m64 -std=c11

C++ benchmarks:

icpc -m64

Fortran benchmarks:

ifort -m64



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## Base Portability Flags

```
600.perlbench_s: -DSPEC_LP64 -DSPEC_LINUX_X64
602.gcc_s: -DSPEC_LP64
605.mcf_s: -DSPEC_LP64
620.omnetpp_s: -DSPEC_LP64
623.xalancbmk_s: -DSPEC_LP64 -DSPEC_LINUX
625.x264_s: -DSPEC_LP64
631.deepsjeng_s: -DSPEC_LP64
641.leela_s: -DSPEC_LP64
648.exchange2_s: -DSPEC_LP64
657.xz_s: -DSPEC_LP64
```

## Base Optimization Flags

### C benchmarks:

```
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP
-L/usr/local/je5.0.1-64/lib -ljemalloc
```

### C++ benchmarks:

```
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmallocc
```

### Fortran benchmarks:

```
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-mem-layout-trans=4
-nostandard-realloc-lhs
```

The flags files that were used to format this result can be browsed at

<http://www.spec.org/cpu2017/flags/Intel-ic19.0u1-official-linux64.2019-07-09.html>  
<http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revJ.html>

You can also download the XML flags sources by saving the following links:

<http://www.spec.org/cpu2017/flags/Intel-ic19.0u1-official-linux64.2019-07-09.xml>  
<http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revJ.xml>

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