



SPEC CPU®2017 Integer Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS C240 M5 (Intel Xeon Platinum 8176, 2.10 GHz)

SPECrate®2017_int_base = 261

SPECrate®2017_int_peak = 277

CPU2017 License: 9019

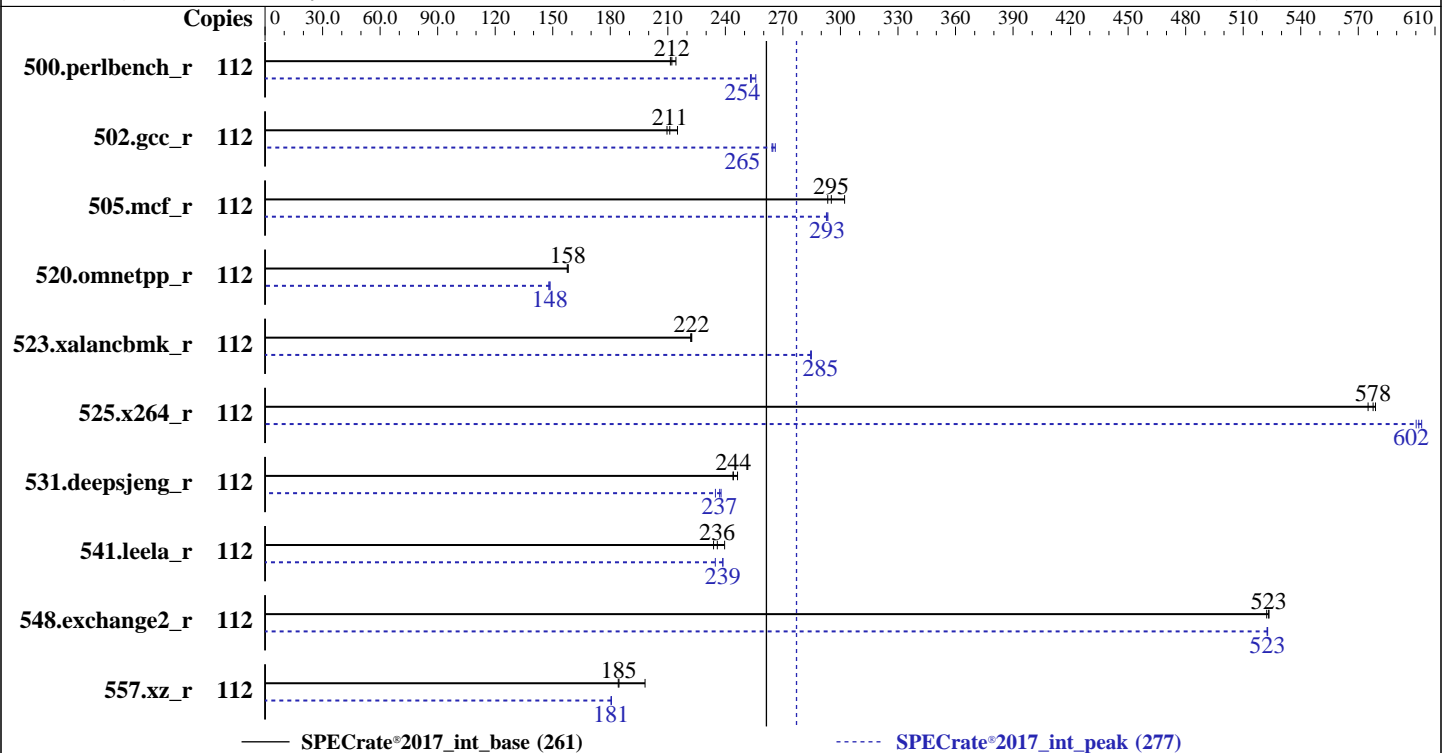
Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Jan-2019

Hardware Availability: Aug-2017

Software Availability: Nov-2018



Hardware

CPU Name: Intel Xeon Platinum 8176
 Max MHz: 3800
 Nominal: 2100
 Enabled: 56 cores, 2 chips, 2 threads/core
 Orderable: 1,2 Chips
 Cache L1: 32 KB I + 32 KB D on chip per core
 L2: 1 MB I+D on chip per core
 L3: 38.5 MB I+D on chip per chip
 Other: None
 Memory: 768 GB (24 x 32 GB 2Rx4 PC4-2666V-R)
 Storage: 1 x 480G SAS SSD
 Other: None

Software

OS: SUSE Linux Enterprise Server 12 SP2 (x86_64) 4.4.120-92.70-default
 Compiler: C/C++: Version 19.0.1.144 of Intel C/C++ Compiler for Linux;
 Fortran: Version 19.0.1.144 of Intel Fortran Compiler for Linux
 Parallel: No
 Firmware: Version 4.0.1 released Oct-2018
 File System: xfs
 System State: Run level 5 (multi-user)
 Base Pointers: 64-bit
 Peak Pointers: 32/64-bit
 Other: jemalloc memory allocator V5.0.1
 Power Management: --



SPEC CPU®2017 Integer Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS C240 M5 (Intel Xeon Platinum 8176, 2.10 GHz)

SPECrate®2017_int_base = 261

SPECrate®2017_int_peak = 277

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Jan-2019
Hardware Availability: Aug-2017
Software Availability: Nov-2018

Results Table

Benchmark	Base							Peak						
	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
500.perlbench_r	112	844	211	841	212	832	214	112	697	256	703	254	705	253
502.gcc_r	112	757	210	752	211	737	215	112	600	264	599	265	596	266
505.mcf_r	112	599	302	613	295	617	293	112	618	293	617	293	618	293
520.omnetpp_r	112	930	158	933	158	930	158	112	989	149	990	148	993	148
523.xalancbmk_r	112	532	222	533	222	532	222	112	415	285	415	285	416	284
525.x264_r	112	341	575	339	578	339	579	112	327	600	326	602	325	603
531.deepsjeng_r	112	521	246	526	244	526	244	112	547	235	542	237	540	238
541.leela_r	112	787	236	774	240	793	234	112	777	239	777	239	790	235
548.exchange2_r	112	562	522	561	523	561	523	112	561	523	561	523	562	522
557.xz_r	112	611	198	655	185	657	184	112	670	181	670	180	670	181

SPECrate®2017_int_base = **261**

SPECrate®2017_int_peak = **277**

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

General Notes

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/cpu2017/lib/ia32:/home/cpu2017/lib/intel64"

Binaries compiled on a system with 1x Intel Core i7-4790 CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.4

Transparent Huge Pages enabled by default

Prior to runcpu invocation

Filesystem page cache synced and cleared with:

```
sync; echo 3> /proc/sys/vm/drop_caches
```

runcpu command invoked through numactl i.e.:

```
numactl --interleave=all runcpu <etc>
```

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2)

(Continued on next page)



SPEC CPU®2017 Integer Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS C240 M5 (Intel Xeon Platinum 8176, 2.10 GHz)

SPECrate®2017_int_base = 261

SPECrate®2017_int_peak = 277

CPU2017 License: 9019

Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Jan-2019

Hardware Availability: Aug-2017

Software Availability: Nov-2018

General Notes (Continued)

is mitigated in the system as tested and documented.

jemalloc: configured and built at default for 32bit (i686) and 64bit (x86_64) targets;
jemalloc: built with the RedHat Enterprise 7.4, and the system compiler gcc 4.8.5;
jemalloc: sources available from jemalloc.net or <https://github.com/jemalloc/jemalloc/releases>

Platform Notes

BIOS Settings:

Intel HyperThreading Technology set to Enabled

CPU performance set to Enterprise

Power Performance Tuning set to OS Controls

SNC set to Enabled

IMC Interleaving set to 1-way Interleave

Patrol Scrub set to Disabled

 Sysinfo program /home/cpu2017/bin/sysinfo

 Rev: r5974 of 2018-05-19 9bcde8f2999c33d61f64985e45859ea9

 running on linux-q5q7 Fri Jan 18 12:22:15 2019

SUT (System Under Test) info as seen by some common utilities.

For more information on this section, see

<https://www.spec.org/cpu2017/Docs/config.html#sysinfo>

From /proc/cpuinfo

 model name : Intel(R) Xeon(R) Platinum 8176 CPU @ 2.10GHz

 2 "physical id"s (chips)

 112 "processors"

 cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)

 cpu cores : 28

 siblings : 56

 physical 0: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 14 16 17 18 19 20 21 22 24 25 26 27

 28 29 30

 physical 1: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 14 16 17 18 19 20 21 22 24 25 26 27

 28 29 30

From lscpu:

Architecture: x86_64

CPU op-mode(s): 32-bit, 64-bit

Byte Order: Little Endian

CPU(s): 112

On-line CPU(s) list: 0-111

Thread(s) per core: 2

(Continued on next page)



SPEC CPU®2017 Integer Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS C240 M5 (Intel Xeon Platinum 8176, 2.10 GHz)

SPECrate®2017_int_base = 261

SPECrate®2017_int_peak = 277

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Jan-2019
Hardware Availability: Aug-2017
Software Availability: Nov-2018

Platform Notes (Continued)

```

Core(s) per socket:      28
Socket(s):              2
NUMA node(s):          4
Vendor ID:              GenuineIntel
CPU family:             6
Model:                  85
Model name:             Intel(R) Xeon(R) Platinum 8176 CPU @ 2.10GHz
Stepping:               4
CPU MHz:                3219.256
CPU max MHz:            3800.0000
CPU min MHz:            1000.0000
BogoMIPS:               4190.17
Virtualization:         VT-x
L1d cache:              32K
L1i cache:              32K
L2 cache:               1024K
L3 cache:               39424K
NUMA node0 CPU(s):     0-3,7-9,14-17,21-23,56-59,63-65,70-73,77-79
NUMA node1 CPU(s):     4-6,10-13,18-20,24-27,60-62,66-69,74-76,80-83
NUMA node2 CPU(s):     28-31,35-37,42-45,49-51,84-87,91-93,98-101,105-107
NUMA node3 CPU(s):     32-34,38-41,46-48,52-55,88-90,94-97,102-104,108-111
Flags:                  fpu vme de pse msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc
aperfmpperf eagerfpu pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg
fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes
xsave avx f16c rdrand lahf_lm abm 3dnowprefetch ida arat epb invpcid_single pln pts
dtherm hwp hwp_act_window hwp_epp hwp_pkg_req intel_pt rsb_ctxsw spec_ctrl stibp
retpoline kaiser tpr_shadow vmmi flexpriority ept vpid fsgsbase tsc_adjust bmi1 hle
avx2 smep bmi2 erms invpcid rtm cqm mpx avx512f avx512dq rdseed adx smap clflushopt
clwb avx512cd avx512bw avx512vl xsaveopt xsavec xgetbv1 cqm_llc cqm_occup_llc

```

```
/proc/cpuinfo cache data
cache size : 39424 KB
```

```

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a
physical chip.
available: 4 nodes (0-3)
node 0 cpus: 0 1 2 3 7 8 9 14 15 16 17 21 22 23 56 57 58 59 63 64 65 70 71 72 73 77 78
79
node 0 size: 192038 MB
node 0 free: 188578 MB
node 1 cpus: 4 5 6 10 11 12 13 18 19 20 24 25 26 27 60 61 62 66 67 68 69 74 75 76 80 81
82 83
node 1 size: 193528 MB
node 1 free: 190349 MB
node 2 cpus: 28 29 30 31 35 36 37 42 43 44 45 49 50 51 84 85 86 87 91 92 93 98 99 100

```

(Continued on next page)



SPEC CPU®2017 Integer Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS C240 M5 (Intel Xeon Platinum 8176, 2.10 GHz)

SPECrate®2017_int_base = 261

SPECrate®2017_int_peak = 277

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Jan-2019
Hardware Availability: Aug-2017
Software Availability: Nov-2018

Platform Notes (Continued)

```

101 105 106 107
node 2 size: 193528 MB
node 2 free: 190534 MB
node 3 cpus: 32 33 34 38 39 40 41 46 47 48 52 53 54 55 88 89 90 94 95 96 97 102 103 104
108 109 110 111
node 3 size: 193391 MB
node 3 free: 190414 MB
node distances:
node  0  1  2  3
  0:  10  11  21  21
  1:  11  10  21  21
  2:  21  21  10  11
  3:  21  21  11  10

From /proc/meminfo
MemTotal:          791026788 kB
HugePages_Total:    0
Hugepagesize:      2048 kB

/usr/bin/lsb_release -d
    SUSE Linux Enterprise Server 12 SP2

From /etc/*release* /etc/*version*
SuSE-release:
    SUSE Linux Enterprise Server 12 (x86_64)
    VERSION = 12
    PATCHLEVEL = 2
    # This file is deprecated and will be removed in a future service pack or release.
    # Please check /etc/os-release for details about this release.
os-release:
    NAME="SLES"
    VERSION="12-SP2"
    VERSION_ID="12.2"
    PRETTY_NAME="SUSE Linux Enterprise Server 12 SP2"
    ID="sles"
    ANSI_COLOR="0;32"
    CPE_NAME="cpe:/o:suse:sles:12:sp2"

uname -a:
    Linux linux-q5q7 4.4.120-92.70-default #1 SMP Wed Mar 14 15:59:43 UTC 2018 (52a83de)
    x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2017-5754 (Meltdown):           Mitigation: PTI
CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: IBRS+IBPB

```

(Continued on next page)



SPEC CPU®2017 Integer Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS C240 M5 (Intel Xeon Platinum 8176, 2.10 GHz)

SPECrate®2017_int_base = 261

SPECrate®2017_int_peak = 277

CPU2017 License: 9019

Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Jan-2019

Hardware Availability: Aug-2017

Software Availability: Nov-2018

Platform Notes (Continued)

run-level 5 Jan 17 23:10

SPEC is set to: /home/cpu2017

Filesystem	Type	Size	Used	Avail	Use%	Mounted on
/dev/sdc3	xfs	404G	30G	374G	8%	/home

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

BIOS Cisco Systems, Inc. C240M5.4.0.1.139.1003182220 10/03/2018

Memory:

24x 0xCE00 M393A4K40BB2-CTD 32 GB 2 rank 2666

(End of data from sysinfo program)

Compiler Version Notes

```

=====
C          | 500.perlbench_r(base, peak) 502.gcc_r(base, peak) 505.mcf_r(base,
          | peak) 525.x264_r(base, peak) 557.xz_r(base, peak)
=====

```

icc (ICC) 19.0.1.144 20181018

Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

```

=====
C++       | 520.omnetpp_r(base, peak) 523.xalancbmk_r(base, peak)
          | 531.deepsjeng_r(base, peak) 541.leela_r(base, peak)
=====

```

icpc (ICC) 19.0.1.144 20181018

Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

```

=====
Fortran   | 548.exchange2_r(base, peak)
=====

```

ifort (IFORT) 19.0.1.144 20181018

Copyright (C) 1985-2018 Intel Corporation. All rights reserved.



SPEC CPU®2017 Integer Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS C240 M5 (Intel Xeon Platinum 8176, 2.10 GHz)

SPECrate®2017_int_base = 261

SPECrate®2017_int_peak = 277

CPU2017 License: 9019

Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Jan-2019

Hardware Availability: Aug-2017

Software Availability: Nov-2018

Base Compiler Invocation

C benchmarks:

```
icc -m64 -std=c11
```

C++ benchmarks:

```
icpc -m64
```

Fortran benchmarks:

```
ifort -m64
```

Base Portability Flags

```
500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
```

```
502.gcc_r: -DSPEC_LP64
```

```
505.mcf_r: -DSPEC_LP64
```

```
520.omnetpp_r: -DSPEC_LP64
```

```
523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX
```

```
525.x264_r: -DSPEC_LP64
```

```
531.deepsjeng_r: -DSPEC_LP64
```

```
541.leela_r: -DSPEC_LP64
```

```
548.exchange2_r: -DSPEC_LP64
```

```
557.xz_r: -DSPEC_LP64
```

Base Optimization Flags

C benchmarks:

```
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
```

```
-qopt-mem-layout-trans=3 -L/home/cpu2017/je5.0.1-64/ -ljemalloc
```

C++ benchmarks:

```
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
```

```
-qopt-mem-layout-trans=3 -L/home/cpu2017/je5.0.1-64/ -ljemalloc
```

Fortran benchmarks:

```
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
```

```
-qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte
```

```
-L/home/cpu2017/je5.0.1-64/ -ljemalloc
```



SPEC CPU®2017 Integer Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS C240 M5 (Intel Xeon Platinum 8176, 2.10 GHz)

SPECrate®2017_int_base = 261

SPECrate®2017_int_peak = 277

CPU2017 License: 9019

Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Jan-2019

Hardware Availability: Aug-2017

Software Availability: Nov-2018

Peak Compiler Invocation

C benchmarks (except as noted below):

```
icc -m64 -std=c11
```

```
502.gcc_r: icc -m32 -std=c11 -L/opt/intel/lib/ia32
```

C++ benchmarks (except as noted below):

```
icpc -m64
```

```
523.xalancbmk_r: icpc -m32 -L/opt/intel/lib/ia32
```

Fortran benchmarks:

```
ifort -m64
```

Peak Portability Flags

```
500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
```

```
502.gcc_r: -D_FILE_OFFSET_BITS=64
```

```
505.mcf_r: -DSPEC_LP64
```

```
520.omnetpp_r: -DSPEC_LP64
```

```
523.xalancbmk_r: -D_FILE_OFFSET_BITS=64 -DSPEC_LINUX
```

```
525.x264_r: -DSPEC_LP64
```

```
531.deepsjeng_r: -DSPEC_LP64
```

```
541.leela_r: -DSPEC_LP64
```

```
548.exchange2_r: -DSPEC_LP64
```

```
557.xz_r: -DSPEC_LP64
```

Peak Optimization Flags

C benchmarks:

```
500.perlbench_r: -w1, -z, muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo  
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3  
-fno-strict-overflow -L/home/cpu2017/je5.0.1-64/  
-ljemalloc
```

```
502.gcc_r: -w1, -z, muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo  
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3  
-L/home/cpu2017/je5.0.1-32/ -ljemalloc
```

```
505.mcf_r: -w1, -z, muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div  
-qopt-mem-layout-trans=3 -L/home/cpu2017/je5.0.1-64/  
-ljemalloc
```

(Continued on next page)



SPEC CPU®2017 Integer Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS C240 M5 (Intel Xeon Platinum 8176, 2.10 GHz)

SPECrate®2017_int_base = 261

SPECrate®2017_int_peak = 277

CPU2017 License: 9019

Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Jan-2019

Hardware Availability: Aug-2017

Software Availability: Nov-2018

Peak Optimization Flags (Continued)

```
525.x264_r: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -fno-alias
-L/home/cpu2017/je5.0.1-64/ -ljemalloc
```

557.xz_r: Same as 505.mcf_r

C++ benchmarks:

```
520.omnetpp_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3
-L/home/cpu2017/je5.0.1-64/ -ljemalloc
```

```
523.xalancbmk_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3
-L/home/cpu2017/je5.0.1-32/ -ljemalloc
```

531.deepsjeng_r: Same as 520.omnetpp_r

541.leela_r: Same as 520.omnetpp_r

Fortran benchmarks:

```
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte
-L/home/cpu2017/je5.0.1-64/ -ljemalloc
```

The flags files that were used to format this result can be browsed at

<http://www.spec.org/cpu2017/flags/Intel-ic19.0-official-linux64.html>

<http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revH.html>

You can also download the XML flags sources by saving the following links:

<http://www.spec.org/cpu2017/flags/Intel-ic19.0-official-linux64.xml>

<http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revH.xml>

SPEC CPU and SPECrate are registered trademarks of the Standard Performance Evaluation Corporation. All other brand and product names appearing in this result are trademarks or registered trademarks of their respective holders.

For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.0.5 on 2019-01-18 15:22:14-0500.

Report generated on 2020-09-04 15:27:40 by CPU2017 PDF formatter v6255.

Originally published on 2019-02-19.