



SPEC® CPU2017 Floating Point Rate Result

Copyright 2017-2019 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS C220 M5 (Intel Xeon Gold 5120
2.20 GHz)

SPECrate2017_fp_base = 149

SPECrate2017_fp_peak = Not Run

CPU2017 License: 9019

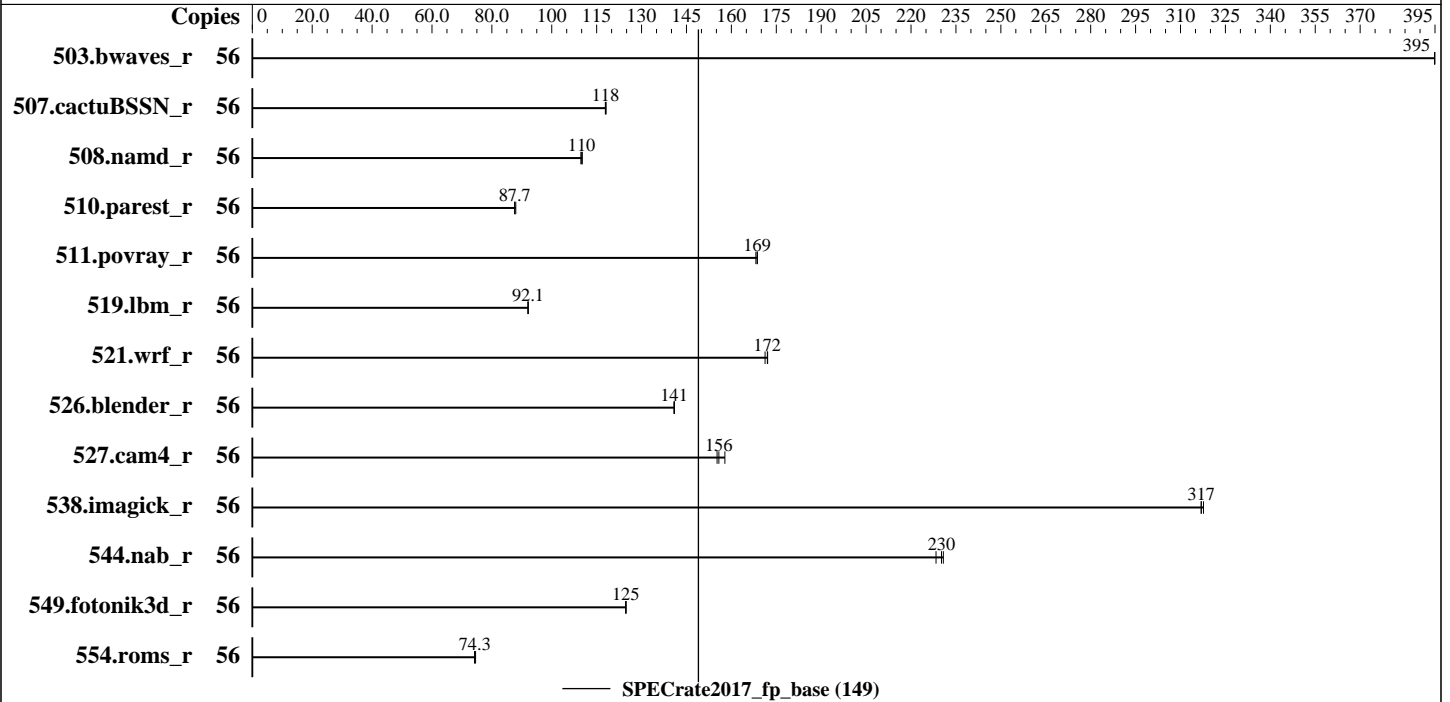
Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Jan-2019

Hardware Availability: Aug-2017

Software Availability: Nov-2018



Hardware

CPU Name: Intel Xeon Gold 5120
 Max MHz.: 3200
 Nominal: 2200
 Enabled: 28 cores, 2 chips, 2 threads/core
 Orderable: 1,2 Chips
 Cache L1: 32 KB I + 32 KB D on chip per core
 L2: 1 MB I+D on chip per core
 L3: 19.25 MB I+D on chip per chip
 Other: None
 Memory: 768 GB (24 x 32 GB 2Rx4 PC4-2666V-R,
 running at 2400)
 Storage: 1 x 240 GB M.2 SATA SSD
 Other: None

Software

OS: SUSE Linux Enterprise Server 12 SP2 (x86_64)
 4.4.120-92.70-default
 Compiler: C/C++: Version 19.0.1.144 of Intel C/C++
 Compiler for Linux;
 Fortran: Version 19.0.1.144 of Intel Fortran
 Compiler for Linux
 Parallel: No
 Firmware: Version 4.0.1 released Oct-2018
 File System: xfs
 System State: Run level 3 (multi-user)
 Base Pointers: 64-bit
 Peak Pointers: Not Applicable
 Other: None



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Results Table

Benchmark	Base							Peak						
	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
503.bwaves_r	56	<u>1422</u>	<u>395</u>	1422	395	1422	395							
507.cactuBSSN_r	56	<u>601</u>	<u>118</u>	600	118	601	118							
508.namd_r	56	483	110	485	110	<u>484</u>	<u>110</u>							
510.parest_r	56	1665	88.0	1672	87.6	<u>1671</u>	<u>87.7</u>							
511.povray_r	56	778	168	775	169	<u>776</u>	<u>169</u>							
519.lbm_r	56	<u>641</u>	<u>92.1</u>	641	92.1	641	92.1							
521.wrf_r	56	<u>729</u>	<u>172</u>	732	171	729	172							
526.blender_r	56	605	141	<u>605</u>	<u>141</u>	606	141							
527.cam4_r	56	621	158	<u>629</u>	<u>156</u>	631	155							
538.imagick_r	56	438	318	439	317	<u>439</u>	<u>317</u>							
544.nab_r	56	408	231	413	228	<u>409</u>	<u>230</u>							
549.fotonik3d_r	56	<u>1749</u>	<u>125</u>	1750	125	1748	125							
554.roms_r	56	1193	74.6	1199	74.2	<u>1197</u>	<u>74.3</u>							

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Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

General Notes

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/cpu2017/lib/ia32:/home/cpu2017/lib/intel64"

Binaries compiled on a system with 1x Intel Core i7-4790 CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.4
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3> /proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:
numactl --interleave=all runcpu <etc>

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

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General Notes (Continued)

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

Platform Notes

BIOS Settings:

Intel HyperThreading Technology set to Enabled

CPU performance set to Enterprise

Power Performance Tuning set to OS Controls

SNC set to Enabled

IMC Interleaving set to 1-way Interleave

Patrol Scrub set to Disabled

Sysinfo program /home/cpu2017/bin/sysinfo

Rev: r5797 of 2017-06-14 96c45e4568ad54c135fd618bcc091c0f

running on linux-dssz Thu Jan 24 14:57:26 2019

SUT (System Under Test) info as seen by some common utilities.

For more information on this section, see

<https://www.spec.org/cpu2017/Docs/config.html#sysinfo>

From /proc/cpuinfo

model name : Intel(R) Xeon(R) Gold 5120 CPU @ 2.20GHz

2 "physical id"s (chips)

56 "processors"

cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)

cpu cores : 14

siblings : 28

physical 0: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 14

physical 1: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 14

From lscpu:

Architecture: x86_64

CPU op-mode(s): 32-bit, 64-bit

Byte Order: Little Endian

CPU(s): 56

On-line CPU(s) list: 0-55

Thread(s) per core: 2

Core(s) per socket: 14

Socket(s): 2

NUMA node(s): 2

Vendor ID: GenuineIntel

CPU family: 6

Model: 85

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Platform Notes (Continued)

```

Model name: Intel(R) Xeon(R) Gold 5120 CPU @ 2.20GHz
Stepping: 4
CPU MHz: 2417.413
CPU max MHz: 3200.0000
CPU min MHz: 1000.0000
BogoMIPS: 4389.68
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 19712K
NUMA node0 CPU(s): 0-13,28-41
NUMA node1 CPU(s): 14-27,42-55
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc
aperfmpperf eagerfpu pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 sse3 sdbg
fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes
xsave avx f16c rdrand lahf_lm abm 3dnowprefetch ida arat epb invpcid_single pln pts
dtherm hwp hwp_act_window hwp_epp hwp_pkg_req intel_pt rsb_ctxsw spec_ctrl stibp
retpoline kaiser tpr_shadow vnmi flexpriority ept vpid fsgsbase tsc_adjust bml hle
avx2 smep bmi2 erms invpcid rtm cqm mpx avx512f avx512dq rdseed adx smap clflushopt
clwb avx512cd avx512bw avx512vl xsaveopt xsavec xgetbv1 cqm_llc cqm_occup_llc

```

```

/proc/cpuinfo cache data
cache size : 19712 KB

```

```

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a
physical chip.
available: 2 nodes (0-1)
node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 28 29 30 31 32 33 34 35 36 37 38 39 40 41
node 0 size: 385627 MB
node 0 free: 385060 MB
node 1 cpus: 14 15 16 17 18 19 20 21 22 23 24 25 26 27 42 43 44 45 46 47 48 49 50 51 52
53 54 55
node 1 size: 387054 MB
node 1 free: 386591 MB
node distances:
node 0 1
0: 10 21
1: 21 10

```

```

From /proc/meminfo
MemTotal: 791226472 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

```

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Platform Notes (Continued)

```

From /etc/*release* /etc/*version*
SuSE-release:
  SUSE Linux Enterprise Server 12 (x86_64)
  VERSION = 12
  PATCHLEVEL = 2
  # This file is deprecated and will be removed in a future service pack or release.
  # Please check /etc/os-release for details about this release.
os-release:
  NAME="SLES"
  VERSION="12-SP2"
  VERSION_ID="12.2"
  PRETTY_NAME="SUSE Linux Enterprise Server 12 SP2"
  ID="sles"
  ANSI_COLOR="0;32"
  CPE_NAME="cpe:/o:suse:sles:12:sp2"

uname -a:
  Linux linux-dssz 4.4.120-92.70-default #1 SMP Wed Mar 14 15:59:43 UTC 2018 (52a83de)
  x86_64 x86_64 x86_64 GNU/Linux

run-level 3 Jan 24 14:46

SPEC is set to: /home/cpu2017
Filesystem      Type  Size  Used Avail Use% Mounted on
/dev/sda3       xfs   212G  141G   72G   67% /home

Additional information from dmidecode follows.  WARNING: Use caution when you interpret
this section. The 'dmidecode' program reads system data which is "intended to allow
hardware to be accurately determined", but the intent may not be met, as there are
frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
  BIOS Cisco Systems, Inc. C220M5.4.0.1.139.1003182107 10/03/2018
  Memory:
    24x 0xCE00 M393A4K40BB2-CTD 32 GB 2 rank 2666, configured at 2400

(End of data from sysinfo program)

```

Compiler Version Notes

```

=====
CC 519.lbm_r(base) 538.imagick_r(base) 544.nab_r(base)
-----
icc (ICC) 19.0.1.144 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
-----
=====

```

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Compiler Version Notes (Continued)

CXXC 508.namd_r(base) 510.parest_r(base)

icpc (ICC) 19.0.1.144 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

CC 511.povray_r(base) 526.blender_r(base)

icpc (ICC) 19.0.1.144 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
icc (ICC) 19.0.1.144 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

FC 507.cactuBSSN_r(base)

icpc (ICC) 19.0.1.144 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
icc (ICC) 19.0.1.144 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
ifort (IFORT) 19.0.1.144 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

FC 503.bwaves_r(base) 549.fotonik3d_r(base) 554.roms_r(base)

ifort (IFORT) 19.0.1.144 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

CC 521.wrf_r(base) 527.cam4_r(base)

ifort (IFORT) 19.0.1.144 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
icc (ICC) 19.0.1.144 20181018
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Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

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Base Compiler Invocation (Continued)

C++ benchmarks:

```
icpc -m64
```

Fortran benchmarks:

```
ifort -m64
```

Benchmarks using both Fortran and C:

```
ifort -m64 icc -m64 -std=c11
```

Benchmarks using both C and C++:

```
icpc -m64 icc -m64 -std=c11
```

Benchmarks using Fortran, C, and C++:

```
icpc -m64 icc -m64 -std=c11 ifort -m64
```

Base Portability Flags

```
503.bwaves_r: -DSPEC_LP64
507.cactuBSSN_r: -DSPEC_LP64
508.namd_r: -DSPEC_LP64
510.parest_r: -DSPEC_LP64
511.povray_r: -DSPEC_LP64
519.lbm_r: -DSPEC_LP64
521.wrf_r: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
526.blender_r: -DSPEC_LP64 -DSPEC_LINUX -funsigned-char
527.cam4_r: -DSPEC_LP64 -DSPEC_CASE_FLAG
538.imagick_r: -DSPEC_LP64
544.nab_r: -DSPEC_LP64
549.fotonik3d_r: -DSPEC_LP64
554.roms_r: -DSPEC_LP64
```

Base Optimization Flags

C benchmarks:

```
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3
```

C++ benchmarks:

```
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3
```

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Base Optimization Flags (Continued)

Fortran benchmarks:

```
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3 -nostandard-realloc-lhs
-align array32byte
```

Benchmarks using both Fortran and C:

```
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3 -nostandard-realloc-lhs
-align array32byte
```

Benchmarks using both C and C++:

```
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3
```

Benchmarks using Fortran, C, and C++:

```
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3 -nostandard-realloc-lhs
-align array32byte
```

The flags files that were used to format this result can be browsed at

<http://www.spec.org/cpu2017/flags/Intel-ic19.0-official-linux64.html>

<http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revH.html>

You can also download the XML flags sources by saving the following links:

<http://www.spec.org/cpu2017/flags/Intel-ic19.0-official-linux64.xml>

<http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revH.xml>

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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