



# SPEC® CPU2017 Integer Speed Result

Copyright 2017-2018 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS C480 M5 (Intel Xeon Gold 6146  
3.20 GHz)

SPECspeed2017\_int\_base = 9.74

SPECspeed2017\_int\_peak = Not Run

CPU2017 License: 9019

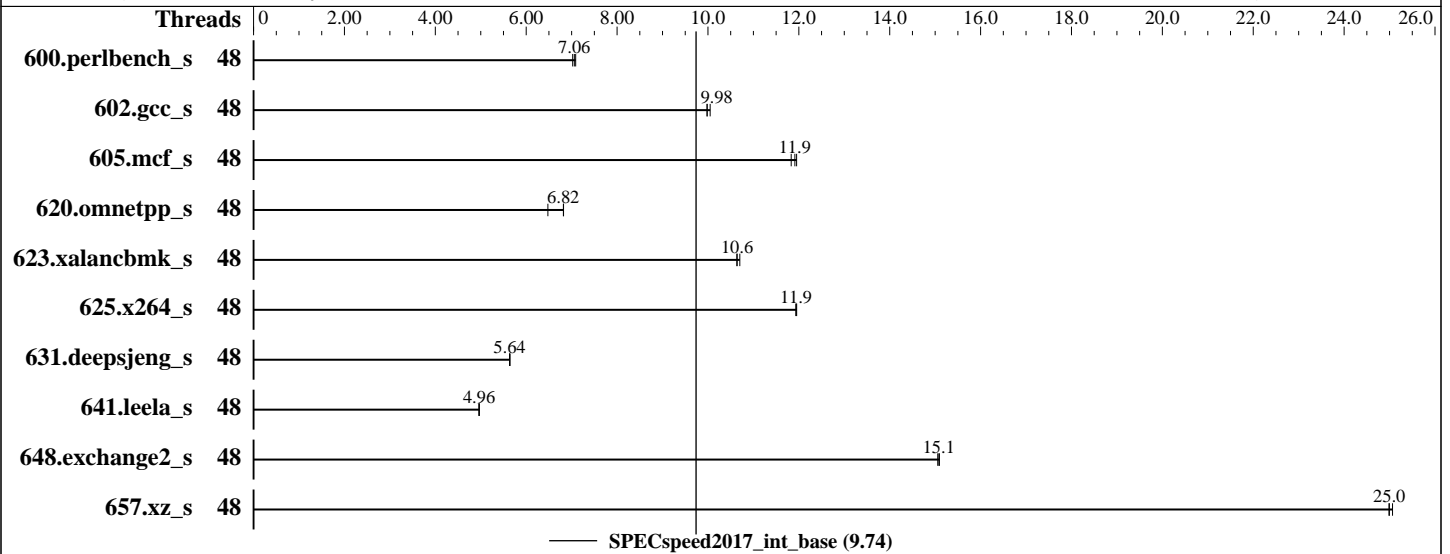
Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Nov-2018

Hardware Availability: Aug-2017

Software Availability: Mar-2018



### Hardware

CPU Name: Intel Xeon Gold 6146  
 Max MHz.: 4200  
 Nominal: 3200  
 Enabled: 48 cores, 4 chips  
 Orderable: 2,4 Chips  
 Cache L1: 32 KB I + 32 KB D on chip per core  
 L2: 1 MB I+D on chip per core  
 L3: 24.75 MB I+D on chip per chip  
 Other: None  
 Memory: 1536 GB (48 x 32 GB 2Rx4 PC4-2666V-R)  
 Storage: 1 x 1 TB HDD, 7.2K RPM  
 Other: None

### Software

OS: SUSE Linux Enterprise Server 12 SP2 (x86\_64)  
 4.4.120-92.70-default  
 Compiler: C/C++: Version 18.0.2.199 of Intel C/C++  
 Compiler for Linux;  
 Fortran: Version 18.0.2.199 of Intel Fortran  
 Compiler for Linux  
 Parallel: Yes  
 Firmware: Version 3.1.3e released Jun-2018  
 File System: xfs  
 System State: Run level 3 (multi-user)  
 Base Pointers: 64-bit  
 Peak Pointers: Not Applicable  
 Other: jemalloc memory allocator V5.0.1



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## Results Table

Benchmark	Base							Peak						
	Threads	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Threads	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
600.perlbench_s	48	253	7.02	250	7.09	<u>251</u>	<u>7.06</u>							
602.gcc_s	48	396	10.0	399	9.98	<u>399</u>	<u>9.98</u>							
605.mcf_s	48	395	12.0	399	11.8	<u>396</u>	<u>11.9</u>							
620.omnetpp_s	48	<u>239</u>	<u>6.82</u>	252	6.48	239	6.82							
623.xalancbmk_s	48	<u>133</u>	<u>10.6</u>	132	10.7	133	10.6							
625.x264_s	48	148	11.9	<u>148</u>	<u>11.9</u>	148	12.0							
631.deepsjeng_s	48	254	5.64	254	5.63	<u>254</u>	<u>5.64</u>							
641.leela_s	48	344	4.97	<u>344</u>	<u>4.96</u>	344	4.96							
648.exchange2_s	48	195	15.1	<u>195</u>	<u>15.1</u>	195	15.1							
657.xz_s	48	247	25.0	247	25.1	<u>247</u>	<u>25.0</u>							

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Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

## Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

## General Notes

Environment variables set by runcpu before the start of the run:

KMP\_AFFINITY = "granularity=fine,scatter"

LD\_LIBRARY\_PATH = "/home/cpu2017/lib/ia32:/home/cpu2017/lib/intel64"

OMP\_STACKSIZE = "192M"

Binaries compiled on a system with 1x Intel Core i7-6700K CPU + 32GB RAM  
memory using Redhat Enterprise Linux 7.5

Transparent Huge Pages enabled by default

Prior to runcpu invocation

Filesystem page cache synced and cleared with:

```
sync; echo 3> /proc/sys/vm/drop_caches
```

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

jemalloc, a general purpose malloc implementation

built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5

sources available from jemalloc.net or <https://github.com/jemalloc/jemalloc/releases>



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## Platform Notes

BIOS Settings:

Intel HyperThreading Technology set to Disabled

CPU performance set to Enterprise

Power Performance Tuning set to OS Controls

SNC set to Disabled

Patrol Scrub set to Disabled

Sysinfo program /home/cpu2017/bin/sysinfo

Rev: r5797 of 2017-06-14 96c45e4568ad54c135fd618bcc091c0f

running on linux-9r4j Fri Nov 30 09:31:25 2018

SUT (System Under Test) info as seen by some common utilities.

For more information on this section, see

<https://www.spec.org/cpu2017/Docs/config.html#sysinfo>

From /proc/cpuinfo

model name : Intel(R) Xeon(R) Gold 6146 CPU @ 3.20GHz

4 "physical id"s (chips)

48 "processors"

cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)

cpu cores : 12

siblings : 12

physical 0: cores 0 1 2 3 4 9 10 16 18 19 25 26

physical 1: cores 0 1 2 3 4 9 10 16 18 19 25 26

physical 2: cores 0 1 2 3 4 9 10 16 18 19 25 26

physical 3: cores 0 1 2 3 4 9 10 16 18 19 25 26

From lscpu:

Architecture: x86\_64

CPU op-mode(s): 32-bit, 64-bit

Byte Order: Little Endian

CPU(s): 48

On-line CPU(s) list: 0-47

Thread(s) per core: 1

Core(s) per socket: 12

Socket(s): 4

NUMA node(s): 4

Vendor ID: GenuineIntel

CPU family: 6

Model: 85

Model name: Intel(R) Xeon(R) Gold 6146 CPU @ 3.20GHz

Stepping: 4

CPU MHz: 1458.695

CPU max MHz: 4200.0000

CPU min MHz: 1200.0000

BogoMIPS: 6393.11

Virtualization: VT-x

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### Platform Notes (Continued)

L1d cache: 32K  
L1i cache: 32K  
L2 cache: 1024K  
L3 cache: 25344K  
NUMA node0 CPU(s): 0-11  
NUMA node1 CPU(s): 12-23  
NUMA node2 CPU(s): 24-35  
NUMA node3 CPU(s): 36-47

Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov  
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp  
lm constant\_tsc art arch\_perfmon pebs bts rep\_good nopl xtopology nonstop\_tsc  
aperfmpperf eagerfpu pni pclmulqdq dtes64 monitor ds\_cpl vmx smx est tm2 ssse3 sdbg  
fma cx16 xtpr pdcm pcid dca sse4\_1 sse4\_2 x2apic movbe popcnt tsc\_deadline\_timer aes  
xsave avx f16c rdrand lahf\_lm abm 3dnowprefetch ida arat epb invpcid\_single pln pts  
dtherm hwp hwp\_act\_window hwp\_epp hwp\_pkg\_req intel\_pt rsb\_ctxsw spec\_ctrl stibp  
retpoline kaiser tpr\_shadow vnmi flexpriority ept vpid fsgsbase tsc\_adjust bmi1 hle  
avx2 smep bmi2 erms invpcid rtm cqm mpx avx512f avx512dq rdseed adx smap clflushopt  
clwb avx512cd avx512bw avx512vl xsaveopt xsavec xgetbv1 cqm\_llc cqm\_occup\_llc

```
/proc/cpuinfo cache data
cache size : 25344 KB
```

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.

```
available: 4 nodes (0-3)
node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11
node 0 size: 385622 MB
node 0 free: 385168 MB
node 1 cpus: 12 13 14 15 16 17 18 19 20 21 22 23
node 1 size: 387057 MB
node 1 free: 386776 MB
node 2 cpus: 24 25 26 27 28 29 30 31 32 33 34 35
node 2 size: 387057 MB
node 2 free: 386854 MB
node 3 cpus: 36 37 38 39 40 41 42 43 44 45 46 47
node 3 size: 387054 MB
node 3 free: 386843 MB
node distances:
node  0  1  2  3
 0:  10  21  21  21
 1:  21  10  21  21
 2:  21  21  10  21
 3:  21  21  21  10
```

```
From /proc/meminfo
MemTotal: 1583914576 kB
HugePages_Total: 0
```

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### Platform Notes (Continued)

Hugepagesize: 2048 kB

From /etc/\*release\* /etc/\*version\*

SuSE-release:

SUSE Linux Enterprise Server 12 (x86\_64)

VERSION = 12

PATCHLEVEL = 2

# This file is deprecated and will be removed in a future service pack or release.

# Please check /etc/os-release for details about this release.

os-release:

NAME="SLES"

VERSION="12-SP2"

VERSION\_ID="12.2"

PRETTY\_NAME="SUSE Linux Enterprise Server 12 SP2"

ID="sles"

ANSI\_COLOR="0;32"

CPE\_NAME="cpe:/o:suse:sles:12:sp2"

uname -a:

Linux linux-9r4j 4.4.120-92.70-default #1 SMP Wed Mar 14 15:59:43 UTC 2018 (52a83de)  
x86\_64 x86\_64 x86\_64 GNU/Linux

run-level 3 Oct 21 23:48

SPEC is set to: /home/cpu2017

Filesystem	Type	Size	Used	Avail	Use%	Mounted on
/dev/sdal	xf	930G	244G	687G	27%	/

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

BIOS Cisco Systems, Inc. C480M5.3.1.3e.0.0613181101 06/13/2018

Memory:

48x 0xCE00 M393A4K40BB2-CTD 32 GB 2 rank 2666

(End of data from sysinfo program)

### Compiler Version Notes

=====  
CC 600.perlbench\_s(base) 602.gcc\_s(base) 605.mcf\_s(base) 625.x264\_s(base)  
657.xz\_s(base)  
-----

icc (ICC) 18.0.2 20180210

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=====  
CXXC 620.omnetpp\_s(base) 623.xalancbmk\_s(base) 631.deepsjeng\_s(base)  
641.leela\_s(base)  
=====

-----  
icpc (ICC) 18.0.2 20180210  
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.  
-----

=====  
FC 648.exchange2\_s(base)  
=====

-----  
ifort (IFORT) 18.0.2 20180210  
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.  
-----

## Base Compiler Invocation

C benchmarks:

icc -m64 -std=c11

C++ benchmarks:

icpc -m64

Fortran benchmarks:

ifort -m64

## Base Portability Flags

600.perlbench\_s: -DSPEC\_LP64 -DSPEC\_LINUX\_X64  
602.gcc\_s: -DSPEC\_LP64  
605.mcf\_s: -DSPEC\_LP64  
620.omnetpp\_s: -DSPEC\_LP64  
623.xalancbmk\_s: -DSPEC\_LP64 -DSPEC\_LINUX  
625.x264\_s: -DSPEC\_LP64  
631.deepsjeng\_s: -DSPEC\_LP64  
641.leela\_s: -DSPEC\_LP64  
648.exchange2\_s: -DSPEC\_LP64  
657.xz\_s: -DSPEC\_LP64



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## Base Optimization Flags

C benchmarks:

```
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div  
-qopt-mem-layout-trans=3 -qopenmp -DSPEC_OPENMP  
-L/usr/local/je5.0.1-64/lib -ljemalloc
```

C++ benchmarks:

```
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div  
-qopt-mem-layout-trans=3 -L/usr/local/je5.0.1-64/lib -ljemalloc
```

Fortran benchmarks:

```
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div  
-qopt-mem-layout-trans=3 -nostandard-realloc-lhs  
-L/usr/local/je5.0.1-64/lib -ljemalloc
```

The flags files that were used to format this result can be browsed at

<http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.2017-12-21.html>

<http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revH.html>

You can also download the XML flags sources by saving the following links:

<http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.2017-12-21.xml>

<http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revH.xml>

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For questions about this result, please contact the tester. For other inquiries, please contact [info@spec.org](mailto:info@spec.org).

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