



# SPEC® CPU2017 Integer Rate Result

Copyright 2017-2018 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS B480 M5 (Intel Xeon Gold 6126  
2.60 GHz)

SPECrate2017\_int\_base = 274

SPECrate2017\_int\_peak = 291

CPU2017 License: 9019

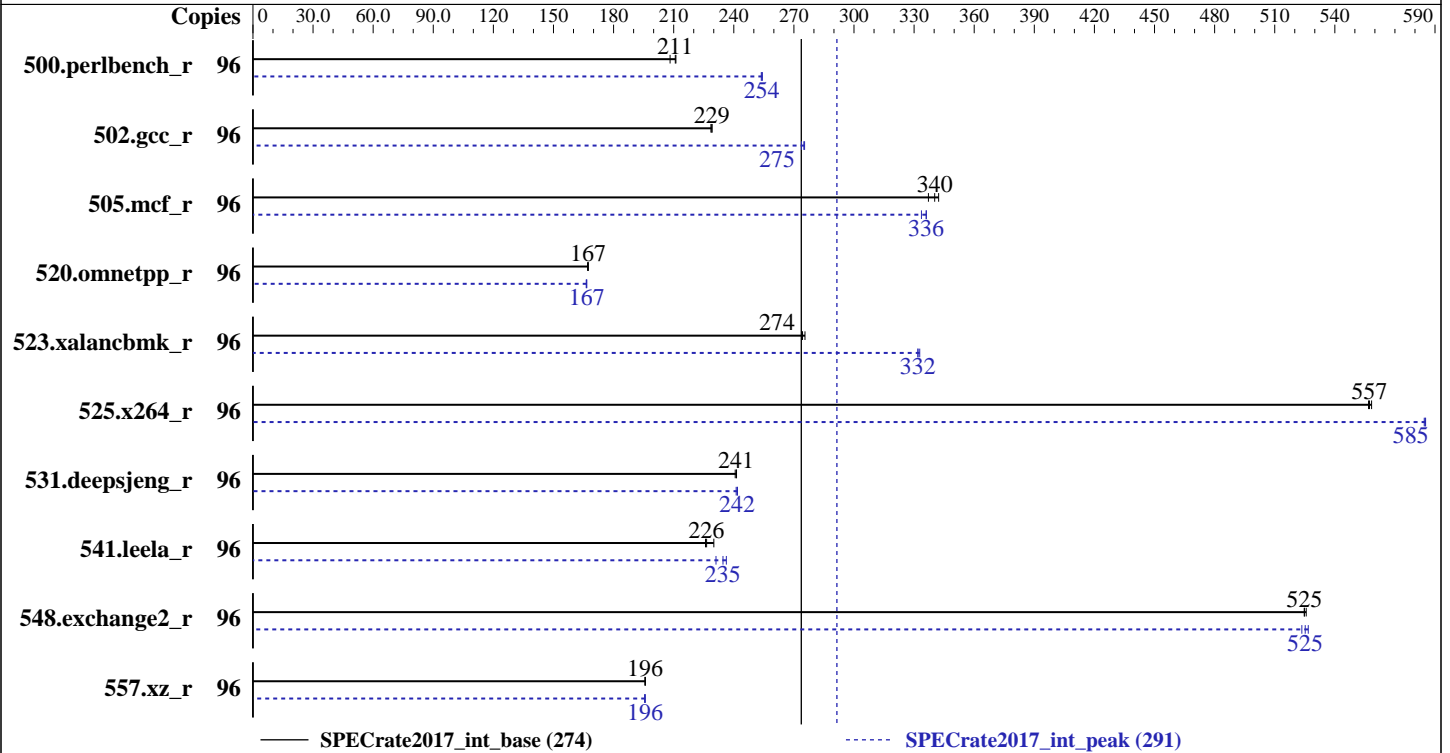
Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Nov-2018

Hardware Availability: Aug-2017

Software Availability: Mar-2018



### Hardware

CPU Name: Intel Xeon Gold 6126  
 Max MHz.: 3700  
 Nominal: 2600  
 Enabled: 48 cores, 4 chips, 2 threads/core  
 Orderable: 2,4 Chips  
 Cache L1: 32 KB I + 32 KB D on chip per core  
 L2: 1 MB I+D on chip per core  
 L3: 19.25 MB I+D on chip per chip  
 Other: None  
 Memory: 1536 GB (48 x 32 GB 2Rx4 PC4-2666V-R)  
 Storage: 1 x 400 GB SSD SAS  
 Other: None

### Software

OS: SUSE Linux Enterprise Server 12 SP2 (x86\_64)  
 4.4.120-92.70-default  
 Compiler: C/C++: Version 18.0.2.199 of Intel C/C++  
 Compiler for Linux;  
 Fortran: Version 18.0.2.199 of Intel Fortran  
 Compiler for Linux  
 Parallel: No  
 Firmware: Version 3.2.3c released Mar-2018  
 File System: xfs  
 System State: Run level 3 (multi-user)  
 Base Pointers: 64-bit  
 Peak Pointers: 32/64-bit  
 Other: jemalloc: jemalloc memory allocator library  
 V5.0.1;



# SPEC CPU2017 Integer Rate Result

Copyright 2017-2018 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS B480 M5 (Intel Xeon Gold 6126  
2.60 GHz)

SPECrate2017\_int\_base = 274

SPECrate2017\_int\_peak = 291

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems

**Test Date:** Nov-2018  
**Hardware Availability:** Aug-2017  
**Software Availability:** Mar-2018

## Results Table

Benchmark	Base							Peak						
	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
500.perlbench_r	96	<b><u>725</u></b>	<b><u>211</u></b>	724	211	734	208	96	602	254	601	254	<b><u>602</u></b>	<b><u>254</u></b>
502.gcc_r	96	593	229	<b><u>594</u></b>	<b><u>229</u></b>	595	229	96	<b><u>494</u></b>	<b><u>275</u></b>	494	275	496	274
505.mcf_r	96	<b><u>456</u></b>	<b><u>340</u></b>	453	342	460	337	96	<b><u>462</u></b>	<b><u>336</u></b>	465	334	462	336
520.omnetpp_r	96	754	167	<b><u>753</u></b>	<b><u>167</u></b>	753	167	96	757	166	756	167	<b><u>756</u></b>	<b><u>167</u></b>
523.xalancbmk_r	96	<b><u>370</u></b>	<b><u>274</u></b>	368	276	370	274	96	305	333	<b><u>305</u></b>	<b><u>332</u></b>	305	332
525.x264_r	96	<b><u>302</u></b>	<b><u>557</u></b>	301	558	302	557	96	288	585	<b><u>287</u></b>	<b><u>585</u></b>	287	585
531.deepsjeng_r	96	457	241	456	241	<b><u>456</u></b>	<b><u>241</u></b>	96	455	242	<b><u>455</u></b>	<b><u>242</u></b>	456	241
541.leela_r	96	691	230	<b><u>702</u></b>	<b><u>226</u></b>	704	226	96	673	236	<b><u>678</u></b>	<b><u>235</u></b>	688	231
548.exchange2_r	96	478	526	<b><u>479</u></b>	<b><u>525</u></b>	479	525	96	477	527	480	524	<b><u>479</u></b>	<b><u>525</u></b>
557.xz_r	96	<b><u>530</u></b>	<b><u>196</u></b>	529	196	530	196	96	530	196	530	195	<b><u>530</u></b>	<b><u>196</u></b>

SPECrate2017\_int\_base = 274

SPECrate2017\_int\_peak = 291

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

## Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

## Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

## General Notes

Environment variables set by runcpu before the start of the run:

LD\_LIBRARY\_PATH = "/home/cpu2017/lib/ia32:/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-32:/home/cpu2017/je5.0.1-64"

Binaries compiled on a system with 1x Intel Core i7-4790 CPU + 32GB RAM  
memory using Redhat Enterprise Linux 7.4  
Transparent Huge Pages enabled by default

Prior to runcpu invocation

Filesystem page cache synced and cleared with:

```
sync; echo 3> /proc/sys/vm/drop_caches
```

runcpu command invoked through numactl i.e.:

```
numactl --interleave=all runcpu <etc>
```

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2)

(Continued on next page)



# SPEC CPU2017 Integer Rate Result

Copyright 2017-2018 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS B480 M5 (Intel Xeon Gold 6126  
2.60 GHz)

SPECrate2017\_int\_base = 274

SPECrate2017\_int\_peak = 291

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems

**Test Date:** Nov-2018  
**Hardware Availability:** Aug-2017  
**Software Availability:** Mar-2018

## General Notes (Continued)

is mitigated in the system as tested and documented.

jemalloc: configured and built at default for  
32bit (i686) and 64bit (x86\_64) targets;  
jemalloc: built with the RedHat Enterprise 7.4,  
and the system compiler gcc 4.8.5;  
jemalloc: sources available from jemalloc.net or  
<https://github.com/jemalloc/jemalloc/releases>

## Platform Notes

BIOS Settings:  
Intel HyperThreading Technology set to Enabled  
CPU performance set to Enterprise  
Power Performance Tuning set to OS Controls  
SNC set to Enabled  
IMC Interleaving set to 1-way Interleave  
Patrol Scrub set to Disabled  
Sysinfo program /home/cpu2017/bin/sysinfo  
Rev: r5797 of 2017-06-14 96c45e4568ad54c135fd618bcc091c0f  
running on linux-xy4f Sat Jan 2 18:31:53 2010

SUT (System Under Test) info as seen by some common utilities.  
For more information on this section, see  
<https://www.spec.org/cpu2017/Docs/config.html#sysinfo>

From /proc/cpuinfo  
model name : Intel(R) Xeon(R) Gold 6126 CPU @ 2.60GHz  
4 "physical id"s (chips)  
96 "processors"  
cores, siblings (Caution: counting these is hw and system dependent. The following  
excerpts from /proc/cpuinfo might not be reliable. Use with caution.)  
cpu cores : 12  
siblings : 24  
physical 0: cores 0 1 3 5 6 8 9 10 11 12 13 14  
physical 1: cores 0 1 3 4 5 6 8 9 10 11 12 13  
physical 2: cores 0 2 3 4 5 8 9 10 11 12 13 14  
physical 3: cores 0 1 2 3 4 6 9 10 11 12 13 14

From lscpu:  
Architecture: x86\_64  
CPU op-mode(s): 32-bit, 64-bit  
Byte Order: Little Endian  
CPU(s): 96  
On-line CPU(s) list: 0-95  
Thread(s) per core: 2

(Continued on next page)



# SPEC CPU2017 Integer Rate Result

Copyright 2017-2018 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS B480 M5 (Intel Xeon Gold 6126  
2.60 GHz)

SPECrate2017\_int\_base = 274

SPECrate2017\_int\_peak = 291

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems

**Test Date:** Nov-2018  
**Hardware Availability:** Aug-2017  
**Software Availability:** Mar-2018

### Platform Notes (Continued)

```

Core(s) per socket:      12
Socket(s):               4
NUMA node(s):           8
Vendor ID:               GenuineIntel
CPU family:              6
Model:                   85
Model name:              Intel(R) Xeon(R) Gold 6126 CPU @ 2.60GHz
Stepping:                4
CPU MHz:                 2530.062
CPU max MHz:             3700.0000
CPU min MHz:             1000.0000
BogoMIPS:                5199.96
Virtualization:         VT-x
L1d cache:               32K
L1i cache:               32K
L2 cache:                1024K
L3 cache:                19712K
NUMA node0 CPU(s):      0-2,5-7,48-50,53-55
NUMA node1 CPU(s):      3,4,8-11,51,52,56-59
NUMA node2 CPU(s):      12-14,18-20,60-62,66-68
NUMA node3 CPU(s):      15-17,21-23,63-65,69-71
NUMA node4 CPU(s):      24-26,29-31,72-74,77-79
NUMA node5 CPU(s):      27,28,32-35,75,76,80-83
NUMA node6 CPU(s):      36-39,42,43,84-87,90,91
NUMA node7 CPU(s):      40,41,44-47,88,89,92-95
Flags:                   fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc
aperfperf eagerfpu pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg
fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes
xsave avx f16c rdrand lahf_lm abm 3dnowprefetch ida arat epb invpcid_single pln pts
dtherm hwp hwp_act_window hwp_epp hwp_pkg_req intel_pt rsb_ctxsw spec_ctrl stibp
retpoline kaiser tpr_shadow vnmi flexpriority ept vpid fsgsbase tsc_adjust bmil hle
avx2 smep bmi2 erms invpcid rtm cqm mpx avx512f avx512dq rdseed adx smap clflushopt
clwb avx512cd avx512bw avx512vl xsaveopt xsavec xgetbv1 cqm_llc cqm_occup_llc

```

```

/proc/cpuinfo cache data
cache size : 19712 KB

```

```

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a
physical chip.
available: 8 nodes (0-7)
node 0 cpus: 0 1 2 5 6 7 48 49 50 53 54 55
node 0 size: 192095 MB
node 0 free: 189541 MB
node 1 cpus: 3 4 8 9 10 11 51 52 56 57 58 59
node 1 size: 193528 MB

```

(Continued on next page)



# SPEC CPU2017 Integer Rate Result

Copyright 2017-2018 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS B480 M5 (Intel Xeon Gold 6126  
2.60 GHz)

SPECrate2017\_int\_base = 274

SPECrate2017\_int\_peak = 291

**CPU2017 License:** 9019

**Test Sponsor:** Cisco Systems

**Tested by:** Cisco Systems

**Test Date:** Nov-2018

**Hardware Availability:** Aug-2017

**Software Availability:** Mar-2018

### Platform Notes (Continued)

```

node 1 free: 191114 MB
node 2 cpus: 12 13 14 18 19 20 60 61 62 66 67 68
node 2 size: 193528 MB
node 2 free: 191125 MB
node 3 cpus: 15 16 17 21 22 23 63 64 65 69 70 71
node 3 size: 193528 MB
node 3 free: 191132 MB
node 4 cpus: 24 25 26 29 30 31 72 73 74 77 78 79
node 4 size: 193528 MB
node 4 free: 191122 MB
node 5 cpus: 27 28 32 33 34 35 75 76 80 81 82 83
node 5 size: 193528 MB
node 5 free: 191112 MB
node 6 cpus: 36 37 38 39 42 43 84 85 86 87 90 91
node 6 size: 193528 MB
node 6 free: 191130 MB
node 7 cpus: 40 41 44 45 46 47 88 89 92 93 94 95
node 7 size: 193525 MB
node 7 free: 191107 MB
node distances:
node  0  1  2  3  4  5  6  7
 0:  10  11  21  21  21  21  21  21
 1:  11  10  21  21  21  21  21  21
 2:  21  21  10  11  21  21  21  21
 3:  21  21  11  10  21  21  21  21
 4:  21  21  21  21  10  11  21  21
 5:  21  21  21  21  11  10  21  21
 6:  21  21  21  21  21  21  10  11
 7:  21  21  21  21  21  21  11  10

```

From /proc/meminfo

```

MemTotal:      1583915000 kB
HugePages_Total:      0
Hugepagesize:    2048 kB

```

From /etc/\*release\* /etc/\*version\*

```

SuSE-release:
  SUSE Linux Enterprise Server 12 (x86_64)
  VERSION = 12
  PATCHLEVEL = 2
  # This file is deprecated and will be removed in a future service pack or release.
  # Please check /etc/os-release for details about this release.
os-release:
  NAME="SLES"
  VERSION="12-SP2"
  VERSION_ID="12.2"
  PRETTY_NAME="SUSE Linux Enterprise Server 12 SP2"

```

(Continued on next page)



# SPEC CPU2017 Integer Rate Result

Copyright 2017-2018 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS B480 M5 (Intel Xeon Gold 6126  
2.60 GHz)

SPECrate2017\_int\_base = 274

SPECrate2017\_int\_peak = 291

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems

**Test Date:** Nov-2018  
**Hardware Availability:** Aug-2017  
**Software Availability:** Mar-2018

### Platform Notes (Continued)

```
ID="sles"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:12:sp2"
```

```
uname -a:
Linux linux-xy4f 4.4.120-92.70-default #1 SMP Wed Mar 14 15:59:43 UTC 2018 (52a83de)
x86_64 x86_64 x86_64 GNU/Linux
```

```
run-level 3 Jan 2 02:36
```

```
SPEC is set to: /home/cpu2017
Filesystem      Type  Size  Used Avail Use% Mounted on
/dev/sdal        xfs   224G   87G  138G  39% /
```

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

```
BIOS Cisco Systems, Inc. B480M5.3.2.3c.0.0307181316 03/07/2018
Memory:
48x 0xCE00 M393A4K40BB2-CTD 32 GB 2 rank 2666
```

(End of data from sysinfo program)

### Compiler Version Notes

```
=====  
CC 500.perlbench_r(base) 502.gcc_r(base) 505.mcf_r(base, peak)  
525.x264_r(base, peak) 557.xz_r(base, peak)  
-----
```

```
icc (ICC) 18.0.2 20180210  
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.  
-----
```

```
=====  
CC 500.perlbench_r(peak) 502.gcc_r(peak)  
-----
```

```
icc (ICC) 18.0.2 20180210  
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.  
-----
```

```
=====  
CXXC 520.omnetpp_r(base) 523.xalancbmk_r(base) 531.deepsjeng_r(base)  
541.leela_r(base)  
-----
```

```
icpc (ICC) 18.0.2 20180210
```

(Continued on next page)



# SPEC CPU2017 Integer Rate Result

Copyright 2017-2018 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS B480 M5 (Intel Xeon Gold 6126  
2.60 GHz)

SPECrate2017\_int\_base = 274

SPECrate2017\_int\_peak = 291

**CPU2017 License:** 9019

**Test Sponsor:** Cisco Systems

**Tested by:** Cisco Systems

**Test Date:** Nov-2018

**Hardware Availability:** Aug-2017

**Software Availability:** Mar-2018

## Compiler Version Notes (Continued)

Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

=====  
CXXC 520.omnetpp\_r(peak) 523.xalancbmk\_r(peak) 531.deepsjeng\_r(peak)  
541.leela\_r(peak)

icpc (ICC) 18.0.2 20180210

Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

=====  
FC 548.exchange2\_r(base, peak)

ifort (IFORT) 18.0.2 20180210

Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

## Base Compiler Invocation

C benchmarks:

icc -m64 -std=c11

C++ benchmarks:

icpc -m64

Fortran benchmarks:

ifort -m64

## Base Portability Flags

500.perlbench\_r: -DSPEC\_LP64 -DSPEC\_LINUX\_X64

502 gcc\_r: -DSPEC\_LP64

505.mcf\_r: -DSPEC\_LP64

520.omnetpp\_r: -DSPEC\_LP64

523.xalancbmk\_r: -DSPEC\_LP64 -DSPEC\_LINUX

525.x264\_r: -DSPEC\_LP64

531.deepsjeng\_r: -DSPEC\_LP64

541.leela\_r: -DSPEC\_LP64

548.exchange2\_r: -DSPEC\_LP64

557.xz\_r: -DSPEC\_LP64



# SPEC CPU2017 Integer Rate Result

Copyright 2017-2018 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS B480 M5 (Intel Xeon Gold 6126  
2.60 GHz)

SPECrate2017\_int\_base = 274

SPECrate2017\_int\_peak = 291

**CPU2017 License:** 9019

**Test Sponsor:** Cisco Systems

**Tested by:** Cisco Systems

**Test Date:** Nov-2018

**Hardware Availability:** Aug-2017

**Software Availability:** Mar-2018

## Base Optimization Flags

C benchmarks:

```
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div  
-qopt-mem-layout-trans=3 -L/home/cpu2017/je5.0.1-64/ -ljemalloc
```

C++ benchmarks:

```
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div  
-qopt-mem-layout-trans=3 -L/home/cpu2017/je5.0.1-64/ -ljemalloc
```

Fortran benchmarks:

```
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div  
-qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte  
-L/home/cpu2017/je5.0.1-64/ -ljemalloc
```

## Peak Compiler Invocation

C benchmarks (except as noted below):

```
icc -m64 -std=c11
```

```
502.gcc_r: icc -m32 -std=c11 -L/opt/intel/compilers_and_libraries_2018/linux/lib/ia32
```

C++ benchmarks (except as noted below):

```
icpc -m64
```

```
523.xalancbmk_r: icpc -m32 -L/opt/intel/compilers_and_libraries_2018/linux/lib/ia32
```

Fortran benchmarks:

```
ifort -m64
```

## Peak Portability Flags

```
500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64  
502.gcc_r: -D_FILE_OFFSET_BITS=64  
505.mcf_r: -DSPEC_LP64  
520.omnetpp_r: -DSPEC_LP64  
523.xalancbmk_r: -D_FILE_OFFSET_BITS=64 -DSPEC_LINUX  
525.x264_r: -DSPEC_LP64  
531.deepsjeng_r: -DSPEC_LP64  
541.leela_r: -DSPEC_LP64  
548.exchange2_r: -DSPEC_LP64  
557.xz_r: -DSPEC_LP64
```





# SPEC CPU2017 Integer Rate Result

Copyright 2017-2018 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS B480 M5 (Intel Xeon Gold 6126  
2.60 GHz)

SPECrate2017\_int\_base = 274

SPECrate2017\_int\_peak = 291

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems

**Test Date:** Nov-2018  
**Hardware Availability:** Aug-2017  
**Software Availability:** Mar-2018

## Peak Optimization Flags

C benchmarks:

```
500.perlbench_r: -w1,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo  
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3  
-fno-strict-overflow -L/home/cpu2017/je5.0.1-64/  
-ljemalloc
```

```
502.gcc_r: -w1,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo  
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3  
-L/home/cpu2017/je5.0.1-32/ -ljemalloc
```

```
505.mcf_r: -w1,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div  
-qopt-mem-layout-trans=3 -L/home/cpu2017/je5.0.1-64/  
-ljemalloc
```

```
525.x264_r: -w1,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div  
-qopt-mem-layout-trans=3 -fno-alias  
-L/home/cpu2017/je5.0.1-64/ -ljemalloc
```

557.xz\_r: Same as 505.mcf\_r

C++ benchmarks:

```
520.omnetpp_r: -w1,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo  
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3  
-L/home/cpu2017/je5.0.1-64/ -ljemalloc
```

```
523.xalancbmk_r: -w1,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo  
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3  
-L/home/cpu2017/je5.0.1-32/ -ljemalloc
```

531.deepsjeng\_r: Same as 520.omnetpp\_r

541.leela\_r: Same as 520.omnetpp\_r

Fortran benchmarks:

```
-w1,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div  
-qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte  
-L/home/cpu2017/je5.0.1-64/ -ljemalloc
```

The flags files that were used to format this result can be browsed at

<http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.2018-06-13.html>

<http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revH.html>



# SPEC CPU2017 Integer Rate Result

Copyright 2017-2018 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS B480 M5 (Intel Xeon Gold 6126  
2.60 GHz)

SPECrate2017\_int\_base = 274

SPECrate2017\_int\_peak = 291

**CPU2017 License:** 9019

**Test Sponsor:** Cisco Systems

**Tested by:** Cisco Systems

**Test Date:** Nov-2018

**Hardware Availability:** Aug-2017

**Software Availability:** Mar-2018

You can also download the XML flags sources by saving the following links:

<http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.2018-06-13.xml>

<http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revH.xml>

SPEC is a registered trademark of the Standard Performance Evaluation Corporation. All other brand and product names appearing in this result are trademarks or registered trademarks of their respective holders.

For questions about this result, please contact the tester. For other inquiries, please contact [info@spec.org](mailto:info@spec.org).

Tested with SPEC CPU2017 v1.0.2 on 2018-11-27 13:40:45 by CPU2017 PDF formatter v6067.

Report generated on 2018-11-27 13:40:45 by CPU2017 PDF formatter v6067.

Originally published on 2018-11-27.