SPEC® CPU2017 Integer Speed Result

Copyright 2017-2018 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS B480 M5 (Intel Xeon Platinum 8180M, 2.50 GHz)

$SPECspeed2017\_int\_base = 9.35$

$SPECspeed2017\_int\_peak = 9.58$

CPU2017 License: 9019

Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Sep-2018

Hardware Availability: Aug-2017

Software Availability: Aug-2018

Threads		
600.perlbench_s	112	6.38 / 7.58
602.gcc_s	112	9.73 / 9.90
605.mcf_s	112	11.2 / 11.2
620.omnetpp_s	112	7.68 / 7.65
623.xalancbmk_s	112	9.76 / 10.3
625.x264_s	112	12.2 / 12.2
631.deepsjeng_s	112	5.19 / 5.16
641.leela_s	112	4.46 / 4.48
648.exchange2_s	112	13.8 / 13.8
657.xz_s	112	25.2 / 25.1

— SPECspeed2017_int_base (9.35)   ---- SPECspeed2017_int_peak (9.58)

Hardware

CPU Name: Intel Xeon Platinum 8180M
 Max MHz.: 3800
 Nominal: 2500
Enabled: 112 cores, 4 chips
Orderable: 2,4 Chips
Cache L1: 32 KB I + 32 KB D on chip per core
 L2: 1 MB I+D on chip per core
 L3: 38.5 MB I+D on chip per chip
 Other: None
Memory: 1536 GB (48 x 32 GB 2Rx4 PC4-2666V-R)
Storage: 1 x 400 GB SSD SAS
Other: None

Software

OS: SUSE Linux Enterprise Server 12 SP2 (x86_64)
4.4.103-92.56-default
Compiler: C/C++: Version 18.0.0.128 of Intel C/C++
Compiler for Linux;
Fortran: Version 18.0.0.128 of Intel Fortran
Compiler for Linux
Parallel: Yes
Firmware: Version 4.0.1b released Aug-2018
File System: xfs
System State: Run level 3 (multi-user)
Base Pointers: 64-bit
Peak Pointers: 32/64-bit
Other: jemalloc: jemalloc memory allocator library
V5.0.1;

SPEC CPU2017 Integer Speed Result

Copyright 2017-2018 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS B480 M5 (Intel Xeon Platinum 8180M, 2.50 GHz)

SPECspeed2017_int_base =   9.35

SPECspeed2017_int_peak =   9.58

CPU2017 License: 9019
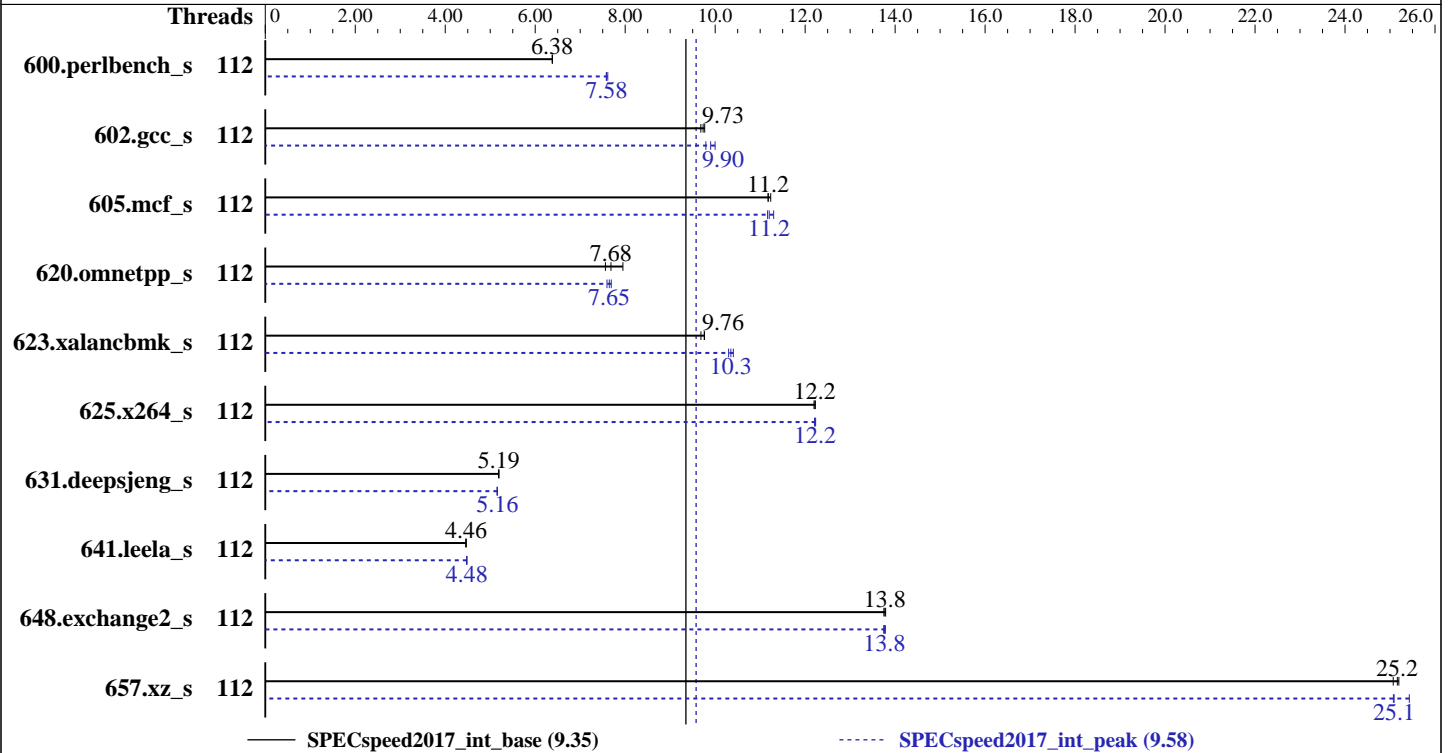**Test Sponsor:** Cisco Systems
Tested by: Cisco Systems

Results Table

Benchmark	Base							Peak						
	Threads	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Threads	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
600.perlbench_s	112	278	6.38	278	6.38	**278**	**6.38**	112	234	7.58	**234**	**7.58**	233	7.61
602.gcc_s	112	408	9.77	411	9.68	**409**	**9.73**	112	**402**	**9.90**	398	10.0	407	9.79
605.mcf_s	112	422	11.2	**422**	**11.2**	420	11.2	112	418	11.3	423	11.2	**421**	**11.2**
620.omnetpp_s	112	**212**	**7.68**	216	7.56	205	7.95	112	212	7.69	215	7.60	**213**	**7.65**
623.xalancbmk_s	112	**145**	**9.76**	146	9.68	145	9.76	112	136	10.4	**137**	**10.3**	138	10.3
625.x264_s	112	144	12.2	**144**	**12.2**	145	12.2	112	**144**	**12.2**	144	12.2	144	12.2
631.deepsjeng_s	112	276	5.19	**276**	**5.19**	276	5.19	112	**278**	**5.16**	278	5.16	278	5.15
641.leela_s	112	382	4.46	383	4.46	**382**	**4.46**	112	381	4.48	**381**	**4.48**	381	4.48
648.exchange2_s	112	214	13.7	213	13.8	**213**	**13.8**	112	**214**	**13.8**	214	13.7	213	13.8
657.xz_s	112	245	25.2	**246**	**25.2**	247	25.1	112	243	25.4	**246**	**25.1**	247	25.1
SPECspeed2017_int_base =		**9.35**												
SPECspeed2017_int_peak =		**9.58**												

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Operating System Notes

```
Stack size set to unlimited using "ulimit -s unlimited"
```

General Notes

```
Environment variables set by runcpu before the start of the run:
KMP_AFFINITY = "granularity=fine,scatter"
LD_LIBRARY_PATH = "/opt/cpu2017/lib/ia32:/opt/cpu2017/lib/intel64:/opt/cpu2017/je5.0.1-32:/opt/cpu2017/je5.0.1-64"
OMP_STACKSIZE = "192M"

 Binaries compiled on a system with 1x Intel Core i7-4790 CPU + 32GB RAM
 memory using Redhat Enterprise Linux 7.4
 Transparent Huge Pages enabled by default
 Prior to runcpu invocation
 Filesystem page cache synced and cleared with:
 sync; echo 3>        /proc/sys/vm/drop_caches
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2)
is mitigated in the system as tested and documented.

 jemalloc: configured and built at default for
 32bit (i686) and 64bit (x86_64) targets;
 jemalloc: built with the RedHat Enterprise 7.4,
 and the system compiler gcc 4.8.5;
 jemalloc: sources available from jemalloc.net or
```

(Continued on next page)

SPEC CPU2017 Integer Speed Result

Copyright 2017-2018 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS B480 M5 (Intel Xeon Platinum 8180M, 2.50 GHz)

SPECspeed2017_int_base = 9.35

SPECspeed2017_int_peak = 9.58

General Notes (Continued)

https://github.com/jemalloc/jemalloc/releases

Platform Notes

```
BIOS Settings:
Intel HyperThreading Technology set to Disabled
CPU performance set to Enterprise
Power Performance Tuning set to OS Controls
SNC set to Disabled
Patrol Scrub set to Disabled
 Sysinfo program /opt/cpu2017/bin/sysinfo
 Rev: r5797 of 2017-06-14 96c45e4568ad54c135fd618bcc091c0f
 running on linux-vb5q Wed Sep 12 02:02:44 2018

 SUT (System Under Test) info as seen by some common utilities.
 For more information on this section, see
    https://www.spec.org/cpu2017/Docs/config.html#sysinfo

 From /proc/cpuinfo
    model name : Intel(R) Xeon(R) Platinum 8180M CPU @ 2.50GHz
       4  "physical id"s (chips)
       112 "processors"
    cores, siblings (Caution: counting these is hw and system dependent. The following
    excerpts from /proc/cpuinfo might not be reliable.  Use with caution.)
      cpu cores : 28
      siblings  : 28
      physical 0: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 14 16 17 18 19 20 21 22 24 25 26 27
      28 29 30
      physical 1: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 14 16 17 18 19 20 21 22 24 25 26 27
      28 29 30
      physical 2: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 14 16 17 18 19 20 21 22 24 25 26 27
      28 29 30
      physical 3: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 14 16 17 18 19 20 21 22 24 25 26 27
      28 29 30

 From lscpu:
      Architecture:          x86_64
      CPU op-mode(s):        32-bit, 64-bit
      Byte Order:            Little Endian
      CPU(s):                112
      On-line CPU(s) list:   0-111
      Thread(s) per core:    1
      Core(s) per socket:    28
      Socket(s):             4
      NUMA node(s):          4
      Vendor ID:             GenuineIntel
```

(Continued on next page)

Cisco Systems

Cisco UCS B480 M5 (Intel Xeon Platinum 8180M, 2.50 GHz)

SPECspeed2017_int_base = 9.35

SPECspeed2017_int_peak = 9.58

CPU2017 License: 9019

Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Sep-2018

Hardware Availability: Aug-2017

Software Availability: Aug-2018

Platform Notes (Continued)

```
        CPU family:            6
        Model:                 85
        Model name:            Intel(R) Xeon(R) Platinum 8180M CPU @ 2.50GHz
        Stepping:              4
        CPU MHz:               3792.885
        CPU max MHz:           3800.0000
        CPU min MHz:           1000.0000
        BogoMIPS:              4999.96
        Virtualization:        VT-x
        L1d cache:             32K
        L1i cache:             32K
        L2 cache:              1024K
        L3 cache:              39424K
        NUMA node0 CPU(s):     0-27
        NUMA node1 CPU(s):     28-55
        NUMA node2 CPU(s):     56-83
        NUMA node3 CPU(s):     84-111
        Flags:                 fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
     pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
     lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc
     aperfmperf eagerfpu pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg
     fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes
     xsave avx f16c rdrand lahf_lm abm 3dnowprefetch ida arat epb invpcid_single pln pts
     dtherm hwp hwp_act_window hwp_epp hwp_pkg_req intel_pt spec_ctrl kaiser tpr_shadow
     vnmi flexpriority ept vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid
     rtm cqm mpx avx512f avx512dq rdseed adx smap clflushopt clwb avx512cd avx512bw
     avx512vl xsaveopt xsavec xgetbv1 cqm_llc cqm_occup_llc

 /proc/cpuinfo cache data
    cache size : 39424 KB

 From numactl --hardware  WARNING: a numactl 'node' might or might not correspond to a
 physical chip.
   available: 4 nodes (0-3)
   node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27
   node 0 size: 385463 MB
   node 0 free: 383007 MB
   node 1 cpus: 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52
   53 54 55
   node 1 size: 387057 MB
   node 1 free: 385130 MB
   node 2 cpus: 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 71 72 73 74 75 76 77 78 79 80
   81 82 83
   node 2 size: 387057 MB
   node 2 free: 384552 MB
   node 3 cpus: 84 85 86 87 88 89 90 91 92 93 94 95 96 97 98 99 100 101 102 103 104 105
   106 107 108 109 110 111
```

(Continued on next page)

Cisco Systems

Cisco UCS B480 M5 (Intel Xeon Platinum 8180M, 2.50 GHz)

SPECspeed2017_int_base = 9.35

SPECspeed2017_int_peak = 9.58

CPU2017 License: 9019

Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Sep-2018

Hardware Availability: Aug-2017

Software Availability: Aug-2018

Platform Notes (Continued)

```
   node 3 size: 387054 MB
   node 3 free: 384520 MB
   node distances:
   node   0   1   2   3
     0:  10  21  21  21
     1:  21  10  21  21
     2:  21  21  10  21
     3:  21  21  21  10

 From /proc/meminfo
    MemTotal:       1583751116 kB
    HugePages_Total:        0
    Hugepagesize:        2048 kB

 From /etc/*release* /etc/*version*
    SuSE-release:
       SUSE Linux Enterprise Server 12 (x86_64)
       VERSION = 12
       PATCHLEVEL = 2
       # This file is deprecated and will be removed in a future service pack or release.
       # Please check /etc/os-release for details about this release.
    os-release:
       NAME="SLES"
       VERSION="12-SP2"
       VERSION_ID="12.2"
       PRETTY_NAME="SUSE Linux Enterprise Server 12 SP2"
       ID="sles"
       ANSI_COLOR="0;32"
       CPE_NAME="cpe:/o:suse:sles:12:sp2"

 uname -a:
    Linux linux-vb5q 4.4.103-92.56-default #1 SMP Wed Dec 27 16:24:31 UTC 2017 (2fd2155)
    x86_64 x86_64 x86_64 GNU/Linux

 run-level 3 Sep 12 00:18

 SPEC is set to: /opt/cpu2017
    Filesystem      Type  Size  Used Avail Use% Mounted on
    /dev/sda1       xfs   280G   53G  227G  19% /

 Additional information from dmidecode follows.  WARNING: Use caution when you interpret
 this section. The 'dmidecode' program reads system data which is "intended to allow
 hardware to be accurately determined", but the intent may not be met, as there are
 frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
    BIOS Cisco Systems, Inc. B480M5.4.0.1b.0.0807180154 08/07/2018
    Memory:
     48x 0xCE00 M393A4K40BB2-CTD 32 GB 2 rank 2666
```

Cisco Systems

Cisco UCS B480 M5 (Intel Xeon Platinum 8180M, 2.50 GHz)

SPECspeed2017_int_base = 9.35

SPECspeed2017_int_peak = 9.58

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Sep-2018
Hardware Availability: Aug-2017
Software Availability: Aug-2018

Platform Notes (Continued)

```
 (End of data from sysinfo program)
```

Compiler Version Notes

```
==============================================================================
  CC   600.perlbench_s(base) 602.gcc_s(base) 605.mcf_s(base) 625.x264_s(base,
       peak) 657.xz_s(base)
------------------------------------------------------------------------------
icc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation.  All rights reserved.
------------------------------------------------------------------------------


==============================================================================
  CC   600.perlbench_s(peak) 602.gcc_s(peak) 605.mcf_s(peak) 657.xz_s(peak)
------------------------------------------------------------------------------
icc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation.  All rights reserved.
------------------------------------------------------------------------------


==============================================================================
  CXXC 620.omnetpp_s(base) 623.xalancbmk_s(base) 631.deepsjeng_s(base)
       641.leela_s(base)
------------------------------------------------------------------------------
icpc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation.  All rights reserved.
------------------------------------------------------------------------------


==============================================================================
 CXXC 620.omnetpp_s(peak) 623.xalancbmk_s(peak) 631.deepsjeng_s(peak)
      641.leela_s(peak)
------------------------------------------------------------------------------
icpc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation.  All rights reserved.
------------------------------------------------------------------------------


==============================================================================
  FC   648.exchange2_s(base, peak)
------------------------------------------------------------------------------
ifort (IFORT) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation.  All rights reserved.
------------------------------------------------------------------------------
```

SPEC CPU2017 Integer Speed Result

Copyright 2017-2018 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS B480 M5 (Intel Xeon Platinum 8180M, 2.50 GHz)

SPECspeed2017_int_base = 9.35

SPECspeed2017_int_peak = 9.58

CPU2017 License: 9019	**Test Date:** Sep-2018
Test Sponsor: Cisco Systems	**Hardware Availability:** Aug-2017
Tested by: Cisco Systems	**Software Availability:** Aug-2018

Base Compiler Invocation

C benchmarks:
`icc -m64 -std=c11`

C++ benchmarks:
`icpc -m64`

Fortran benchmarks:
`ifort -m64`

Base Portability Flags

600.perlbench_s: `-DSPEC_LP64 -DSPEC_LINUX_X64`
602.gcc_s: `-DSPEC_LP64`
605.mcf_s: `-DSPEC_LP64`
620.omnetpp_s: `-DSPEC_LP64`
623.xalancbmk_s: `-DSPEC_LP64 -DSPEC_LINUX`
625.x264_s: `-DSPEC_LP64`
631.deepsjeng_s: `-DSPEC_LP64`
641.leela_s: `-DSPEC_LP64`
648.exchange2_s: `-DSPEC_LP64`
657.xz_s: `-DSPEC_LP64`

Base Optimization Flags

C benchmarks:
```
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -qopenmp -DSPEC_OPENMP
-L/usr/local/je5.0.1-64/lib -ljemalloc
```

C++ benchmarks:
```
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -L/usr/local/je5.0.1-64/lib -ljemalloc
```

Fortran benchmarks:
```
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte
-L/usr/local/je5.0.1-64/lib -ljemalloc
```

Standard Performance Evaluation Corporation (info@spec.org)

https://www.spec.org/

SPEC CPU2017 Integer Speed Result

Copyright 2017-2018 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS B480 M5 (Intel Xeon Platinum 8180M, 2.50 GHz)

SPECspeed2017_int_base = 9.35

SPECspeed2017_int_peak = 9.58

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Sep-2018
Hardware Availability: Aug-2017
Software Availability: Aug-2018

Peak Compiler Invocation

C benchmarks:
```
icc -m64 -std=c11
```

C++ benchmarks (except as noted below):
```
icpc -m64
```

```
623.xalancbmk_s: icpc -m32 -L/opt/intel/compilers_and_libraries_2018/linux/lib/ia32
```

Fortran benchmarks:
```
ifort -m64
```

Peak Portability Flags

```
600.perlbench_s: -DSPEC_LP64 -DSPEC_LINUX_X64
602.gcc_s: -DSPEC_LP64
605.mcf_s: -DSPEC_LP64
620.omnetpp_s: -DSPEC_LP64
623.xalancbmk_s: -D_FILE_OFFSET_BITS=64 -DSPEC_LINUX
625.x264_s: -DSPEC_LP64
631.deepsjeng_s: -DSPEC_LP64
641.leela_s: -DSPEC_LP64
648.exchange2_s: -DSPEC_LP64
657.xz_s: -DSPEC_LP64
```

Peak Optimization Flags

C benchmarks:

```
600.perlbench_s: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -O2
-xCORE-AVX512 -qopt-mem-layout-trans=3 -ipo -O3
-no-prec-div -DSPEC_SUPPRESS_OPENMP -qopenmp
-DSPEC_OPENMP -fno-strict-overflow
-L/usr/local/je5.0.1-64/lib -ljemalloc
```

```
602.gcc_s: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -O2
-xCORE-AVX512 -qopt-mem-layout-trans=3 -ipo -O3
-no-prec-div -DSPEC_SUPPRESS_OPENMP -qopenmp
-DSPEC_OPENMP -L/usr/local/je5.0.1-64/lib -ljemalloc
```

```
605.mcf_s: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3
-DSPEC_SUPPRESS_OPENMP -qopenmp -DSPEC_OPENMP
```

(Continued on next page)

Standard Performance Evaluation Corporation (info@spec.org)

https://www.spec.org/

Cisco Systems

Cisco UCS B480 M5 (Intel Xeon Platinum 8180M, 2.50 GHz)

SPECspeed2017_int_base = 9.35

SPECspeed2017_int_peak = 9.58

CPU2017 License:	9019	**Test Date:**	Sep-2018
Test Sponsor:	Cisco Systems	**Hardware Availability:**	Aug-2017
Tested by:	Cisco Systems	**Software Availability:**	Aug-2018

Peak Optimization Flags (Continued)

605.mcf_s (continued):
`-L/usr/local/je5.0.1-64/lib -ljemalloc`

625.x264_s: `-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div`
`-qopt-mem-layout-trans=3 -qopenmp -DSPEC_OPENMP`
`-L/usr/local/je5.0.1-64/lib -ljemalloc`

657.xz_s: `Same as 602.gcc_s`

C++ benchmarks:

620.omnetpp_s: `-Wl,-z,muldefs -prof-gen`(pass 1) `-prof-use`(pass 2) `-ipo`
`-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3`
`-DSPEC_SUPPRESS_OPENMP -qopenmp -DSPEC_OPENMP`
`-L/usr/local/je5.0.1-64/lib -ljemalloc`

623.xalancbmk_s: `-Wl,-z,muldefs -prof-gen`(pass 1) `-prof-use`(pass 2) `-ipo`
`-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3`
`-DSPEC_SUPPRESS_OPENMP -qopenmp -DSPEC_OPENMP`
`-L/usr/local/je5.0.1-32/lib -ljemalloc`

631.deepsjeng_s: `Same as 620.omnetpp_s`

641.leela_s: `Same as 620.omnetpp_s`

Fortran benchmarks:
`-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div`
`-qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte`
`-L/usr/local/je5.0.1-64/lib -ljemalloc`

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.2017-12-21.html
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revH.html

---

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.2017-12-21.xml
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revH.xml

---

For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU2017 v1.0.2 on 2018-09-12 02:02:43-0400.
Report generated on 2018-10-31 19:14:43 by CPU2017 PDF formatter v6067.
Originally published on 2018-10-02.