SPEC CPU®2017 Integer Rate Result

Cisco Systems

Cisco UCS C480 M5 (Intel Xeon Platinum 8158, 3.00GHz)

$SPECrate^{®}2017\_int\_base = 308$

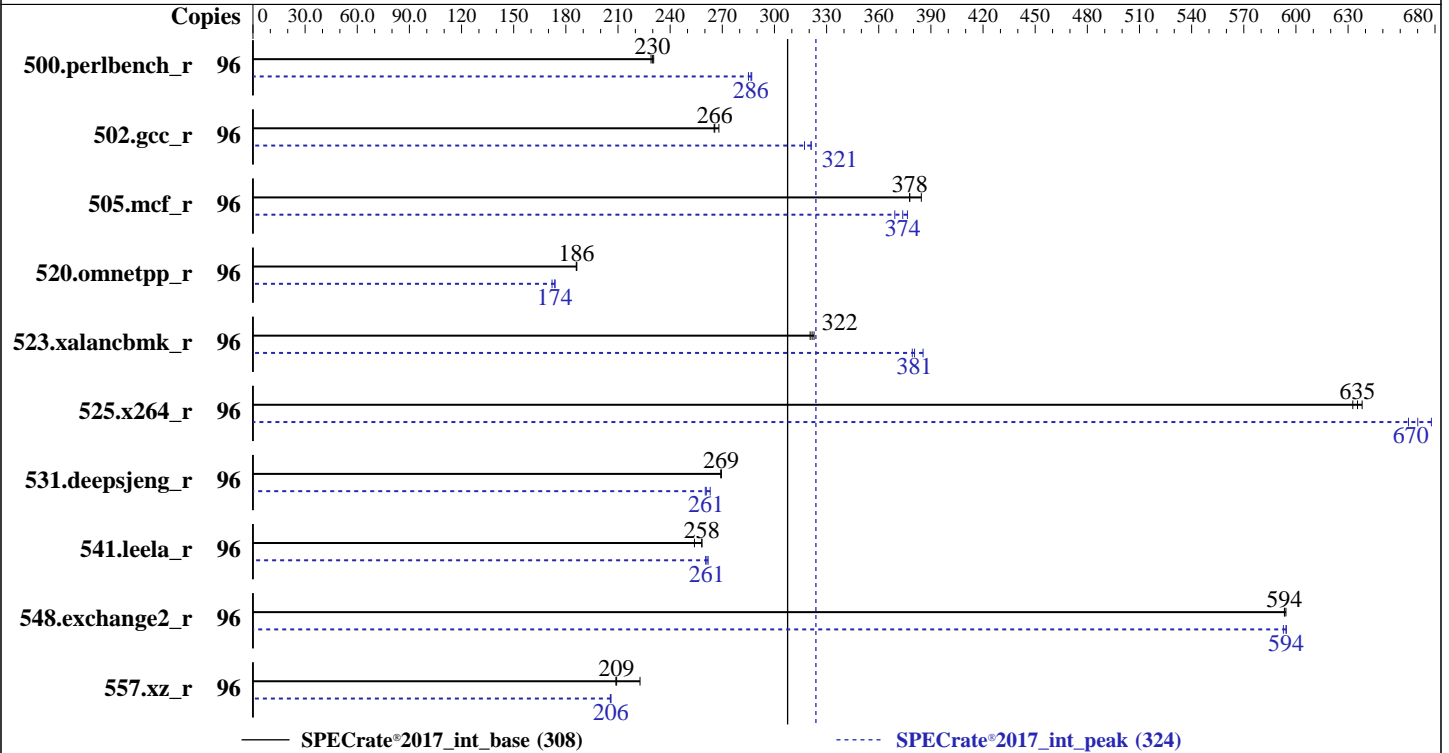$SPECrate^{®}2017\_int\_peak = 324$

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Oct-2017
Hardware Availability: Aug-2017
Software Availability: Sep-2017

Benchmark	Copies	base	peak
500.perlbench_r	96	230	286
502.gcc_r	96	266	321
505.mcf_r	96	378	374
520.omnetpp_r	96	186	174
523.xalancbmk_r	96	322	381
525.x264_r	96	635	670
531.deepsjeng_r	96	269	261
541.leela_r	96	258	261
548.exchange2_r	96	594	594
557.xz_r	96	209	206

SPECrate®2017_int_base (308) · SPECrate®2017_int_peak (324)

Hardware

CPU Name: Intel Xeon Platinum 8158
Max MHz: 3700
Nominal: 3000
Enabled: 48 cores, 4 chips, 2 threads/core
Orderable: 2,4 Chips
Cache L1: 32 KB I + 32 KB D on chip per core
 L2: 1 MB I+D on chip per core
 L3: 24.75 MB I+D on chip per chip
 Other: None
Memory: 768 GB (48 x 16 GB 2Rx4 PC4-2666V-R)
Storage: 2 x 1 TB SAS HDD, 7.2K RPM
Other: None

Software

OS: SUSE Linux Enterprise Server 12 SP2 (x86_64) 4.4.21-69-default
Compiler: C/C++: Version 18.0.0.128 of Intel C/C++ Compiler for Linux; Fortran: Version 18.0.0.128 of Intel Fortran Compiler for Linux
Parallel: No
Firmware: Version 3.1.0 released Jun-2017
File System: btrfs
System State: Run level 3 (multi-user)
Base Pointers: 64-bit
Peak Pointers: 32/64-bit
Other: jemalloc: jemalloc memory allocator library V5.0.1; jemalloc: configured and built at default for 32bit (i686) and 64bit (x86_64) targets
Power Management: --

SPEC CPU®2017 Integer Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS C480 M5 (Intel Xeon Platinum 8158, 3.00GHz)

SPECrate®2017_int_base = 308

SPECrate®2017_int_peak = 324

Results Table

Benchmark	Base							Peak						
	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
500.perlbench_r	96	667	229	**665**	**230**	663	231	96	533	287	536	285	**533**	**286**
502.gcc_r	96	507	268	**512**	**266**	512	265	96	423	321	428	317	**423**	**321**
505.mcf_r	96	403	384	**411**	**378**	411	378	96	**415**	**374**	420	369	412	377
520.omnetpp_r	96	676	186	677	186	**677**	**186**	96	725	174	732	172	**725**	**174**
523.xalancbmk_r	96	**315**	**322**	314	323	316	321	96	263	386	**266**	**381**	267	379
525.x264_r	96	266	633	**265**	**635**	263	638	96	253	665	248	678	**251**	**670**
531.deepsjeng_r	96	408	269	409	269	**408**	**269**	96	423	260	**422**	**261**	418	263
541.leela_r	96	626	254	**616**	**258**	616	258	96	610	260	**609**	**261**	607	262
548.exchange2_r	96	423	594	**424**	**594**	424	593	96	424	593	**423**	**594**	423	594
557.xz_r	96	466	223	497	209	**496**	**209**	96	504	206	**504**	**206**	504	206
SPECrate®2017_int_base =		**308**												
SPECrate®2017_int_peak =		**324**												

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes

The taskset mechanism was used to bind copies to processors. The config file option 'submit' was used to generate taskset commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

General Notes

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/opt/cpu2017/lib/ia32:/opt/cpu2017/lib/intel64:/opt/cpu2017/je5.0.1-32:/opt/cpu2017/je5.0.1-64"

Binaries compiled on a system with 1x Intel Core i7-4790 CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.4
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3>   /proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:
numactl --interleave=all runcpu <etc>
jemalloc, a general purpose malloc implementation
built with the RedHat Enterprise 7.4, and the system compiler gcc 4.8.5
sources available from jemalloc.net or https://github.com/jemalloc/jemalloc/releases

SPEC CPU®2017 Integer Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS C480 M5 (Intel Xeon Platinum 8158, 3.00GHz)

SPECrate®2017_int_base = 308

SPECrate®2017_int_peak = 324

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Oct-2017
Hardware Availability: Aug-2017
Software Availability: Sep-2017

Platform Notes

```
BIOS Settings:
Intel HyperThreading Technology set to Enabled
CPU performance set to Enterprise
Power Performance Tuning set to OS
SNC set to Disabled
IMC Interleaving set to 1-way Interleave
Patrol Scrub set to Disabled
 Sysinfo program /opt/cpu2017/bin/sysinfo
 Rev: r5797 of 2017-06-14 96c45e4568ad54c135fd618bcc091c0f
 running on linux-qew3 Sat Oct 28 11:00:12 2017

 SUT (System Under Test) info as seen by some common utilities.
 For more information on this section, see
    https://www.spec.org/cpu2017/Docs/config.html#sysinfo

 From /proc/cpuinfo
    model name : Intel(R) Xeon(R) Platinum 8158 CPU @ 3.00GHz
       4  "physical id"s (chips)
       96 "processors"
    cores, siblings (Caution: counting these is hw and system dependent. The following
    excerpts from /proc/cpuinfo might not be reliable.  Use with caution.)
       cpu cores : 12
       siblings  : 24
       physical 0: cores 0 1 2 3 4 9 10 16 18 19 25 26
       physical 1: cores 0 1 3 9 10 16 18 19 24 25 26 27
       physical 2: cores 0 1 2 3 4 9 10 16 18 19 25 26
       physical 3: cores 0 1 2 3 4 9 10 16 18 19 25 26

 From lscpu:
      Architecture:        x86_64
      CPU op-mode(s):      32-bit, 64-bit
      Byte Order:          Little Endian
      CPU(s):              96
      On-line CPU(s) list: 0-95
      Thread(s) per core:  2
      Core(s) per socket:  12
      Socket(s):           4
      NUMA node(s):        8
      Vendor ID:           GenuineIntel
      CPU family:          6
      Model:               85
      Model name:          Intel(R) Xeon(R) Platinum 8158 CPU @ 3.00GHz
      Stepping:            4
      CPU MHz:             1481.634
      CPU max MHz:         3700.0000
      CPU min MHz:         1200.0000
      BogoMIPS:            6000.24
```

(Continued on next page)

Cisco Systems

Cisco UCS C480 M5 (Intel Xeon Platinum 8158, 3.00GHz)

SPECrate®2017_int_base = 308

SPECrate®2017_int_peak = 324

CPU2017 License: 9019

Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Oct-2017

Hardware Availability: Aug-2017

Software Availability: Sep-2017

Platform Notes (Continued)

```
      Virtualization:        VT-x
      L1d cache:             32K
      L1i cache:             32K
      L2 cache:              1024K
      L3 cache:              25344K
      NUMA node0 CPU(s):     0-2,5,7,10,48-50,53,55,58
      NUMA node1 CPU(s):     3,4,6,8,9,11,51,52,54,56,57,59
      NUMA node2 CPU(s):     12,13,15,17,20,21,60,61,63,65,68,69
      NUMA node3 CPU(s):     14,16,18,19,22,23,62,64,66,67,70,71
      NUMA node4 CPU(s):     24-26,29,31,34,72-74,77,79,82
      NUMA node5 CPU(s):     27,28,30,32,33,35,75,76,78,80,81,83
      NUMA node6 CPU(s):     36-38,41,43,46,84-86,89,91,94
      NUMA node7 CPU(s):     39,40,42,44,45,47,87,88,90,92,93,95
      Flags:                 fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
    pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
    lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc
    aperfmperf eagerfpu pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg
    fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes
    xsave avx f16c rdrand lahf_lm abm 3dnowprefetch ida arat epb pln pts dtherm hwp
    hwp_act_window hwp_epp hwp_pkg_req intel_pt tpr_shadow vnmi flexpriority ept vpid
    fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm cqm mpx avx512f
    avx512dq rdseed adx smap clflushopt clwb avx512cd avx512bw avx512vl xsaveopt xsavec
    xgetbv1 cqm_llc cqm_occup_llc

 /proc/cpuinfo cache data
   cache size : 25344 KB

 From numactl --hardware  WARNING: a numactl 'node' might or might not correspond to a
 physical chip.
   available: 8 nodes (0-7)
   node 0 cpus: 0 1 2 5 7 10 48 49 50 53 55 58
   node 0 size: 95326 MB
   node 0 free: 92691 MB
   node 1 cpus: 3 4 6 8 9 11 51 52 54 56 57 59
   node 1 size: 96760 MB
   node 1 free: 94063 MB
   node 2 cpus: 12 13 15 17 20 21 60 61 63 65 68 69
   node 2 size: 96760 MB
   node 2 free: 93390 MB
   node 3 cpus: 14 16 18 19 22 23 62 64 66 67 70 71
   node 3 size: 96760 MB
   node 3 free: 94559 MB
   node 4 cpus: 24 25 26 29 31 34 72 73 74 77 79 82
   node 4 size: 96760 MB
   node 4 free: 94353 MB
   node 5 cpus: 27 28 30 32 33 35 75 76 78 80 81 83
   node 5 size: 96760 MB
```

(Continued on next page)

Cisco Systems

Cisco UCS C480 M5 (Intel Xeon Platinum 8158, 3.00GHz)

SPECrate®2017_int_base = 308

SPECrate®2017_int_peak = 324

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Oct-2017
Hardware Availability: Aug-2017
Software Availability: Sep-2017

Platform Notes (Continued)

```
   node 5 free: 93898 MB
   node 6 cpus: 36 37 38 41 43 46 84 85 86 89 91 94
   node 6 size: 96760 MB
   node 6 free: 94044 MB
   node 7 cpus: 39 40 42 44 45 47 87 88 90 92 93 95
   node 7 size: 96757 MB
   node 7 free: 93929 MB
   node distances:
   node   0   1   2   3   4   5   6   7
     0:  10  11  21  21  21  21  31  31
     1:  11  10  21  21  21  21  31  31
     2:  21  21  10  11  31  31  21  21
     3:  21  21  11  10  31  31  21  21
     4:  21  21  31  31  10  11  21  21
     5:  21  21  31  31  11  10  21  21
     6:  31  31  21  21  21  21  10  11
     7:  31  31  21  21  21  21  11  10

 From /proc/meminfo
    MemTotal:       791190356 kB
    HugePages_Total:        0
    Hugepagesize:        2048 kB

 From /etc/*release* /etc/*version*
    SuSE-release:
       SUSE Linux Enterprise Server 12 (x86_64)
       VERSION = 12
       PATCHLEVEL = 2
       # This file is deprecated and will be removed in a future service pack or release.
       # Please check /etc/os-release for details about this release.
    os-release:
       NAME="SLES"
       VERSION="12-SP2"
       VERSION_ID="12.2"
       PRETTY_NAME="SUSE Linux Enterprise Server 12 SP2"
       ID="sles"
       ANSI_COLOR="0;32"
       CPE_NAME="cpe:/o:suse:sles:12:sp2"

 uname -a:
    Linux linux-qew3 4.4.21-69-default #1 SMP Tue Oct 25 10:58:20 UTC 2016 (9464f67)
    x86_64 x86_64 x86_64 GNU/Linux

 run-level 3 Oct 27 20:30

 SPEC is set to: /opt/cpu2017
    Filesystem      Type    Size   Used Avail Use% Mounted on
```

(Continued on next page)

SPEC CPU®2017 Integer Rate Result

Cisco Systems

Cisco UCS C480 M5 (Intel Xeon Platinum 8158, 3.00GHz)

SPECrate®2017_int_base = 308

SPECrate®2017_int_peak = 324

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Oct-2017
Hardware Availability: Aug-2017
Software Availability: Sep-2017

Platform Notes (Continued)

```
      /dev/sdc1       btrfs  1.9T  136G  1.7T   8% /opt

 Additional information from dmidecode follows.  WARNING: Use caution when you interpret
 this section. The 'dmidecode' program reads system data which is "intended to allow
 hardware to be accurately determined", but the intent may not be met, as there are
 frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
   BIOS Cisco Systems, Inc. C480M5.3.1.0.272.0613172154 06/13/2017
   Memory:
    48x 0xCE00 M393A2G40EB2-CTD 16 GB 2 rank 2666

 (End of data from sysinfo program)
```

Compiler Version Notes

```
==============================================================================
C        | 500.perlbench_r(base, peak) 502.gcc_r(base, peak) 505.mcf_r(base,
         | peak) 525.x264_r(base, peak) 557.xz_r(base, peak)
------------------------------------------------------------------------------
icc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation.  All rights reserved.
------------------------------------------------------------------------------


==============================================================================
C++      | 520.omnetpp_r(base, peak) 523.xalancbmk_r(base, peak)
         | 531.deepsjeng_r(base, peak) 541.leela_r(base, peak)
------------------------------------------------------------------------------
icpc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation.  All rights reserved.
------------------------------------------------------------------------------


==============================================================================
Fortran | 548.exchange2_r(base, peak)
------------------------------------------------------------------------------
ifort (IFORT) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation.  All rights reserved.
------------------------------------------------------------------------------
```

Base Compiler Invocation

C benchmarks:
icc

C++ benchmarks:
icpc

Standard Performance Evaluation Corporation (info@spec.org)
https://www.spec.org/

Cisco Systems

Cisco UCS C480 M5 (Intel Xeon Platinum 8158, 3.00GHz)

SPECrate®2017_int_base = 308

SPECrate®2017_int_peak = 324

CPU2017 License:	9019	**Test Date:**	Oct-2017
Test Sponsor:	Cisco Systems	**Hardware Availability:**	Aug-2017
Tested by:	Cisco Systems	**Software Availability:**	Sep-2017

Base Compiler Invocation (Continued)

Fortran benchmarks:
`ifort`

Base Portability Flags

500.perlbench_r: `-DSPEC_LP64 -DSPEC_LINUX_X64`
502.gcc_r: `-DSPEC_LP64`
505.mcf_r: `-DSPEC_LP64`
520.omnetpp_r: `-DSPEC_LP64`
523.xalancbmk_r: `-DSPEC_LP64 -DSPEC_LINUX`
525.x264_r: `-DSPEC_LP64`
531.deepsjeng_r: `-DSPEC_LP64`
541.leela_r: `-DSPEC_LP64`
548.exchange2_r: `-DSPEC_LP64`
557.xz_r: `-DSPEC_LP64`

Base Optimization Flags

C benchmarks:
`-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div`
`-qopt-mem-layout-trans=3 -L/usr/local/je5.0.1-64/lib -ljemalloc`

C++ benchmarks:
`-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div`
`-qopt-mem-layout-trans=3 -L/usr/local/je5.0.1-64/lib -ljemalloc`

Fortran benchmarks:
`-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div`
`-qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte`
`-L/usr/local/je5.0.1-64/lib -ljemalloc`

Base Other Flags

C benchmarks:
`-m64 -std=c11`

C++ benchmarks:
`-m64`

(Continued on next page)

Cisco Systems

Cisco UCS C480 M5 (Intel Xeon Platinum 8158, 3.00GHz)

SPECrate®2017_int_base = 308

SPECrate®2017_int_peak = 324

Base Other Flags (Continued)

Fortran benchmarks:

`-m64`

Peak Compiler Invocation

C benchmarks:

`icc`

C++ benchmarks:

`icpc`

Fortran benchmarks:

`ifort`

Peak Portability Flags

500.perlbench_r: `-DSPEC_LP64 -DSPEC_LINUX_X64`
502.gcc_r: `-D_FILE_OFFSET_BITS=64`
505.mcf_r: `-DSPEC_LP64`
520.omnetpp_r: `-DSPEC_LP64`
523.xalancbmk_r: `-D_FILE_OFFSET_BITS=64 -DSPEC_LINUX`
525.x264_r: `-DSPEC_LP64`
531.deepsjeng_r: `-DSPEC_LP64`
541.leela_r: `-DSPEC_LP64`
548.exchange2_r: `-DSPEC_LP64`
557.xz_r: `-DSPEC_LP64`

Peak Optimization Flags

C benchmarks:

500.perlbench_r: `-Wl,-z,muldefs -prof-gen`(pass 1) `-prof-use`(pass 2) `-ipo`
`-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3`
`-fno-strict-overflow -L/usr/local/je5.0.1-64/lib`
`-ljemalloc`

502.gcc_r: `-L/opt/intel/compilers_and_libraries_2018/linux/lib/ia32`
`-Wl,-z,muldefs -prof-gen`(pass 1) `-prof-use`(pass 2) `-ipo`
`-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3`
`-L/usr/local/je5.0.1-32/lib -ljemalloc`

(Continued on next page)

Cisco Systems

Cisco UCS C480 M5 (Intel Xeon Platinum 8158, 3.00GHz)

SPECrate®2017_int_base = 308

SPECrate®2017_int_peak = 324

CPU2017 License:	9019	**Test Date:**	Oct-2017
Test Sponsor:	Cisco Systems	**Hardware Availability:**	Aug-2017
Tested by:	Cisco Systems	**Software Availability:**	Sep-2017

Peak Optimization Flags (Continued)

505.mcf_r: `-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-mem-layout-trans=3 -L/usr/local/je5.0.1-64/lib -ljemalloc`

525.x264_r: `-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-mem-layout-trans=3 -fno-alias -L/usr/local/je5.0.1-64/lib -ljemalloc`

557.xz_r: `Same as 505.mcf_r`

C++ benchmarks:

520.omnetpp_r: `-Wl,-z,muldefs` -prof-gen(pass 1) -prof-use(pass 2) `-ipo -xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3 -L/usr/local/je5.0.1-64/lib -ljemalloc`

523.xalancbmk_r: `-L/opt/intel/compilers_and_libraries_2018/linux/lib/ia32 -Wl,-z,muldefs` -prof-gen(pass 1) -prof-use(pass 2) `-ipo -xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3 -L/usr/local/je5.0.1-32/lib -ljemalloc`

531.deepsjeng_r: `Same as 520.omnetpp_r`

541.leela_r: `Same as 520.omnetpp_r`

Fortran benchmarks:
`-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte -L/usr/local/je5.0.1-64/lib -ljemalloc`

Peak Other Flags

C benchmarks (except as noted below):
`-m64 -std=c11`

502.gcc_r: `-m32 -std=c11`

C++ benchmarks (except as noted below):
`-m64`

523.xalancbmk_r: `-m32`

(Continued on next page)

Standard Performance Evaluation Corporation (info@spec.org)   https://www.spec.org/

Cisco Systems

Cisco UCS C480 M5 (Intel Xeon Platinum 8158, 3.00GHz)

SPECrate®2017_int_base = 308

SPECrate®2017_int_peak = 324

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Oct-2017
Hardware Availability: Aug-2017
Software Availability: Sep-2017

Peak Other Flags (Continued)

Fortran benchmarks:

-m64

The flags files that were used to format this result can be browsed at

http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.html
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revH.html

---

You can also download the XML flags sources by saving the following links:

http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.xml
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revH.xml

---

For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.0.2 on 2017-10-28 14:00:11-0400.
Report generated on 2020-09-03 17:41:22 by CPU2017 PDF formatter v6255.
Originally published on 2017-11-14.