



SPEC CPU®2017 Integer Rate Result

Copyright 2017-2024 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS C240 M7 (Intel Xeon Bronze 3508U, 2.10GHz)

SPECrate®2017_int_base = 46.1

SPECrate®2017_int_peak = 47.3

CPU2017 License: 9019

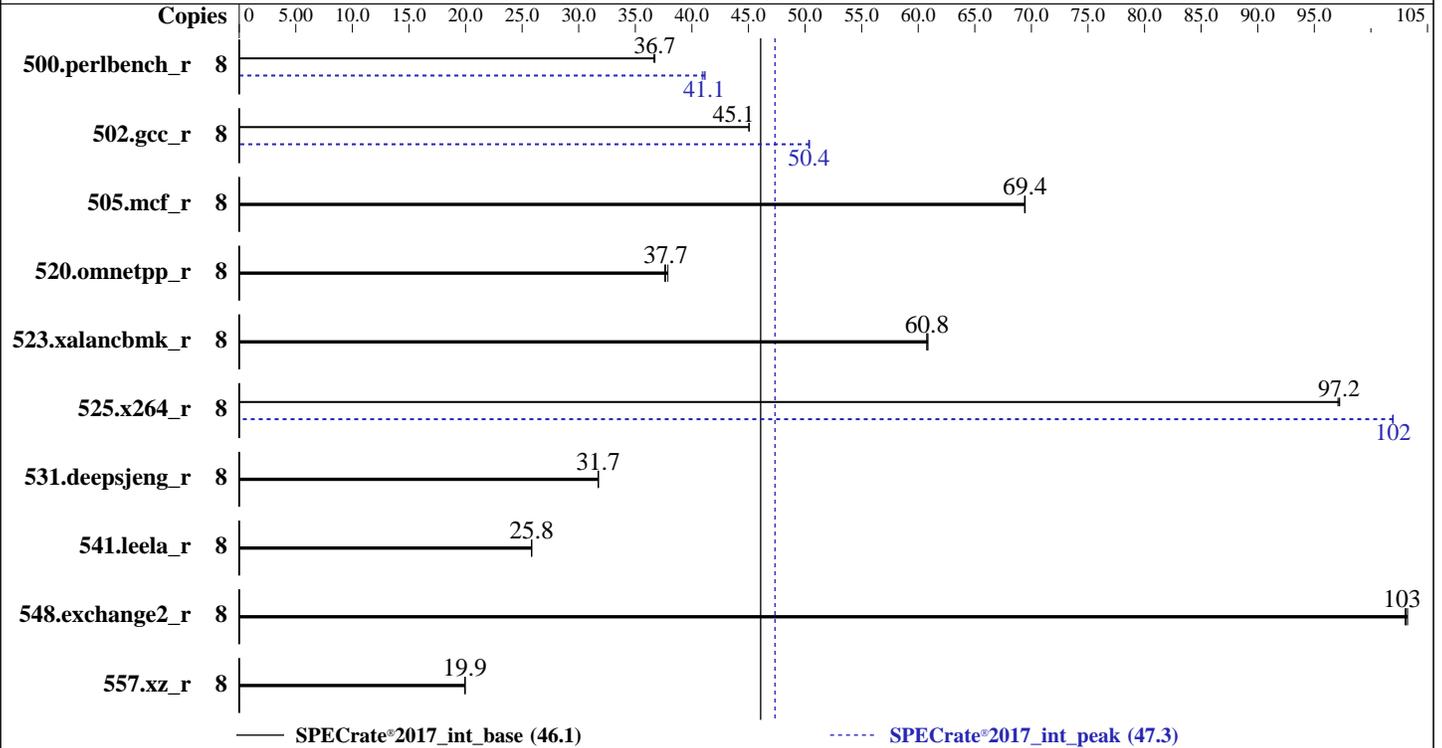
Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Apr-2024

Hardware Availability: Feb-2024

Software Availability: Dec-2023



Hardware

CPU Name: Intel Xeon Bronze 3508U
 Max MHz: 2200
 Nominal: 2100
 Enabled: 8 cores, 1 chip
 Orderable: 1 Chips
 Cache L1: 32 KB I + 48 KB D on chip per core
 L2: 2 MB I+D on chip per core
 L3: 22.5 MB I+D on chip per chip
 Other: None
 Memory: 512 GB (8 x 64 GB 2Rx4 PC5-5600B-R, running at 4400)
 Storage: 1 x 960 GB M.2 SSD SATA
 Other: CPU Cooling: Air

Software

OS: SUSE Linux Enterprise Server 15 SP5
 5.14.21-150500.53-default
 Compiler: C/C++: Version 2023.2.3 of Intel oneAPI DPC++/C++ Compiler for Linux;
 Fortran: Version 2023.2.3 of Intel Fortran Compiler for Linux;
 Parallel: No
 Firmware: Version 4.3.3a released Jan-2024
 File System: btrfs
 System State: Run level 3 (multi-user)
 Base Pointers: 64-bit
 Peak Pointers: 32/64-bit
 Other: jemalloc memory allocator V5.0.1
 Power Management: BIOS set to prefer performance at the cost of additional power usage



SPEC CPU®2017 Integer Rate Result

Copyright 2017-2024 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS C240 M7 (Intel Xeon Bronze 3508U, 2.10GHz)

SPECrate®2017_int_base = 46.1

SPECrate®2017_int_peak = 47.3

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Apr-2024
Hardware Availability: Feb-2024
Software Availability: Dec-2023

Results Table

Benchmark	Base							Peak						
	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
500.perlbench_r	8	348	36.6	<u>347</u>	<u>36.7</u>	347	36.7	8	<u>310</u>	<u>41.1</u>	311	40.9	309	41.2
502.gcc_r	8	251	45.1	251	45.0	<u>251</u>	<u>45.1</u>	8	<u>225</u>	<u>50.4</u>	225	50.4	225	50.3
505.mcf_r	8	186	69.4	<u>186</u>	<u>69.4</u>	186	69.4	8	186	69.4	<u>186</u>	<u>69.4</u>	186	69.4
520.omnetpp_r	8	279	37.6	<u>279</u>	<u>37.7</u>	277	37.9	8	279	37.6	<u>279</u>	<u>37.7</u>	277	37.9
523.xalancbmk_r	8	<u>139</u>	<u>60.8</u>	139	60.9	139	60.8	8	<u>139</u>	<u>60.8</u>	139	60.9	139	60.8
525.x264_r	8	144	97.2	<u>144</u>	<u>97.2</u>	144	97.1	8	<u>137</u>	<u>102</u>	137	102	137	102
531.deepsjeng_r	8	<u>289</u>	<u>31.7</u>	289	31.7	289	31.7	8	<u>289</u>	<u>31.7</u>	289	31.7	289	31.7
541.leela_r	8	513	25.8	513	25.8	<u>513</u>	<u>25.8</u>	8	513	25.8	513	25.8	<u>513</u>	<u>25.8</u>
548.exchange2_r	8	203	103	203	103	<u>203</u>	<u>103</u>	8	203	103	203	103	<u>203</u>	<u>103</u>
557.xz_r	8	<u>433</u>	<u>19.9</u>	433	19.9	433	20.0	8	<u>433</u>	<u>19.9</u>	433	19.9	433	20.0

SPECrate®2017_int_base = 46.1

SPECrate®2017_int_peak = 47.3

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

Environment Variables Notes

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/lib/ia32:/home/cpu2017/je5.0.1-32"
MALLOC_CONF = "retain:true"

General Notes

Binaries compiled on a system with 2x Intel Xeon Platinum 8280M CPU + 384GB RAM memory using Red Hat Enterprise Linux 8.4
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3> /proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:
numactl --interleave=all runcpu <etc>
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.
jemalloc, a general purpose malloc implementation

(Continued on next page)



SPEC CPU®2017 Integer Rate Result

Copyright 2017-2024 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS C240 M7 (Intel Xeon Bronze 3508U, 2.10GHz)

SPECrate®2017_int_base = 46.1

SPECrate®2017_int_peak = 47.3

CPU2017 License: 9019

Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Apr-2024

Hardware Availability: Feb-2024

Software Availability: Dec-2023

General Notes (Continued)

built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5
sources available from jemalloc.net or <https://github.com/jemalloc/jemalloc/releases>

Platform Notes

BIOS Settings:

Sub NUMA Clustering set to Enable SNC2(2-clusters)
ADDDC Sparing set to Disabled
DCU Streamer Prefetch set to Disabled
Enhanced CPU performance set to Auto
LLC Dead Line set to Disabled
Processor C6 Report set to Enabled

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6732 of 2022-11-07 fe91c89b7ed5c36ae2c92cc097bec197
running on localhost Wed Apr 10 18:40:15 2024

SUT (System Under Test) info as seen by some common utilities.

Table of contents

1. uname -a
2. w
3. Username
4. ulimit -a
5. sysinfo process ancestry
6. /proc/cpuinfo
7. lscpu
8. numactl --hardware
9. /proc/meminfo
10. who -r
11. Systemd service manager version: systemd 249 (249.16+suse.171.gdad0071f15)
12. Failed units, from systemctl list-units --state=failed
13. Services, from systemctl list-unit-files
14. Linux kernel boot-time arguments, from /proc/cmdline
15. cpupower frequency-info
16. sysctl
17. /sys/kernel/mm/transparent_hugepage
18. /sys/kernel/mm/transparent_hugepage/khugepaged
19. OS release
20. Disk information
21. /sys/devices/virtual/dmi/id
22. dmidecode
23. BIOS

```

1. uname -a
Linux localhost 5.14.21-150500.53-default #1 SMP PREEMPT_DYNAMIC Wed May 10 07:56:26 UTC 2023 (b630043)
x86_64 x86_64 x86_64 GNU/Linux

```

```

2. w
18:40:15 up 6 min, 1 user, load average: 0.00, 0.03, 0.02
USER TTY FROM LOGIN@ IDLE JCPU PCPU WHAT
root tty1 - 18:38 7.00s 1.57s 0.09s -bash

```

(Continued on next page)



SPEC CPU®2017 Integer Rate Result

Copyright 2017-2024 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS C240 M7 (Intel Xeon Bronze 3508U, 2.10GHz)

SPECrate®2017_int_base = 46.1

SPECrate®2017_int_peak = 47.3

CPU2017 License: 9019

Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Apr-2024

Hardware Availability: Feb-2024

Software Availability: Dec-2023

Platform Notes (Continued)

3. Username

From environment variable \$USER: root

4. ulimit -a

```

core file size          (blocks, -c) unlimited
data seg size          (kbytes, -d) unlimited
scheduling priority    (-e) 0
file size              (blocks, -f) unlimited
pending signals        (-i) 2062684
max locked memory      (kbytes, -l) 64
max memory size        (kbytes, -m) unlimited
open files             (-n) 1024
pipe size              (512 bytes, -p) 8
POSIX message queues   (bytes, -q) 819200
real-time priority     (-r) 0
stack size             (kbytes, -s) unlimited
cpu time               (seconds, -t) unlimited
max user processes     (-u) 2062684
virtual memory         (kbytes, -v) unlimited
file locks             (-x) unlimited

```

5. sysinfo process ancestry

```

/usr/lib/systemd/systemd --switched-root --system --deserialize 30
login -- root
-bash
-bash
runcpu --nobuild --action validate --define default-platform-flags --define numcopies=8 -c
  ic2023.2.3-lin-sapphirerapids-rate-20231121.cfg --reportable --iterations 3 --define smt-on --define
  cores=4 --define physicalfirst --define invoke_with_interleave --define drop_caches --tune all -o all
  intrate
runcpu --nobuild --action validate --define default-platform-flags --define numcopies=8 --configfile
  ic2023.2.3-lin-sapphirerapids-rate-20231121.cfg --reportable --iterations 3 --define smt-on --define
  cores=4 --define physicalfirst --define invoke_with_interleave --define drop_caches --tune all
  --output_format all --nopower --runmode rate --tune base:peak --size refrate intrate --nopreenv
  --note-preenv --logfile $SPEC/tmp/CPU2017.076/templogs/preenv.intrate.076.0.log --lognum 076.0
  --from_runcpu 2
specperl $SPEC/bin/sysinfo
$SPEC = /home/cpu2017

```

6. /proc/cpuinfo

```

model name      : INTEL(R) XEON(R) BRONZE 3508U
vendor_id      : GenuineIntel
cpu family     : 6
model          : 143
stepping      : 8
microcode     : 0x2b000571
bugs          : spectre_v1 spectre_v2 spec_store_bypass swapgs eibrs_pbrsb
cpu cores     : 8
siblings      : 8
1 physical ids (chips)
8 processors (hardware threads)
physical id 0: core ids 0-7
physical id 0: apicids 0,2,4,6,8,10,12,14
Caution: /proc/cpuinfo data regarding chips, cores, and threads is not necessarily reliable, especially for
virtualized systems. Use the above data carefully.

```

(Continued on next page)



SPEC CPU®2017 Integer Rate Result

Copyright 2017-2024 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS C240 M7 (Intel Xeon Bronze 3508U, 2.10GHz)

SPECrate®2017_int_base = 46.1

SPECrate®2017_int_peak = 47.3

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Apr-2024
Hardware Availability: Feb-2024
Software Availability: Dec-2023

Platform Notes (Continued)

7. lscpu

From lscpu from util-linux 2.37.4:

```

Architecture:          x86_64
CPU op-mode(s):        32-bit, 64-bit
Address sizes:         46 bits physical, 57 bits virtual
Byte Order:            Little Endian
CPU(s):                8
On-line CPU(s) list:  0-7
Vendor ID:             GenuineIntel
Model name:            INTEL(R) XEON(R) BRONZE 3508U
CPU family:            6
Model:                 143
Thread(s) per core:   1
Core(s) per socket:   8
Socket(s):             1
Stepping:              8
CPU max MHz:           2200.0000
CPU min MHz:           800.0000
BogoMIPS:              4200.00
Flags:                 fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov pat pse36
                        clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
                        lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology
                        nonstop_tsc cpuid aperfmperf tsc_known_freq pni pclmulqdq dtes64 monitor
                        ds_cpl smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2
                        x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm
                        abm 3dnowprefetch cpuid_fault epb cat_l3 cat_l2 cdp_l3 invpcid_single
                        intel_ppin cdp_l2 ssbd mba ibrs ibpb stibp ibrs_enhanced fsgsbase
                        tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm cqm rdt_a avx512f
                        avx512dq rdseed adx smap avx512ifma clflushopt clwb intel_pt avx512cd
                        sha_ni avx512bw avx512vl xsaveopt xsavec xgetbv1 xsavec cqm_llc
                        cqm_occup_llc cqm_mbm_total cqm_mbm_local split_lock_detect avx_vnni
                        avx512_bf16 wbnoinvd dtherm ida arat pln pts hwp hwp_act_window hwp_epp
                        hwp_pkg_req avx512vbmi umip pku ospke waitpkg avx512_vbmi2 gfni vaes
                        vpclmulqdq avx512_vnni avx512_bitalg tme avx512_vpopcntdq la57 rdpid
                        bus_lock_detect cldemote movdiri movdir64b enqcmd fsrm md_clear serialize
                        tsxldtrk pconfig arch_lbr avx512_fp16 flush_l1d arch_capabilities

L1d cache:             384 KiB (8 instances)
L1i cache:             256 KiB (8 instances)
L2 cache:              16 MiB (8 instances)
L3 cache:              22.5 MiB (1 instance)
NUMA node(s):         2
NUMA node0 CPU(s):   0-3
NUMA node1 CPU(s):   4-7
Vulnerability Itlb multihit: Not affected
Vulnerability L1tf:   Not affected
Vulnerability Mds:    Not affected
Vulnerability Meltdown: Not affected
Vulnerability Mmio stale data: Not affected
Vulnerability Retbleed: Not affected
Vulnerability Spec store bypass: Mitigation; Speculative Store Bypass disabled via prctl and seccomp
Vulnerability Spectre v1: Mitigation; usercopy/swapgs barriers and __user pointer sanitization
Vulnerability Spectre v2: Mitigation; Enhanced IBRS, IBPB conditional, RSB filling, PBRSE-eIBRS SW
                        sequence
Vulnerability Srbds:  Not affected
Vulnerability Tsx async abort: Not affected

```

From lscpu --cache:

NAME	ONE-SIZE	ALL-SIZE	WAYS	TYPE	LEVEL	SETS	PHY-LINE	COHERENCY-SIZE

(Continued on next page)



SPEC CPU®2017 Integer Rate Result

Copyright 2017-2024 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS C240 M7 (Intel Xeon Bronze 3508U, 2.10GHz)

SPECrate®2017_int_base = 46.1

SPECrate®2017_int_peak = 47.3

CPU2017 License: 9019

Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Apr-2024

Hardware Availability: Feb-2024

Software Availability: Dec-2023

Platform Notes (Continued)

L1d	48K	384K	12 Data	1	64	1	64
L1i	32K	256K	8 Instruction	1	64	1	64
L2	2M	16M	16 Unified	2	2048	1	64
L3	22.5M	22.5M	15 Unified	3	24576	1	64

8. numactl --hardware

NOTE: a numactl 'node' might or might not correspond to a physical chip.

```

available: 2 nodes (0-1)
node 0 cpus: 0-3
node 0 size: 257694 MB
node 0 free: 257040 MB
node 1 cpus: 4-7
node 1 size: 258007 MB
node 1 free: 256687 MB
node distances:
node  0  1
  0: 10 12
  1: 12 10

```

9. /proc/meminfo

MemTotal: 528078696 kB

10. who -r

run-level 3 Apr 10 18:33

11. Systemd service manager version: systemd 249 (249.16+suse.171.gdad0071f15)

```

Default Target Status
multi-user      degraded

```

12. Failed units, from systemctl list-units --state=failed

```

UNIT          LOAD ACTIVE SUB    DESCRIPTION
* smartd.service loaded failed failed Self Monitoring and Reporting Technology (SMART) Daemon

```

13. Services, from systemctl list-unit-files

```

STATE          UNIT FILES
enabled        YaST2-Firstboot YaST2-Second-Stage apparmor auditd cron display-manager getty@ irqbalance
                chronyd console-getty cups cups-browsed debug-shell ebttables exchange-bmc-os-info
                issue-generator kbdsettings klog lvm2-monitor nscd postfix purge-kernels rollback rsyslog
                smartd sshd systemd-pstore wicked wickedd-auto4 wickedd-dhcp4 wickedd-dhcp6 wickedd-nanny
enabled-runtime systemd-remount-fs
disabled       autofs autoyast-initscripts blk-availability boot-sysctl ca-certificates chrony-wait
                chronyd console-getty cups cups-browsed debug-shell ebttables exchange-bmc-os-info
                firewallld gpm grub2-once haveged haveged-switch-root ipmi ipmievd issue-add-ssh-keys
                kexec-load lunmask man-db-create multipathd nfs nfs-blkmap rpcbind rpmconfigcheck rsyncd
                serial-getty@ smartd_generate_opts snmpd snmptrapd systemd-boot-check-no-failures
                systemd-network-generator systemd-sysext systemd-time-wait-sync systemd-timesyncd udisks2
                vncserver@
indirect       wickedd

```

14. Linux kernel boot-time arguments, from /proc/cmdline

```

BOOT_IMAGE=/boot/vmlinuz-5.14.21-150500.53-default
root=UUID=a52509ae-6843-4da4-9108-8987d04eb252
splash=silent
mitigations=auto

```

(Continued on next page)



SPEC CPU®2017 Integer Rate Result

Copyright 2017-2024 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS C240 M7 (Intel Xeon Bronze 3508U, 2.10GHz)

SPECrate®2017_int_base = 46.1

SPECrate®2017_int_peak = 47.3

CPU2017 License: 9019

Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Apr-2024

Hardware Availability: Feb-2024

Software Availability: Dec-2023

Platform Notes (Continued)

```
quiet
security=apparmor
```

```
-----
15. cpupower frequency-info
analyzing CPU 0:
  current policy: frequency should be within 800 MHz and 2.20 GHz.
                   The governor "performance" may decide which speed to use
                   within this range.
  boost state support:
    Supported: yes
    Active: yes
```

```
-----
16. sysctl
kernel.numa_balancing          1
kernel.randomize_va_space     2
vm.compaction_proactiveness    20
vm.dirty_background_bytes      0
vm.dirty_background_ratio      10
vm.dirty_bytes                 0
vm.dirty_expire_centisecs     3000
vm.dirty_ratio                 20
vm.dirty_writeback_centisecs   500
vm.dirtytime_expire_seconds    43200
vm.extfrag_threshold           500
vm.min_unmapped_ratio          1
vm.nr_hugepages                0
vm.nr_hugepages_mempolicy      0
vm.nr_overcommit_hugepages     0
vm.swappiness                  1
vm.watermark_boost_factor      15000
vm.watermark_scale_factor      10
vm.zone_reclaim_mode           0
```

```
-----
17. /sys/kernel/mm/transparent_hugepage
defrag          always defer defer+madvice [madvice] never
enabled         [always] madvice never
hpage_pmd_size  2097152
shmem_enabled   always within_size advise [never] deny force
```

```
-----
18. /sys/kernel/mm/transparent_hugepage/khugepaged
alloc_sleep_millisecs  60000
defrag                 1
max_ptes_none          511
max_ptes_shared        256
max_ptes_swap          64
pages_to_scan          4096
scan_sleep_millisecs   10000
```

```
-----
19. OS release
From /etc/*-release /etc/*-version
os-release SUSE Linux Enterprise Server 15 SP5
```

```
-----
20. Disk information
SPEC is set to: /home/cpu2017
```

(Continued on next page)



SPEC CPU®2017 Integer Rate Result

Copyright 2017-2024 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS C240 M7 (Intel Xeon Bronze 3508U, 2.10GHz)

SPECrate®2017_int_base = 46.1

SPECrate®2017_int_peak = 47.3

CPU2017 License: 9019

Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Apr-2024

Hardware Availability: Feb-2024

Software Availability: Dec-2023

Platform Notes (Continued)

Filesystem	Type	Size	Used	Avail	Use%	Mounted on
/dev/sda2	btrfs	222G	20G	198G	10%	/home

```

21. /sys/devices/virtual/dmi/id
Vendor:      Cisco Systems Inc
Product:     UCSC-C240-M7SX
Serial:      WZP27100DJ5

```

```

22. dmidecode
Additional information from dmidecode 3.4 follows.  WARNING: Use caution when you interpret this section.
The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately
determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the
"DMTF SMBIOS" standard.
Memory:
  8x 0xCE00 M321R8GA0PB0-CWMCH 64 GB 2 rank 5600, configured at 4400

```

```

23. BIOS
(This section combines info from /sys/devices and dmidecode.)
BIOS Vendor:      Cisco Systems, Inc.
BIOS Version:     C240M7.4.3.3a.0.0118241337
BIOS Date:        01/18/2024
BIOS Revision:    5.32

```

Compiler Version Notes

```

=====
C | 502.gcc_r(peak)
=====

```

```

Intel(R) oneAPI DPC++/C++ Compiler for applications running on IA-32, Version 2023.2.3 Build x
Copyright (C) 1985-2023 Intel Corporation. All rights reserved.
=====

```

```

=====
C | 500.perlbench_r(base, peak) 502.gcc_r(base) 505.mcf_r(base, peak) 525.x264_r(base, peak)
  | 557.xz_r(base, peak)
=====

```

```

Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2023.2.3 Build x
Copyright (C) 1985-2023 Intel Corporation. All rights reserved.
=====

```

```

=====
C | 502.gcc_r(peak)
=====

```

```

Intel(R) oneAPI DPC++/C++ Compiler for applications running on IA-32, Version 2023.2.3 Build x
Copyright (C) 1985-2023 Intel Corporation. All rights reserved.
=====

```

```

=====
C | 500.perlbench_r(base, peak) 502.gcc_r(base) 505.mcf_r(base, peak) 525.x264_r(base, peak)
  | 557.xz_r(base, peak)
=====

```

```

Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2023.2.3 Build x
Copyright (C) 1985-2023 Intel Corporation. All rights reserved.
=====

```

(Continued on next page)



SPEC CPU®2017 Integer Rate Result

Copyright 2017-2024 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS C240 M7 (Intel Xeon Bronze 3508U, 2.10GHz)

SPECrate®2017_int_base = 46.1

SPECrate®2017_int_peak = 47.3

CPU2017 License: 9019

Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Apr-2024

Hardware Availability: Feb-2024

Software Availability: Dec-2023

Compiler Version Notes (Continued)

C++ | 520.omnetpp_r(base, peak) 523.xalancbmk_r(base, peak) 531.deepsjeng_r(base, peak)
541.leela_r(base, peak)

Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2023.2.3 Build x
Copyright (C) 1985-2023 Intel Corporation. All rights reserved.

Fortran | 548.exchange2_r(base, peak)

Intel(R) Fortran Compiler for applications running on Intel(R) 64, Version 2023.2.3 Build x
Copyright (C) 1985-2023 Intel Corporation. All rights reserved.

Base Compiler Invocation

C benchmarks:

icx

C++ benchmarks:

icpx

Fortran benchmarks:

ifx

Base Portability Flags

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502 gcc_r: -DSPEC_LP64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64

Base Optimization Flags

C benchmarks:

-w -std=c11 -m64 -Wl,-z,muldefs -xsapphirerapids -O3 -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4

(Continued on next page)



SPEC CPU®2017 Integer Rate Result

Copyright 2017-2024 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS C240 M7 (Intel Xeon Bronze 3508U, 2.10GHz)

SPECrate®2017_int_base = 46.1

SPECrate®2017_int_peak = 47.3

CPU2017 License: 9019

Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Apr-2024

Hardware Availability: Feb-2024

Software Availability: Dec-2023

Base Optimization Flags (Continued)

C benchmarks (continued):

```
-L/home/specdev/new_compilers/ic2023.2.3/compiler/lib/intel64_lin
-lqkmallo
```

C++ benchmarks:

```
-w -std=c++14 -m64 -Wl,-z,muldefs -xsapphirerapids -O3 -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-L/home/specdev/new_compilers/ic2023.2.3/compiler/lib/intel64_lin
-lqkmallo
```

Fortran benchmarks:

```
-w -m64 -Wl,-z,muldefs -xsapphirerapids -O3 -ffast-math -flto
-mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-nostandard-realloc-lhs -align array32byte -auto
-L/home/specdev/new_compilers/ic2023.2.3/compiler/lib/intel64_lin
-lqkmallo
```

Peak Compiler Invocation

C benchmarks:

```
icx
```

C++ benchmarks:

```
icpx
```

Fortran benchmarks:

```
ifx
```

Peak Portability Flags

```
500.perlbenc_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -D_FILE_OFFSET_BITS=64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64
```



SPEC CPU®2017 Integer Rate Result

Copyright 2017-2024 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS C240 M7 (Intel Xeon Bronze 3508U, 2.10GHz)

SPECrate®2017_int_base = 46.1

SPECrate®2017_int_peak = 47.3

CPU2017 License: 9019

Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Apr-2024

Hardware Availability: Feb-2024

Software Availability: Dec-2023

Peak Optimization Flags

C benchmarks:

```
500.perlbench_r: -w -std=c11 -m64 -Wl,-z,muldefs
-fprofile-generate(pass 1)
-fprofile-use=default.profdata(pass 2) -xCORE-AVX2(pass 1)
-flto -Ofast -xCORE-AVX512 -ffast-math -mfpmath=sse
-funroll-loops -qopt-mem-layout-trans=4
-fno-strict-overflow
-L/home/specdev/new_compilers/ic2023.2.3/compiler/lib/intel64_lin
-lqkmallocc
```

```
502.gcc_r: -m32
-L/home/specdev/new_compilers/ic2023.2.3/compiler/lib/ia32_lin
-std=gnu89 -Wl,-z,muldefs -fprofile-generate(pass 1)
-fprofile-use=default.profdata(pass 2) -xCORE-AVX2(pass 1)
-flto -Ofast -xCORE-AVX512 -ffast-math -mfpmath=sse
-funroll-loops -qopt-mem-layout-trans=4
-L/usr/local/jemalloc32-5.0.1/lib -ljemallocc
```

505.mcf_r: basepeak = yes

```
525.x264_r: -w -std=c11 -m64 -Wl,-z,muldefs -xsapphirerapids -Ofast
-ffast-math -flto -mfpmath=sse -funroll-loops
-qopt-mem-layout-trans=4 -fno-alias
-L/home/specdev/new_compilers/ic2023.2.3/compiler/lib/intel64_lin
-lqkmallocc
```

557.xz_r: basepeak = yes

C++ benchmarks:

520.omnetpp_r: basepeak = yes

523.xalancbmk_r: basepeak = yes

531.deepsjeng_r: basepeak = yes

541.leela_r: basepeak = yes

Fortran benchmarks:

548.exchange2_r: basepeak = yes



SPEC CPU®2017 Integer Rate Result

Copyright 2017-2024 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS C240 M7 (Intel Xeon Bronze 3508U, 2.10GHz)

SPECrate®2017_int_base = 46.1

SPECrate®2017_int_peak = 47.3

CPU2017 License: 9019

Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Apr-2024

Hardware Availability: Feb-2024

Software Availability: Dec-2023

The flags files that were used to format this result can be browsed at

<http://www.spec.org/cpu2017/flags/Intel-ic2024-official-linux64.html>

<http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.0-EMR-revD.html>

You can also download the XML flags sources by saving the following links:

<http://www.spec.org/cpu2017/flags/Intel-ic2024-official-linux64.xml>

<http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.0-EMR-revD.xml>

SPEC CPU and SPECrate are registered trademarks of the Standard Performance Evaluation Corporation. All other brand and product names appearing in this result are trademarks or registered trademarks of their respective holders.

For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.1.9 on 2024-04-10 21:40:15-0400.

Report generated on 2024-05-07 22:21:53 by CPU2017 PDF formatter v6716.

Originally published on 2024-05-07.