SPEC CPU®2017 Integer Speed Result

Cisco Systems

Cisco UCS C245 M6 (AMD EPYC 7282 16-core) Processor)

$SPECspeed^{®}2017\_int\_base = 8.41$

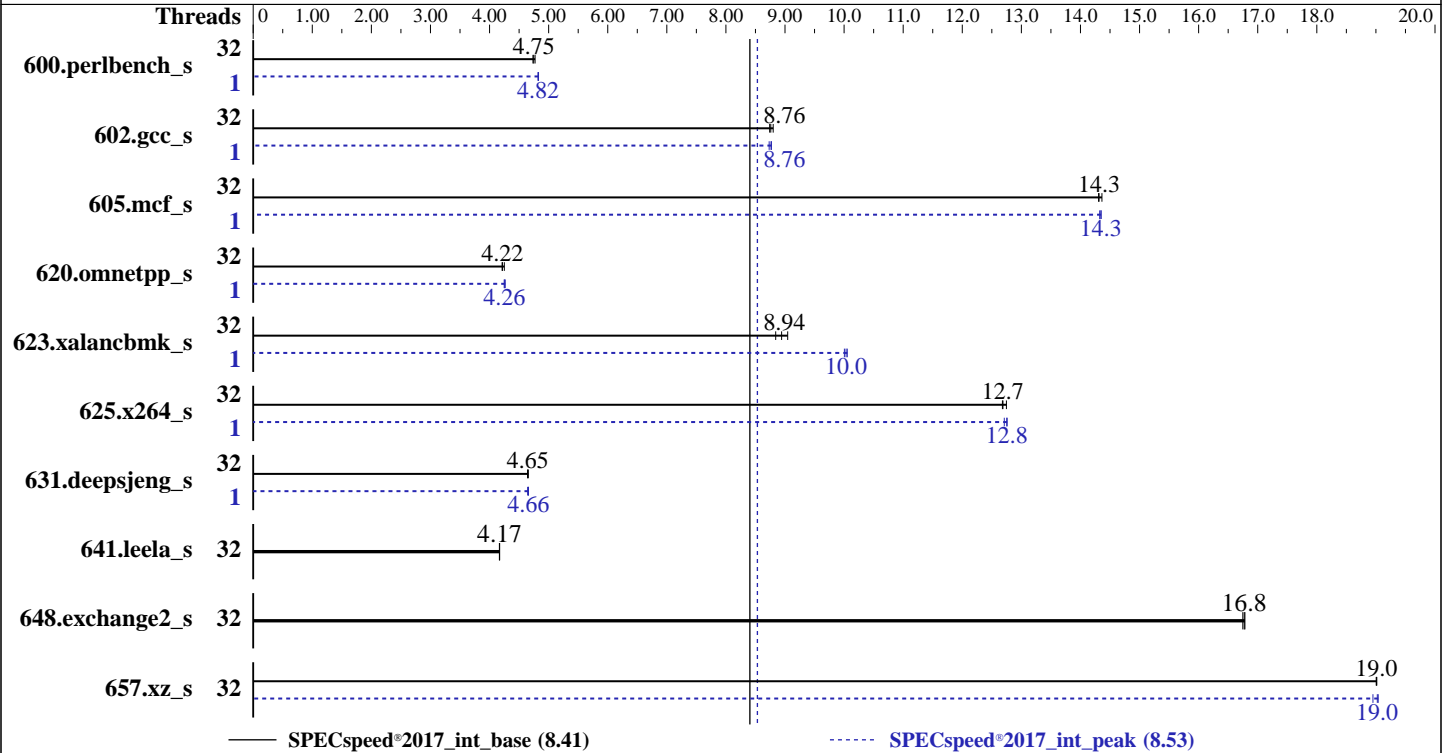$SPECspeed^{®}2017\_int\_peak = 8.53$

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Oct-2022
Hardware Availability: Aug-2021
Software Availability: Dec-2021

Threads	Benchmark	Base	Peak
	600.perlbench_s	4.75 (32)	4.82 (1)
	602.gcc_s	8.76 (32)	8.76 (1)
	605.mcf_s	14.3 (32)	14.3 (1)
	620.omnetpp_s	4.22 (32)	4.26 (1)
	623.xalancbmk_s	8.94 (32)	10.0 (1)
	625.x264_s	12.7 (32)	12.8 (1)
	631.deepsjeng_s	4.65 (32)	4.66 (1)
	641.leela_s	4.17 (32)	
	648.exchange2_s	16.8 (32)	
	657.xz_s	19.0 (32)	19.0

SPECspeed®2017_int_base (8.41)
SPECspeed®2017_int_peak (8.53)

Hardware

CPU Name: AMD EPYC 7282
 Max MHz: 3200
 Nominal: 2800
Enabled: 32 cores, 2 chips
Orderable: 1,2 chips
Cache L1: 32 KB I + 32 KB D on chip per core
 L2: 512 KB I+D on chip per core
 L3: 64 MB I+D on chip per chip, 16 MB shared / 4 cores
 Other: None
Memory: 2 TB (16 x 128 GB 4Rx4 PC4-3200AA-L)
Storage: 1 x 960 GB M.2 SSD SATA
Other: None

Software

OS: SUSE Linux Enterprise Server 15 SP3 (x86_64) kernel version 5.3.18-57-default
Compiler: C/C++/Fortran: Version 3.2.0 of AOCC
Parallel: Yes
Firmware: Version 4.2.2b released May-2022
File System: xfs
System State: Run level 3 (multi-user)
Base Pointers: 64-bit
Peak Pointers: 64-bit
Other: jemalloc: jemalloc memory allocator library v5.1.0
Power Management: BIOS and OS set to prefer performance at the cost of additional power usage

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Results Table

Benchmark	Base							Peak						
	Threads	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Threads	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
600.perlbench_s	32	375	4.73	**374**	**4.75**	372	4.77	1	368	4.83	368	4.82	**368**	**4.82**
602.gcc_s	32	**455**	**8.76**	456	8.74	452	8.80	1	456	8.73	**454**	**8.76**	454	8.77
605.mcf_s	32	330	14.3	**330**	**14.3**	329	14.4	1	330	14.3	**329**	**14.3**	329	14.3
620.omnetpp_s	32	384	4.25	**387**	**4.22**	387	4.21	1	382	4.26	**383**	**4.26**	384	4.25
623.xalancbmk_s	32	160	8.84	157	9.05	**158**	**8.94**	1	**141**	**10.0**	142	10.0	141	10.1
625.x264_s	32	138	12.7	139	12.7	**139**	**12.7**	1	139	12.7	**138**	**12.8**	138	12.8
631.deepsjeng_s	32	308	4.66	**308**	**4.65**	309	4.64	1	308	4.66	**308**	**4.66**	309	4.64
641.leela_s	32	409	4.17	**409**	**4.17**	409	4.17	32	409	4.17	**409**	**4.17**	409	4.17
648.exchange2_s	32	**175**	**16.8**	175	16.8	176	16.7	32	**175**	**16.8**	175	16.8	176	16.7
657.xz_s	32	325	19.0	325	19.0	**325**	**19.0**	32	325	19.0	**325**	**19.0**	326	19.0
SPECspeed®2017_int_base =			**8.41**											
SPECspeed®2017_int_peak =			**8.53**											

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Compiler Notes

```
The AMD64 AOCC Compiler Suite is available at
http://developer.amd.com/amd-aocc/
```

Submit Notes

```
The config file option 'submit' was used.
'numactl' was used to bind copies to the cores.
See the configuration file for details.
```

Operating System Notes

```
'ulimit -s unlimited' was used to set environment stack size limit
'ulimit -l 2097152' was used to set environment locked pages in memory limit

runcpu command invoked through numactl i.e.:
numactl --interleave=all runcpu <etc>

To limit dirty cache to 8% of memory, 'sysctl -w vm.dirty_ratio=8' run as root.
To limit swap usage to minimum necessary, 'sysctl -w vm.swappiness=1' run as root.
To free node-local memory and avoid remote memory usage,
'sysctl -w vm.zone_reclaim_mode=1' run as root.
To clear filesystem caches, 'sync; sysctl -w vm.drop_caches=3' run as root.
To disable address space layout randomization (ASLR) to reduce run-to-run
variability, 'sysctl -w kernel.randomize_va_space=0' run as root.

To enable Transparent Hugepages (THP) for all allocations,
```

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Operating System Notes (Continued)

```
'echo always > /sys/kernel/mm/transparent_hugepage/enabled' and
'echo always > /sys/kernel/mm/transparent_hugepage/defrag' run as root.
```

Environment Variables Notes

```
Environment variables set by runcpu before the start of the run:
GOMP_CPU_AFFINITY = "0-31"
LD_LIBRARY_PATH =
     "/home/cpu2017/amd_speed_aocc320_milanx_A_lib/lib;/home/cpu2017/amd_spee
     d_aocc320_milanx_A_lib/lib32:"
LIBOMP_NUM_HIDDEN_HELPER_THREADS = "0"
MALLOC_CONF = "retain:true"
OMP_DYNAMIC = "false"
OMP_SCHEDULE = "static"
OMP_STACKSIZE = "128M"
OMP_THREAD_LIMIT = "32"

Environment variables set by runcpu during the 600.perlbench_s peak run:
GOMP_CPU_AFFINITY = "0"

Environment variables set by runcpu during the 602.gcc_s peak run:
GOMP_CPU_AFFINITY = "0"

Environment variables set by runcpu during the 605.mcf_s peak run:
GOMP_CPU_AFFINITY = "0"

Environment variables set by runcpu during the 620.omnetpp_s peak run:
GOMP_CPU_AFFINITY = "0"

Environment variables set by runcpu during the 623.xalancbmk_s peak run:
GOMP_CPU_AFFINITY = "0"

Environment variables set by runcpu during the 625.x264_s peak run:
GOMP_CPU_AFFINITY = "0"

Environment variables set by runcpu during the 631.deepsjeng_s peak run:
GOMP_CPU_AFFINITY = "0"

Environment variables set by runcpu during the 657.xz_s peak run:
GOMP_CPU_AFFINITY = "0-31"
LIBOMP_NUM_HIDDEN_HELPER_THREADS = "0"
```

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General Notes

Binaries were compiled on a system with 2x AMD EPYC 7742 CPU + 1TiB Memory using openSUSE 15.2

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2)
is mitigated in the system as tested and documented.

jemalloc: configured and built with GCC v4.8.2 in RHEL 7.4 (No options specified)
jemalloc 5.1.0 is available here:
https://github.com/jemalloc/jemalloc/releases/download/5.1.0/jemalloc-5.1.0.tar.bz2

Platform Notes

BIOS Configuration
 SMT Mode set to Disabled
 NUMA nodes per socket set to NPS1
 ACPI SRAT L3 Cache As NUMA Domain set to Enabled
 DRAM Scrub Time set to Disabled
 Determinism Slider set to Power
 L1 Stream HW Prefetcher set to Enabled
 APBDIS set to 1

 Sysinfo program /home/cpu2017/bin/sysinfo
 Rev: r6622 of 2021-04-07 982a61ec0915b55891ef0e16acafc64d
 running on SPEC-SRV02 Wed Oct 26 10:16:09 2022

 SUT (System Under Test) info as seen by some common utilities.
 For more information on this section, see
    https://www.spec.org/cpu2017/Docs/config.html#sysinfo

 From /proc/cpuinfo
    model name : AMD EPYC 7282 16-Core Processor
       2 "physical id"s (chips)
      32 "processors"
    cores, siblings (Caution: counting these is hw and system dependent. The following
    excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
       cpu cores : 16
       siblings : 16
       physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
       physical 1: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

 From lscpu from util-linux 2.36.2:
      Architecture: x86_64

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Platform Notes (Continued)

```
CPU op-mode(s):                 32-bit, 64-bit
Byte Order:                     Little Endian
Address sizes:                  43 bits physical, 48 bits virtual
CPU(s):                         32
On-line CPU(s) list:            0-31
Thread(s) per core:             1
Core(s) per socket:             16
Socket(s):                      2
NUMA node(s):                   8
Vendor ID:                      AuthenticAMD
CPU family:                     23
Model:                          49
Model name:                     AMD EPYC 7282 16-Core Processor
Stepping:                       0
Frequency boost:                enabled
CPU MHz:                        1582.465
CPU max MHz:                    2800.0000
CPU min MHz:                    1500.0000
BogoMIPS:                       5589.16
Virtualization:                 AMD-V
L1d cache:                      1 MiB
L1i cache:                      1 MiB
L2 cache:                       16 MiB
L3 cache:                       128 MiB
NUMA node0 CPU(s):              0-3
NUMA node1 CPU(s):              4-7
NUMA node2 CPU(s):              8-11
NUMA node3 CPU(s):              12-15
NUMA node4 CPU(s):              16-19
NUMA node5 CPU(s):              20-23
NUMA node6 CPU(s):              24-27
NUMA node7 CPU(s):              28-31
Vulnerability Itlb multihit:    Not affected
Vulnerability L1tf:             Not affected
Vulnerability Mds:              Not affected
Vulnerability Meltdown:         Not affected
Vulnerability Spec store bypass: Mitigation; Speculative Store Bypass disabled via
prctl and seccomp
Vulnerability Spectre v1:        Mitigation; usercopy/swapgs barriers and __user
pointer sanitization
Vulnerability Spectre v2:        Mitigation; Full AMD retpoline, IBPB conditional,
IBRS_FW, STIBP disabled, RSB filling
Vulnerability Srbds:            Not affected
Vulnerability Tsx async abort:  Not affected
Flags:                          fpu vme de pse tsc msr pae mce cx8 apic sep mtrr
pge mca cmov pat pse36 clflush mmx fxsr sse sse2 ht syscall nx mmxext fxsr_opt
pdpe1gb rdtscp lm constant_tsc rep_good nopl nonstop_tsc cpuid extd_apicid
```

(Continued on next page)

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Platform Notes (Continued)

```
    aperfmperf pni pclmulqdq monitor ssse3 fma cx16 sse4_1 sse4_2 movbe popcnt aes xsave
    avx f16c rdrand lahf_lm cmp_legacy svm extapic cr8_legacy abm sse4a misalignsse
    3dnowprefetch osvw ibs skinit wdt tce topoext perfctr_core perfctr_nb bpext
    perfctr_llc mwaitx cpb cat_l3 cdp_l3 hw_pstate sme ssbd mba sev ibrs ibpb stibp
    vmmcall sev_es fsgsbase bmi1 avx2 smep bmi2 cqm rdt_a rdseed adx smap clflushopt
    clwb sha_ni xsaveopt xsavec xgetbv1 xsaves cqm_llc cqm_occup_llc cqm_mbm_total
    cqm_mbm_local clzero irperf xsaveerptr wbnoinvd arat npt lbrv svm_lock nrip_save
    tsc_scale vmcb_clean flushbyasid decodeassists pausefilter pfthreshold avic
    v_vmsave_vmload vgif umip rdpid overflow_recov succor smca

 From lscpu --cache:
    NAME ONE-SIZE ALL-SIZE WAYS TYPE          LEVEL   SETS PHY-LINE COHERENCY-SIZE
    L1d       32K       1M    8 Data            1     64       1             64
    L1i       32K       1M    8 Instruction     1     64       1             64
    L2       512K      16M    8 Unified         2   1024       1             64
    L3        16M     128M   16 Unified         3  16384       1             64

 /proc/cpuinfo cache data
    cache size : 512 KB

 From numactl --hardware
 WARNING: a numactl 'node' might or might not correspond to a physical chip.
   available: 8 nodes (0-7)
   node 0 cpus: 0 1 2 3
   node 0 size: 257863 MB
   node 0 free: 257666 MB
   node 1 cpus: 4 5 6 7
   node 1 size: 258046 MB
   node 1 free: 257925 MB
   node 2 cpus: 8 9 10 11
   node 2 size: 258012 MB
   node 2 free: 257899 MB
   node 3 cpus: 12 13 14 15
   node 3 size: 245937 MB
   node 3 free: 245806 MB
   node 4 cpus: 16 17 18 19
   node 4 size: 258046 MB
   node 4 free: 257547 MB
   node 5 cpus: 20 21 22 23
   node 5 size: 258046 MB
   node 5 free: 257796 MB
   node 6 cpus: 24 25 26 27
   node 6 size: 258046 MB
   node 6 free: 257806 MB
   node 7 cpus: 28 29 30 31
   node 7 size: 258045 MB
   node 7 free: 257891 MB
```

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Platform Notes (Continued)

```
  node distances:
  node   0   1   2   3   4   5   6   7
    0:  10  11  11  11  32  32  32  32
    1:  11  10  11  11  32  32  32  32
    2:  11  11  10  11  32  32  32  32
    3:  11  11  11  10  32  32  32  32
    4:  32  32  32  32  10  11  11  11
    5:  32  32  32  32  11  10  11  11
    6:  32  32  32  32  11  11  10  11
    7:  32  32  32  32  11  11  11  10

From /proc/meminfo
   MemTotal:       2101293916 kB
   HugePages_Total:        0
   Hugepagesize:        2048 kB

/sys/devices/system/cpu/cpu*/cpufreq/scaling_governor has
   performance

From /etc/*release* /etc/*version*
   os-release:
       NAME="SLES"
       VERSION="15-SP3"
       VERSION_ID="15.3"
       PRETTY_NAME="SUSE Linux Enterprise Server 15 SP3"
       ID="sles"
       ID_LIKE="suse"
       ANSI_COLOR="0;32"
       CPE_NAME="cpe:/o:suse:sles:15:sp3"

uname -a:
   Linux SPEC-SRV02 5.3.18-57-default #1 SMP Wed Apr 28 10:54:41 UTC 2021 (ba3c2e9)
   x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2018-12207 (iTLB Multihit):                  Not affected
CVE-2018-3620 (L1 Terminal Fault):               Not affected
Microarchitectural Data Sampling:                Not affected
CVE-2017-5754 (Meltdown):                        Not affected
CVE-2018-3639 (Speculative Store Bypass):        Mitigation: Speculative Store
                                                 Bypass disabled via prctl and
                                                 seccomp
CVE-2017-5753 (Spectre variant 1):               Mitigation: usercopy/swapgs
                                                 barriers and __user pointer
                                                 sanitization
CVE-2017-5715 (Spectre variant 2):               Mitigation: Full AMD retpoline,
```

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Platform Notes (Continued)

```
                                         IBPB: conditional, IBRS_FW, STIBP:
                                         disabled, RSB filling
 CVE-2020-0543 (Special Register Buffer Data Sampling): Not affected
 CVE-2019-11135 (TSX Asynchronous Abort):               Not affected

 run-level 3 Oct 25 04:30

 SPEC is set to: /home/cpu2017
    Filesystem      Type  Size  Used Avail Use% Mounted on
    /dev/sdb1       xfs   223G   21G  203G  10% /

 From /sys/devices/virtual/dmi/id
    Vendor:          Cisco Systems Inc
    Product:         UCSC-C245-M6SX
    Serial:          WZP251302NJ


 Additional information from dmidecode 3.2 follows.  WARNING: Use caution when you
 interpret this section. The 'dmidecode' program reads system data which is "intended to
 allow hardware to be accurately determined", but the intent may not be met, as there are
 frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
   Memory:
     16x 0xCE00 M386AAG40AM3-CWE 128 GB 4 rank 3200

 BIOS:
    BIOS Vendor:      Cisco Systems, Inc.
    BIOS Version:     C245M6.4.2.2b.0.0509222122
    BIOS Date:        05/09/2022
    BIOS Revision:    5.14

 (End of data from sysinfo program)
```

Compiler Version Notes

```
==============================================================================
C        | 600.perlbench_s(base, peak) 602.gcc_s(base, peak) 605.mcf_s(base,
         | peak) 625.x264_s(base, peak) 657.xz_s(base, peak)
------------------------------------------------------------------------------
AMD clang version 13.0.0 (CLANG: AOCC_3.2.0-Build#128 2021_11_12) (based on
  LLVM Mirror.Version.13.0.0)
Target: x86_64-unknown-linux-gnu
Thread model: posix
InstalledDir: /opt/AMD/aocc-compiler-3.2.0/bin
------------------------------------------------------------------------------


==============================================================================
C++      | 620.omnetpp_s(base, peak) 623.xalancbmk_s(base, peak)
```

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Compiler Version Notes (Continued)

```
         | 631.deepsjeng_s(base, peak) 641.leela_s(base, peak)
------------------------------------------------------------------------
AMD clang version 13.0.0 (CLANG: AOCC_3.2.0-Build#128 2021_11_12) (based on
  LLVM Mirror.Version.13.0.0)
Target: x86_64-unknown-linux-gnu
Thread model: posix
InstalledDir: /opt/AMD/aocc-compiler-3.2.0/bin
------------------------------------------------------------------------


========================================================================
Fortran | 648.exchange2_s(base, peak)
------------------------------------------------------------------------
AMD clang version 13.0.0 (CLANG: AOCC_3.2.0-Build#128 2021_11_12) (based on
  LLVM Mirror.Version.13.0.0)
Target: x86_64-unknown-linux-gnu
Thread model: posix
InstalledDir: /opt/AMD/aocc-compiler-3.2.0/bin
------------------------------------------------------------------------
```

Base Compiler Invocation

C benchmarks:
`clang`

C++ benchmarks:
`clang++`

Fortran benchmarks:
`flang`

Base Portability Flags

600.perlbench_s: `-DSPEC_LINUX_X64 -DSPEC_LP64`
602.gcc_s: `-DSPEC_LP64`
605.mcf_s: `-DSPEC_LP64`
620.omnetpp_s: `-DSPEC_LP64`
623.xalancbmk_s: `-DSPEC_LINUX -DSPEC_LP64`
625.x264_s: `-DSPEC_LP64`
631.deepsjeng_s: `-DSPEC_LP64`
641.leela_s: `-DSPEC_LP64`
648.exchange2_s: `-DSPEC_LP64`
657.xz_s: `-DSPEC_LP64`

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Base Optimization Flags

C benchmarks:

```
-m64 -Wl,-allow-multiple-definition -Wl,-mllvm -Wl,-enable-licm-vrp
-Wl,-mllvm -Wl,-region-vectorize -Wl,-mllvm -Wl,-function-specialize
-Wl,-mllvm -Wl,-align-all-nofallthru-blocks=6
-Wl,-mllvm -Wl,-reduce-array-computations=3 -O3 -march=znver3
-fveclib=AMDLIBM -ffast-math -fopenmp -flto -fstruct-layout=5
-mllvm -unroll-threshold=50 -mllvm -inline-threshold=1000
-fremap-arrays -mllvm -function-specialize -flv-function-specialization
-mllvm -enable-gvn-hoist -mllvm -global-vectorize-slp=true
-mllvm -enable-licm-vrp -mllvm -reduce-array-computations=3 -z muldefs
-DSPEC_OPENMP -fopenmp=libomp -lomp -lamdlibm -ljemalloc -lflang
```

C++ benchmarks:

```
-m64 -Wl,-mllvm -Wl,-region-vectorize
-Wl,-mllvm -Wl,-function-specialize
-Wl,-mllvm -Wl,-align-all-nofallthru-blocks=6
-Wl,-mllvm -Wl,-reduce-array-computations=3 -O3 -march=znver3
-fveclib=AMDLIBM -ffast-math -fopenmp -flto
-mllvm -enable-partial-unswitch -mllvm -unroll-threshold=100
-finline-aggressive -flv-function-specialization
-mllvm -loop-unswitch-threshold=200000 -mllvm -reroll-loops
-mllvm -aggressive-loop-unswitch -mllvm -extra-vectorizer-passes
-mllvm -reduce-array-computations=3 -mllvm -global-vectorize-slp=true
-mllvm -convert-pow-exp-to-int=false -z muldefs
-fvirtual-function-elimination -fvisibility=hidden -DSPEC_OPENMP
-fopenmp=libomp -lomp -lamdlibm -ljemalloc -lflang
```

Fortran benchmarks:

```
-m64 -Wl,-mllvm -Wl,-inline-recursion=4
-Wl,-mllvm -Wl,-lsr-in-nested-loop -Wl,-mllvm -Wl,-enable-iv-split
-Wl,-mllvm -Wl,-region-vectorize -Wl,-mllvm -Wl,-function-specialize
-Wl,-mllvm -Wl,-align-all-nofallthru-blocks=6
-Wl,-mllvm -Wl,-reduce-array-computations=3 -O3 -march=znver3
-fveclib=AMDLIBM -ffast-math -fopenmp -flto -z muldefs
-mllvm -unroll-aggressive -mllvm -unroll-threshold=150 -DSPEC_OPENMP
-fopenmp=libomp -lomp -lamdlibm -ljemalloc -lflang
```

Base Other Flags

C benchmarks:

```
-Wno-unused-command-line-argument -Wno-return-type
```

C++ benchmarks:

```
-Wno-unused-command-line-argument -Wno-return-type
```

(Continued on next page)

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Base Other Flags (Continued)

Fortran benchmarks:
```
-Wno-return-type
```

Peak Compiler Invocation

C benchmarks:
```
clang
```

C++ benchmarks:
```
clang++
```

Fortran benchmarks:
```
flang
```

Peak Portability Flags

```
Same as Base Portability Flags
```

Peak Optimization Flags

C benchmarks:

```
600.perlbench_s: -m64 -Wl,-allow-multiple-definition
-Wl,-mllvm -Wl,-enable-licm-vrp
-Wl,-mllvm -Wl,-function-specialize
-Wl,-mllvm -Wl,-align-all-nofallthru-blocks=6
-Wl,-mllvm -Wl,-reduce-array-computations=3 -Ofast
-march=znver3 -fveclib=AMDLIBM -ffast-math -fopenmp
-flto -fstruct-layout=5 -mllvm -unroll-threshold=50
-fremap-arrays -flv-function-specialization
-mllvm -inline-threshold=1000 -mllvm -enable-gvn-hoist
-mllvm -global-vectorize-slp=true
-mllvm -function-specialize -mllvm -enable-licm-vrp
-mllvm -reduce-array-computations=3 -DSPEC_OPENMP
-fopenmp=libomp -lomp -lamdlibm -ljemalloc -lflang
```

```
602.gcc_s: Same as 600.perlbench_s
```

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Tested by: Cisco Systems

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Hardware Availability: Aug-2021
Software Availability: Dec-2021

Peak Optimization Flags (Continued)

605.mcf_s: `Same as 600.perlbench_s`

625.x264_s: `-m64 -Wl,-allow-multiple-definition`
`-Wl,-mllvm -Wl,-enable-licm-vrp`
`-Wl,-mllvm -Wl,-do-block-reorder=aggressive`
`-Wl,-mllvm -Wl,-region-vectorize`
`-Wl,-mllvm -Wl,-function-specialize`
`-Wl,-mllvm -Wl,-align-all-nofallthru-blocks=6`
`-Wl,-mllvm -Wl,-reduce-array-computations=3 -Ofast`
`-march=znver3 -fveclib=AMDLIBM -ffast-math -fopenmp`
`-flto -fstruct-layout=5 -mllvm -unroll-threshold=50`
`-mllvm -inline-threshold=1000 -fremap-arrays`
`-mllvm -function-specialize -flv-function-specialization`
`-mllvm -enable-gvn-hoist -mllvm -global-vectorize-slp=true`
`-mllvm -enable-licm-vrp -mllvm -reduce-array-computations=3`
`-mllvm -do-block-reorder=aggressive -DSPEC_OPENMP`
`-fopenmp=libomp -lomp -lamdlibm -ljemalloc -lflang`

657.xz_s: `Same as 625.x264_s`

C++ benchmarks:

620.omnetpp_s: `-m64 -Wl,-mllvm -Wl,-function-specialize`
`-Wl,-mllvm -Wl,-align-all-nofallthru-blocks=6`
`-Wl,-mllvm -Wl,-reduce-array-computations=3 -Ofast`
`-march=znver3 -fveclib=AMDLIBM -ffast-math -fopenmp`
`-flto -finline-aggressive -mllvm -unroll-threshold=100`
`-flv-function-specialization -mllvm -enable-licm-vrp`
`-mllvm -reroll-loops -mllvm -aggressive-loop-unswitch`
`-mllvm -reduce-array-computations=3`
`-mllvm -global-vectorize-slp=true`
`-fvirtual-function-elimination -fvisibility=hidden`
`-DSPEC_OPENMP -fopenmp=libomp -lomp -lamdlibm -ljemalloc`
`-lflang`

623.xalancbmk_s: `-m64 -Wl,-mllvm -Wl,-function-specialize`
`-Wl,-mllvm -Wl,-align-all-nofallthru-blocks=6`
`-Wl,-mllvm -Wl,-reduce-array-computations=3`
`-Wl,-mllvm -Wl,-do-block-reorder=aggressive -Ofast`
`-march=znver3 -fveclib=AMDLIBM -ffast-math -fopenmp`
`-flto -finline-aggressive -mllvm -unroll-threshold=100`
`-flv-function-specialization -mllvm -enable-licm-vrp`
`-mllvm -reroll-loops -mllvm -aggressive-loop-unswitch`
`-mllvm -reduce-array-computations=3`
`-mllvm -global-vectorize-slp=true`
`-mllvm -do-block-reorder=aggressive`

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Peak Optimization Flags (Continued)

623.xalancbmk_s (continued):
```
-fvirtual-function-elimination -fvisibility=hidden
-DSPEC_OPENMP -fopenmp=libomp -lomp -lamdlibm -ljemalloc
-lflang
```

631.deepsjeng_s: `-m64 -Wl,-mllvm -Wl,-do-block-reorder=aggressive`
```
-Wl,-mllvm -Wl,-region-vectorize
-Wl,-mllvm -Wl,-function-specialize
-Wl,-mllvm -Wl,-align-all-nofallthru-blocks=6
-Wl,-mllvm -Wl,-reduce-array-computations=3 -O3
-march=znver3 -fveclib=AMDLIBM -ffast-math -fopenmp
-flto -mllvm -enable-partial-unswitch
-mllvm -unroll-threshold=100 -finline-aggressive
-flv-function-specialization
-mllvm -loop-unswitch-threshold=200000 -mllvm -reroll-loops
-mllvm -aggressive-loop-unswitch
-mllvm -extra-vectorizer-passes
-mllvm -reduce-array-computations=3
-mllvm -global-vectorize-slp=true
-mllvm -convert-pow-exp-to-int=false
-mllvm -do-block-reorder=aggressive
-fvirtual-function-elimination -fvisibility=hidden
-DSPEC_OPENMP -fopenmp=libomp -lomp -lamdlibm -ljemalloc
-lflang
```

641.leela_s: `basepeak = yes`

Fortran benchmarks:

648.exchange2_s: `basepeak = yes`

Peak Other Flags

C benchmarks:
```
-Wno-unused-command-line-argument -Wno-return-type
```

C++ benchmarks:
```
-Wno-unused-command-line-argument -Wno-return-type
```

Fortran benchmarks:
```
-Wno-return-type
```

SPEC CPU®2017 Integer Speed Result

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The flags files that were used to format this result can be browsed at

http://www.spec.org/cpu2017/flags/aocc320-flags-A1.html
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-AMD-v2-revD.html

You can also download the XML flags sources by saving the following links:

http://www.spec.org/cpu2017/flags/aocc320-flags-A1.xml
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-AMD-v2-revD.xml

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