SPEC CPU®2017 Floating Point Rate Result

Copyright 2017-2022 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS X210c M6 (Intel Xeon Gold 5320T, 2.30GHz)

SPECrate®2017_fp_base = 301

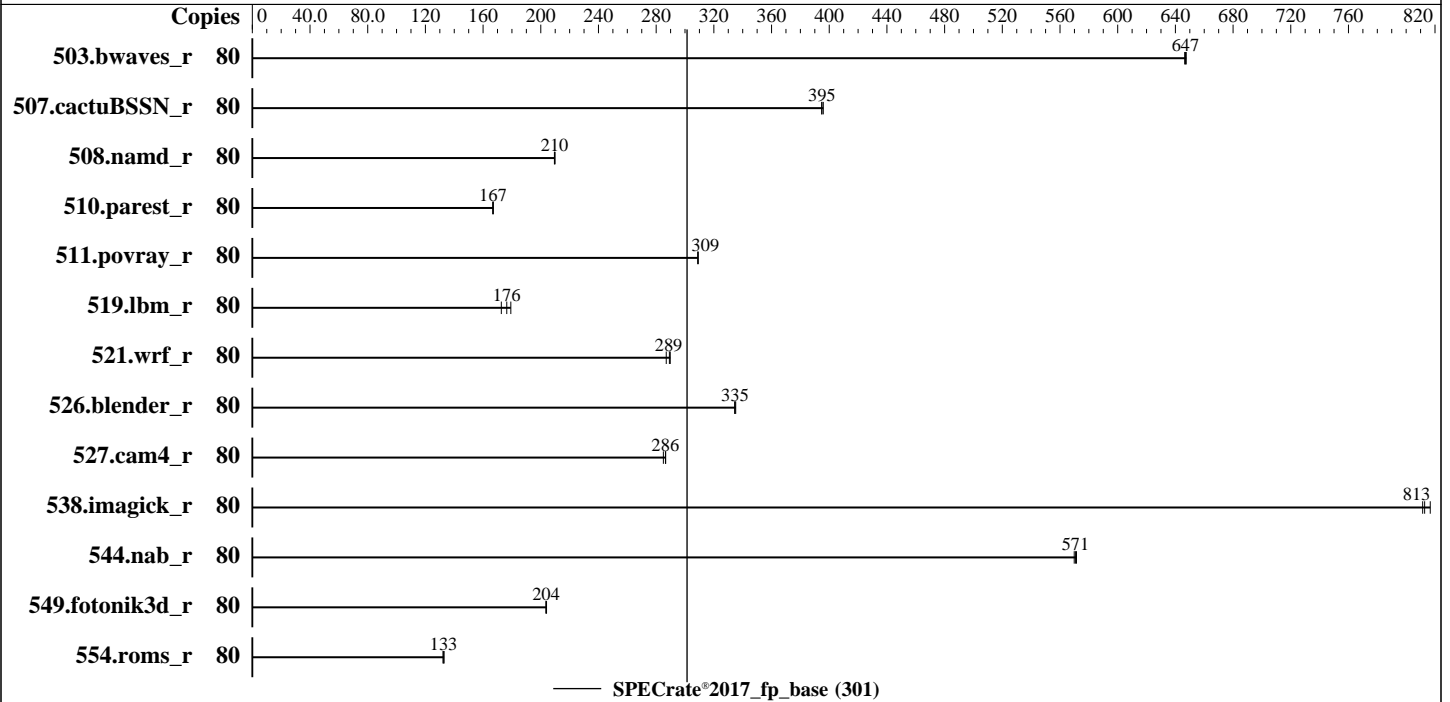SPECrate®2017_fp_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Dec-2021
Hardware Availability: Sep-2021
Software Availability: Sep-2021

Benchmark	Copies	Result
503.bwaves_r	80	647
507.cactuBSSN_r	80	395
508.namd_r	80	210
510.parest_r	80	167
511.povray_r	80	309
519.lbm_r	80	176
521.wrf_r	80	289
526.blender_r	80	335
527.cam4_r	80	286
538.imagick_r	80	813
544.nab_r	80	571
549.fotonik3d_r	80	204
554.roms_r	80	133

SPECrate®2017_fp_base (301)

Hardware

CPU Name: Intel Xeon Gold 5320T
 Max MHz: 3500
 Nominal: 2300
Enabled: 40 cores, 2 chips, 2 threads/core
Orderable: 1,2 Chips
Cache L1: 32 KB I + 48 KB D on chip per core
 L2: 1.25 MB I+D on chip per core
 L3: 30 MB I+D on chip per chip
 Other: None
Memory: 2 TB (32 x 64 GB 2Rx4 PC4-3200AA-R, running at 2933)
Storage: 1 x 240 GB M.2 SSD SATA
Other: None

Software

OS: SUSE Linux Enterprise Server 15 SP3
 5.3.18-57-default
Compiler: C/C++: Version 2021.4.0 of Intel oneAPI DPC++/C++ Compiler Build 20210924 for Linux;
 Fortran: Version 2021.4.0 of Intel Fortran Compiler
 Classic Build 20210910 for Linux;
Parallel: No
Firmware: Version 5.0.1d released Aug-2021
File System: xfs
System State: Run level 3 (multi-user)
Base Pointers: 64-bit
Peak Pointers: Not Applicable
Other: jemalloc memory allocator V5.0.1
Power Management: BIOS and OS set to prefer performance at the cost of additional power usage

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Results Table

Benchmark	Base							Peak						
	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
503.bwaves_r	80	1239	648	**1240**	**647**	1241	646							
507.cactuBSSN_r	80	**256**	**395**	256	396	257	395							
508.namd_r	80	362	210	**363**	**210**	363	209							
510.parest_r	80	1253	167	1256	167	**1254**	**167**							
511.povray_r	80	605	309	**605**	**309**	604	309							
519.lbm_r	80	**478**	**176**	488	173	470	179							
521.wrf_r	80	**620**	**289**	618	290	624	287							
526.blender_r	80	364	335	**364**	**335**	364	334							
527.cam4_r	80	488	287	491	285	**488**	**286**							
538.imagick_r	80	245	811	244	817	**245**	**813**							
544.nab_r	80	236	571	236	570	**236**	**571**							
549.fotonik3d_r	80	1532	204	**1530**	**204**	1528	204							
554.roms_r	80	**958**	**133**	956	133	962	132							

SPECrate®2017_fp_base =   301

SPECrate®2017_fp_peak =   Not Run

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

Environment Variables Notes

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-64"
MALLOC_CONF = "retain:true"

General Notes

Binaries compiled on a system with 1x Intel Core i9-7940X CPU + 64GB RAM
memory using openSUSE Leap 15.2
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:

(Continued on next page)

Standard Performance Evaluation Corporation (info@spec.org)
https://www.spec.org/

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General Notes (Continued)

```
 sync; echo 3>        /proc/sys/vm/drop_caches
 runcpu command invoked through numactl i.e.:
 numactl --interleave=all runcpu <etc>
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2)
is mitigated in the system as tested and documented.
 jemalloc, a general purpose malloc implementation
 built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5
 sources available from jemalloc.net or https://github.com/jemalloc/jemalloc/releases
```

Platform Notes

```
BIOS Settings:
Adjacent Cache Line Prefetcher set to Disabled
DCU Streamer Prefetch set to Disabled
Sub NUMA Clustering set to Enabled
LLC Dead Line set to Disabled
Memory Refresh Rate set to 1x Refresh
ADDDC Sparing set to Disabled
Patrol Scrub set to Disabled
Processor C6 Report set to Enabled

 Sysinfo program /home/cpu2017/bin/sysinfo
 Rev: r6622 of 2021-04-07 982a61ec0915b55891ef0e16acafc64d
 running on perf-blade1 Wed Dec  8 05:06:14 2021

 SUT (System Under Test) info as seen by some common utilities.
 For more information on this section, see
    https://www.spec.org/cpu2017/Docs/config.html#sysinfo

 From /proc/cpuinfo
    model name : Intel(R) Xeon(R) Gold 5320T CPU @ 2.30GHz
       2  "physical id"s (chips)
       80 "processors"
    cores, siblings (Caution: counting these is hw and system dependent. The following
    excerpts from /proc/cpuinfo might not be reliable.  Use with caution.)
       cpu cores : 20
       siblings  : 40
       physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19
       physical 1: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19

 From lscpu from util-linux 2.36.2:
     Architecture:                x86_64
```

(Continued on next page)

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Platform Notes (Continued)

```
        CPU op-mode(s):                 32-bit, 64-bit
        Byte Order:                     Little Endian
        Address sizes:                  46 bits physical, 57 bits virtual
        CPU(s):                         80
        On-line CPU(s) list:            0-79
        Thread(s) per core:             2
        Core(s) per socket:             20
        Socket(s):                      2
        NUMA node(s):                   4
        Vendor ID:                      GenuineIntel
        CPU family:                     6
        Model:                          106
        Model name:                     Intel(R) Xeon(R) Gold 5320T CPU @ 2.30GHz
        Stepping:                       6
        CPU MHz:                        1505.919
        CPU max MHz:                    3500.0000
        CPU min MHz:                    800.0000
        BogoMIPS:                       4600.00
        Virtualization:                 VT-x
        L1d cache:                      1.9 MiB
        L1i cache:                      1.3 MiB
        L2 cache:                       50 MiB
        L3 cache:                       60 MiB
        NUMA node0 CPU(s):              0-9,40-49
        NUMA node1 CPU(s):              10-19,50-59
        NUMA node2 CPU(s):              20-29,60-69
        NUMA node3 CPU(s):              30-39,70-79
        Vulnerability Itlb multihit:    Not affected
        Vulnerability L1tf:             Not affected
        Vulnerability Mds:              Not affected
        Vulnerability Meltdown:         Not affected
        Vulnerability Spec store bypass: Mitigation; Speculative Store Bypass disabled via
        prctl and seccomp
        Vulnerability Spectre v1:       Mitigation; usercopy/swapgs barriers and __user
        pointer sanitization
        Vulnerability Spectre v2:       Mitigation; Enhanced IBRS, IBPB conditional, RSB
        filling
        Vulnerability Srbds:            Not affected
        Vulnerability Tsx async abort:  Not affected
        Flags:                          fpu vme de pse tsc msr pae mce cx8 apic sep mtrr
        pge mca cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx
        pdpe1gb rdtscp lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology
        nonstop_tsc cpuid aperfmperf pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2
        ssse3 sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt
        tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault
        epb cat_l3 invpcid_single ssbd mba ibrs ibpb stibp ibrs_enhanced tpr_shadow vnmi
        flexpriority ept vpid ept_ad fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms
```

(Continued on next page)

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CPU2017 License:	9019	**Test Date:**	Dec-2021
Test Sponsor:	Cisco Systems	**Hardware Availability:**	Sep-2021
Tested by:	Cisco Systems	**Software Availability:**	Sep-2021

Platform Notes (Continued)

```
    invpcid rtm cqm rdt_a avx512f avx512dq rdseed adx smap avx512ifma clflushopt clwb
    intel_pt avx512cd sha_ni avx512bw avx512vl xsaveopt xsavec xgetbv1 xsaves cqm_llc
    cqm_occup_llc cqm_mbm_total cqm_mbm_local split_lock_detect wbnoinvd dtherm ida arat
    pln pts hwp hwp_act_window hwp_epp hwp_pkg_req avx512vbmi umip pku ospke
    avx512_vbmi2 gfni vaes vpclmulqdq avx512_vnni avx512_bitalg tme avx512_vpopcntdq
    la57 rdpid fsrm md_clear pconfig flush_l1d arch_capabilities

  From lscpu --cache:
      NAME ONE-SIZE ALL-SIZE WAYS TYPE           LEVEL   SETS PHY-LINE COHERENCY-SIZE
      L1d        48K     1.9M  12 Data            1     64       1             64
      L1i        32K     1.3M   8 Instruction     1     64       1             64
      L2        1.3M      50M  20 Unified         2   1024       1             64
      L3         30M      60M  12 Unified         3  40960       1             64


  /proc/cpuinfo cache data
     cache size : 30720 KB


  From numactl --hardware
  WARNING: a numactl 'node' might or might not correspond to a physical chip.
    available: 4 nodes (0-3)
    node 0 cpus: 0 1 2 3 4 5 6 7 8 9 40 41 42 43 44 45 46 47 48 49
    node 0 size: 515684 MB
    node 0 free: 515039 MB
    node 1 cpus: 10 11 12 13 14 15 16 17 18 19 50 51 52 53 54 55 56 57 58 59
    node 1 size: 516090 MB
    node 1 free: 515521 MB
    node 2 cpus: 20 21 22 23 24 25 26 27 28 29 60 61 62 63 64 65 66 67 68 69
    node 2 size: 516056 MB
    node 2 free: 515359 MB
    node 3 cpus: 30 31 32 33 34 35 36 37 38 39 70 71 72 73 74 75 76 77 78 79
    node 3 size: 516087 MB
    node 3 free: 515451 MB
    node distances:
    node   0   1   2   3
      0:  10  11  20  20
      1:  11  10  20  20
      2:  20  20  10  11
      3:  20  20  11  10

  From /proc/meminfo
     MemTotal:       2113453632 kB
     HugePages_Total:        0
     Hugepagesize:        2048 kB


  /sys/devices/system/cpu/cpu*/cpufreq/scaling_governor has
     performance
```

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Platform Notes (Continued)

```
From /etc/*release* /etc/*version*
   os-release:
      NAME="SLES"
      VERSION="15-SP3"
      VERSION_ID="15.3"
      PRETTY_NAME="SUSE Linux Enterprise Server 15 SP3"
      ID="sles"
      ID_LIKE="suse"
      ANSI_COLOR="0;32"
      CPE_NAME="cpe:/o:suse:sles:15:sp3"

uname -a:
   Linux perf-blade1 5.3.18-57-default #1 SMP Wed Apr 28 10:54:41 UTC 2021 (ba3c2e9)
   x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2018-12207 (iTLB Multihit):                   Not affected
CVE-2018-3620 (L1 Terminal Fault):                Not affected
Microarchitectural Data Sampling:                 Not affected
CVE-2017-5754 (Meltdown):                         Not affected
CVE-2018-3639 (Speculative Store Bypass):         Mitigation: Speculative Store
                                                  Bypass disabled via prctl and
                                                  seccomp
CVE-2017-5753 (Spectre variant 1):                Mitigation: usercopy/swapgs
                                                  barriers and __user pointer
                                                  sanitization
CVE-2017-5715 (Spectre variant 2):                Mitigation: Enhanced IBRS, IBPB:
                                                  conditional, RSB filling
CVE-2020-0543 (Special Register Buffer Data Sampling): Not affected
CVE-2019-11135 (TSX Asynchronous Abort):          Not affected

run-level 3 Dec 7 21:30

SPEC is set to: /home/cpu2017
   Filesystem      Type  Size  Used Avail Use% Mounted on
   /dev/sda3       xfs   181G   54G  128G  30% /home

From /sys/devices/virtual/dmi/id
    Vendor:         Cisco Systems Inc
    Product:        UCSX-210C-M6
    Serial:         FCH25057AMV

Additional information from dmidecode 3.2 follows.  WARNING: Use caution when you
interpret this section. The 'dmidecode' program reads system data which is "intended to
allow hardware to be accurately determined", but the intent may not be met, as there are
frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
```

(Continued on next page)

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Platform Notes (Continued)

```
    Memory:
      32x 0xCE00 M393A8G40AB2-CWE 64 GB 2 rank 3200, configured at 2933

  BIOS:
     BIOS Vendor:        Cisco Systems, Inc.
     BIOS Version:       X210M6.5.0.1d.0.0816211754
     BIOS Date:          08/16/2021
     BIOS Revision:      5.22

  (End of data from sysinfo program)
```

Compiler Version Notes

```
==============================================================================
C                   | 519.lbm_r(base) 538.imagick_r(base) 544.nab_r(base)
------------------------------------------------------------------------------
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
  Version 2021.4.0 Build 20210924
Copyright (C) 1985-2021 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------


==============================================================================
C++                 | 508.namd_r(base) 510.parest_r(base)
------------------------------------------------------------------------------
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
  Version 2021.4.0 Build 20210924
Copyright (C) 1985-2021 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------


==============================================================================
C++, C              | 511.povray_r(base) 526.blender_r(base)
------------------------------------------------------------------------------
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
  Version 2021.4.0 Build 20210924
Copyright (C) 1985-2021 Intel Corporation. All rights reserved.
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
  Version 2021.4.0 Build 20210924
Copyright (C) 1985-2021 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------


==============================================================================
C++, C, Fortran | 507.cactuBSSN_r(base)
------------------------------------------------------------------------------
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
  Version 2021.4.0 Build 20210924
Copyright (C) 1985-2021 Intel Corporation. All rights reserved.
```

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Compiler Version Notes (Continued)

```
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
  Version 2021.4.0 Build 20210924
Copyright (C) 1985-2021 Intel Corporation. All rights reserved.
Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on
  Intel(R) 64, Version 2021.4.0 Build 20210910_000000
Copyright (C) 1985-2021 Intel Corporation.  All rights reserved.
------------------------------------------------------------------------------


==============================================================================
Fortran         | 503.bwaves_r(base) 549.fotonik3d_r(base) 554.roms_r(base)
------------------------------------------------------------------------------
Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on
  Intel(R) 64, Version 2021.4.0 Build 20210910_000000
Copyright (C) 1985-2021 Intel Corporation.  All rights reserved.
------------------------------------------------------------------------------


==============================================================================
Fortran, C      | 521.wrf_r(base) 527.cam4_r(base)
------------------------------------------------------------------------------
Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on
  Intel(R) 64, Version 2021.4.0 Build 20210910_000000
Copyright (C) 1985-2021 Intel Corporation.  All rights reserved.
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
  Version 2021.4.0 Build 20210924
Copyright (C) 1985-2021 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------
```

Base Compiler Invocation

C benchmarks:
icx

C++ benchmarks:
icpx

Fortran benchmarks:
ifort

Benchmarks using both Fortran and C:
ifort icx

Benchmarks using both C and C++:
icpx icx

Benchmarks using Fortran, C, and C++:
icpx icx ifort

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Base Portability Flags

503.bwaves_r: `-DSPEC_LP64`
507.cactuBSSN_r: `-DSPEC_LP64`
508.namd_r: `-DSPEC_LP64`
510.parest_r: `-DSPEC_LP64`
511.povray_r: `-DSPEC_LP64`
519.lbm_r: `-DSPEC_LP64`
521.wrf_r: `-DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian`
526.blender_r: `-DSPEC_LP64 -DSPEC_LINUX -funsigned-char`
527.cam4_r: `-DSPEC_LP64 -DSPEC_CASE_FLAG`
538.imagick_r: `-DSPEC_LP64`
544.nab_r: `-DSPEC_LP64`
549.fotonik3d_r: `-DSPEC_LP64`
554.roms_r: `-DSPEC_LP64`

Base Optimization Flags

C benchmarks:
`-w -std=c11 -m64 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math -flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4 -mbranches-within-32B-boundaries -ljemalloc -L/home/cpu2017/je5.0.1-64`

C++ benchmarks:
`-w -m64 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math -flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4 -mbranches-within-32B-boundaries -ljemalloc -L/home/cpu2017/je5.0.1-64`

Fortran benchmarks:
`-w -m64 -Wl,-z,muldefs -xCORE-AVX512 -O3 -ipo -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-multiple-gather-scatter-by-shuffles -qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte -mbranches-within-32B-boundaries -ljemalloc -L/home/cpu2017/je5.0.1-64`

Benchmarks using both Fortran and C:
`-w -m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math -flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4 -O3 -ipo -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-multiple-gather-scatter-by-shuffles -mbranches-within-32B-boundaries -nostandard-realloc-lhs -align array32byte -ljemalloc -L/home/cpu2017/je5.0.1-64`

Benchmarks using both C and C++:
`-w -m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math -flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4`

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Base Optimization Flags (Continued)

Benchmarks using both C and C++ (continued):
```
-mbranches-within-32B-boundaries -ljemalloc -L/home/cpu2017/je5.0.1-64
```

Benchmarks using Fortran, C, and C++:
```
-w -m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4 -O3
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles
-mbranches-within-32B-boundaries -nostandard-realloc-lhs
-align array32byte -ljemalloc -L/home/cpu2017/je5.0.1-64
```

The flags files that were used to format this result can be browsed at
```
http://www.spec.org/cpu2017/flags/Intel-ic2021-official-linux64_revA.2021-12-22.html
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.0-ICX-revJ.html
```

You can also download the XML flags sources by saving the following links:
```
http://www.spec.org/cpu2017/flags/Intel-ic2021-official-linux64_revA.2021-12-22.xml
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.0-ICX-revJ.xml
```

For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.1.8 on 2021-12-08 08:06:13-0500.
Report generated on 2022-01-05 13:31:46 by CPU2017 PDF formatter v6442.
Originally published on 2022-01-04.