



SPEC CPU®2017 Floating Point Rate Result

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Tyrone Systems

(Test Sponsor: Netweb Pte Ltd)

Tyrone Camarero DS400E1U-224R4
(2.10 GHz, Intel Xeon Gold 6252)

SPECrate®2017_fp_base = 241

SPECrate®2017_fp_peak = 244

CPU2017 License: 006042

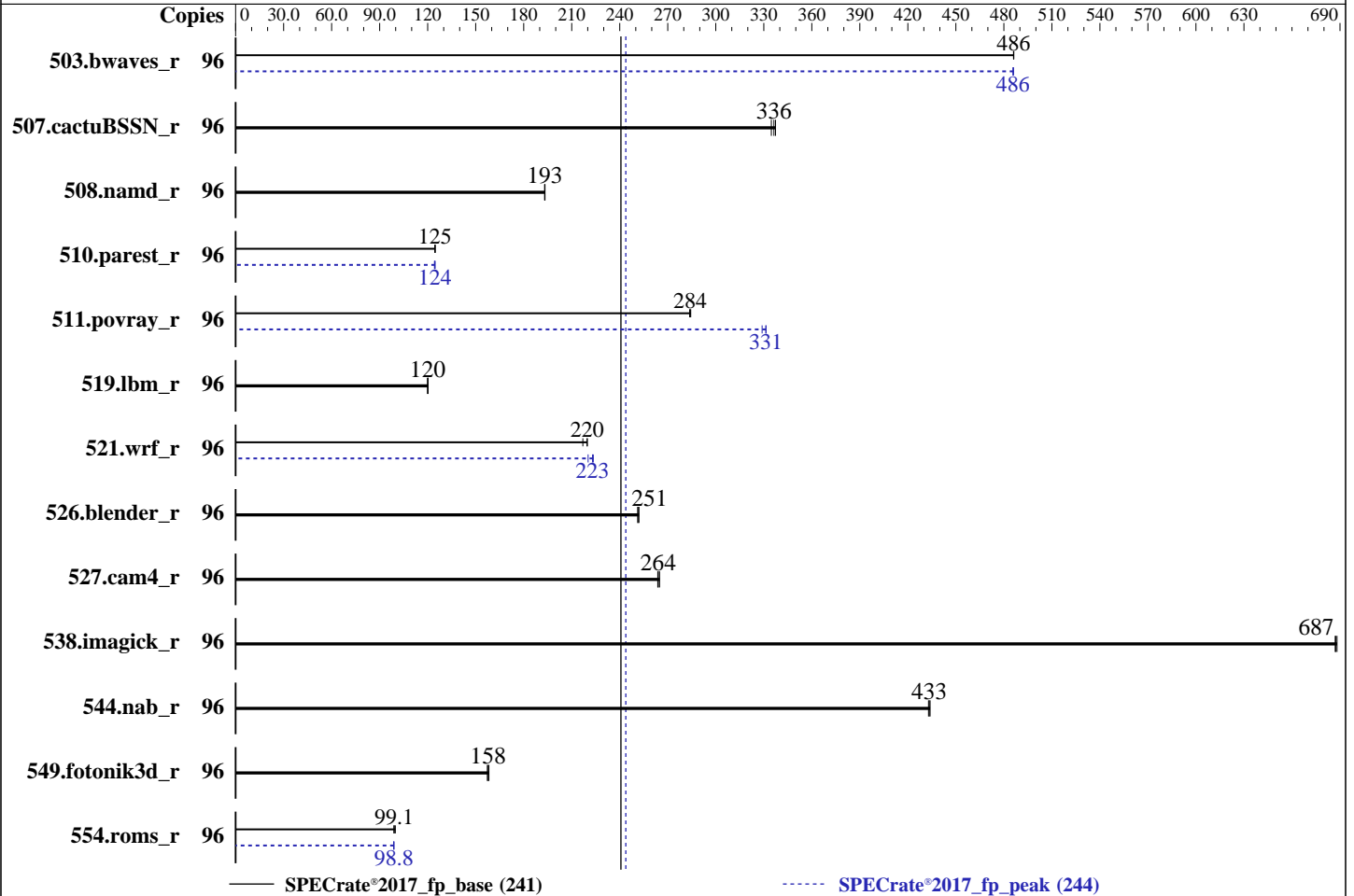
Test Sponsor: Netweb Pte Ltd

Tested by: Tyrone Systems

Test Date: Feb-2021

Hardware Availability: Aug-2020

Software Availability: Dec-2020



Hardware

CPU Name: Intel Xeon Gold 6252
 Max MHz: 3700
 Nominal: 2100
 Enabled: 48 cores, 2 chips, 2 threads/core
 Orderable: 1,2 (chip)s
 Cache L1: 32 KB I + 32 KB D on chip per core
 L2: 1 MB I+D on chip per core
 L3: 35.75 MB I+D on chip per chip
 Other: None
 Memory: 384 GB (12 x 32 GB 2Rx4 PC4-2933Y-R)
 Storage: 1 x 480 GB SATA SSD
 Other: None

Software

OS: CentOS Linux release 8.3.2011
 4.18.0-240.el8.x86_64
 Compiler: C/C++: Version 19.1.1.217 of Intel C/C++
 Compiler Build 20200306 for Linux;
 Fortran: Version 19.1.1.217 of Intel Fortran
 Compiler Build 20200306 for Linux
 Parallel: No
 Firmware: Version 3.4 released Oct-2020
 File System: xfs
 System State: Run level 3 (multi-user)
 Base Pointers: 64-bit
 Peak Pointers: 64-bit
 Other: jemalloc memory allocator V5.0.1
 Power Management: BIOS set to prefer performance at
 the cost of additional power usage



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Results Table

Benchmark	Base							Peak						
	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
503.bwaves_r	96	1980	486	1980	486	1981	486	96	1981	486	1982	486	1982	486
507.cactuBSSN_r	96	360	337	363	335	361	336	96	360	337	363	335	361	336
508.namd_r	96	472	193	472	193	472	193	96	472	193	472	193	472	193
510.parest_r	96	2015	125	2014	125	2017	124	96	2018	124	2015	125	2022	124
511.povray_r	96	789	284	788	284	790	284	96	676	331	677	331	681	329
519.lbm_r	96	842	120	843	120	844	120	96	842	120	843	120	844	120
521.wrf_r	96	979	220	991	217	979	220	96	962	223	976	220	964	223
526.blender_r	96	582	251	580	252	582	251	96	582	251	580	252	582	251
527.cam4_r	96	637	264	634	265	636	264	96	637	264	634	265	636	264
538.imagick_r	96	347	688	348	687	347	687	96	347	688	348	687	347	687
544.nab_r	96	372	434	373	433	373	433	96	372	434	373	433	373	433
549.fotonik3d_r	96	2364	158	2379	157	2371	158	96	2364	158	2379	157	2371	158
554.roms_r	96	1529	99.8	1539	99.1	1543	98.9	96	1543	98.9	1544	98.8	1544	98.8

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Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Compiler Notes

The inconsistent Compiler version information under Compiler Version section is due to a discrepancy in Intel Compiler.

The correct version of C/C++ compiler is: Version 19.1.1.217 Build 20200306 Compiler for Linux

The correct version of Fortran compiler is: Version 19.1.1.217 Build 20200306 Compiler for Linux

Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

Environment Variables Notes

Environment variables set by runcpu before the start of the run:

LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-64"

MALLOC_CONF = "retain:true"



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General Notes

Binaries compiled on a system with 2x Intel Cascade Lake CPU 4214R + 384 GB RAM memory using Centos 8.2 x86_64

Transparent Huge Pages enabled by default

Prior to runcpu invocation

Filesystem page cache synced and cleared with:

```
sync; echo 3> /proc/sys/vm/drop_caches
```

runcpu command invoked through numactl i.e.:

```
numactl --interleave=all runcpu <etc>
```

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

jemalloc, a general purpose malloc implementation

built with the Centos 8.2 x86_64, and the system compiler gcc 4.8.5

sources available from jemalloc.net or <https://github.com/jemalloc/jemalloc/releases>

Platform Notes

BIOS Settings:

Power Technology = Custom

Power Performance Tuning = BIOS Controls EPB

ENERGY_PERF_BIAS_CFG mode = Extreme Performance

SNC = Enable

Stale AtoS = Disable

IMC Interleaving = 1-way Interleave

Patrol Scrub = Disable

Sysinfo program /home/cpu2017/bin/sysinfo

Rev: r6538 of 2020-09-24 e8664e66d2d7080afeaa89d4b38e2f1c

running on spec Tue Feb 16 20:59:25 2021

SUT (System Under Test) info as seen by some common utilities.

For more information on this section, see

<https://www.spec.org/cpu2017/Docs/config.html#sysinfo>

From /proc/cpuinfo

```
model name : Intel(R) Xeon(R) Gold 6252 CPU @ 2.10GHz
```

```
2 "physical id"s (chips)
```

```
96 "processors"
```

cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)

```
cpu cores : 24
```

```
siblings : 48
```

```
physical 0: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 16 17 18 19 20 21 25 26 27 28 29
```

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Platform Notes (Continued)

physical 1: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 16 17 18 19 20 21 25 26 27 28 29

From lscpu:

```

Architecture:          x86_64
CPU op-mode(s):        32-bit, 64-bit
Byte Order:             Little Endian
CPU(s):                 96
On-line CPU(s) list:   0-95
Thread(s) per core:    2
Core(s) per socket:    24
Socket(s):              2
NUMA node(s):          2
Vendor ID:              GenuineIntel
CPU family:             6
Model:                  85
Model name:             Intel(R) Xeon(R) Gold 6252 CPU @ 2.10GHz
Stepping:               7
CPU MHz:                1475.327
CPU max MHz:            3700.0000
CPU min MHz:            1000.0000
BogoMIPS:               4200.00
Virtualization:         VT-x
L1d cache:              32K
L1i cache:              32K
L2 cache:               1024K
L3 cache:               36608K
NUMA node0 CPU(s):     0-23,48-71
NUMA node1 CPU(s):     24-47,72-95

```

```

Flags:                  fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpeltb rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
aperfperf pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16
xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave
avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_l3 cdp_l3
invpcid_single intel_ppin ssbd mba ibrs ibpb stibp ibrs_enhanced tpr_shadow vnmi
flexpriority ept vpid ept_ad fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms
invpcid cqm mpx rdt_a avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt
avx512cd avx512bw avx512vl xsaveopt xsavec xgetbv1 xsaves cqm_llc cqm_occup_llc
cqm_mbm_total cqm_mbm_local dtherm ida arat pln pts pku ospke avx512_vnni md_clear
flush_lld arch_capabilities

```

```

/proc/cpuinfo cache data
cache size : 36608 KB

```

```

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a
physical chip.
available: 2 nodes (0-1)

```

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Platform Notes (Continued)

```
node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 48 49 50 51
52 53 54 55 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 71
```

```
node 0 size: 177651 MB
```

```
node 0 free: 169790 MB
```

```
node 1 cpus: 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 72
73 74 75 76 77 78 79 80 81 82 83 84 85 86 87 88 89 90 91 92 93 94 95
```

```
node 1 size: 180636 MB
```

```
node 1 free: 173085 MB
```

```
node distances:
```

```
node 0 1
```

```
0: 10 21
```

```
1: 21 10
```

```
From /proc/meminfo
```

```
MemTotal: 394855904 kB
```

```
HugePages_Total: 0
```

```
Hugepagesize: 2048 kB
```

```
/sbin/tuned-adm active
```

```
Current active profile: throughput-performance
```

```
/sys/devices/system/cpu/cpu*/cpufreq/scaling_governor has
performance
```

```
From /etc/*release* /etc/*version*
```

```
centos-release: CentOS Linux release 8.3.2011
```

```
centos-release-upstream: Derived from Red Hat Enterprise Linux 8.3
```

```
os-release:
```

```
NAME="CentOS Linux"
```

```
VERSION="8"
```

```
ID="centos"
```

```
ID_LIKE="rhel fedora"
```

```
VERSION_ID="8"
```

```
PLATFORM_ID="platform:el8"
```

```
PRETTY_NAME="CentOS Linux 8"
```

```
ANSI_COLOR="0;31"
```

```
redhat-release: CentOS Linux release 8.3.2011
```

```
system-release: CentOS Linux release 8.3.2011
```

```
system-release-cpe: cpe:/o:centos:centos:8
```

```
uname -a:
```

```
Linux spec 4.18.0-240.el8.x86_64 #1 SMP Fri Sep 25 19:48:47 UTC 2020 x86_64 x86_64
x86_64 GNU/Linux
```

```
Kernel self-reported vulnerability status:
```

```
CVE-2018-12207 (iTLB Multihit):
```

```
KVM: Mitigation: Split huge pages
```

(Continued on next page)



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Platform Notes (Continued)

CVE-2018-3620 (L1 Terminal Fault):	Not affected
Microarchitectural Data Sampling:	Not affected
CVE-2017-5754 (Meltdown):	Not affected
CVE-2018-3639 (Speculative Store Bypass):	Mitigation: Speculative Store Bypass disabled via prctl and seccomp
CVE-2017-5753 (Spectre variant 1):	Mitigation: usercopy/swapgs barriers and __user pointer sanitization
CVE-2017-5715 (Spectre variant 2):	Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling
CVE-2020-0543 (Special Register Buffer Data Sampling):	Not affected
CVE-2019-11135 (TSX Asynchronous Abort):	Mitigation: TSX disabled

run-level 3 Feb 16 11:45

SPEC is set to: /home/cpu2017

Filesystem	Type	Size	Used	Avail	Use%	Mounted on
/dev/mapper/cl-home	xfs	372G	154G	218G	42%	/home

From /sys/devices/virtual/dmi/id

Vendor:	Tyrone Systems
Product:	Tyrone Camarero DS400E1
Serial:	S263875X9527668

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

Memory:

12x NO DIMM NO DIMM
12x Samsung M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2934

BIOS:

BIOS Vendor:	American Megatrends Inc.
BIOS Version:	3.4
BIOS Date:	10/30/2020
BIOS Revision:	5.14

(End of data from sysinfo program)

Compiler Version Notes

```
=====
C          | 519.lbm_r(base, peak) 538.imagick_r(base, peak)
          | 544.nab_r(base, peak)
```

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Compiler Version Notes (Continued)

Intel(R) C Compiler for applications running on Intel(R) 64, Version 2021.1
NextGen Build 20200304
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

=====
C++ | 508.namd_r(base, peak) 510.parest_r(base, peak)

Intel(R) C++ Compiler for applications running on Intel(R) 64, Version 2021.1
NextGen Build 20200304
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

=====
C++, C | 511.povray_r(base) 526.blender_r(base, peak)

Intel(R) C++ Compiler for applications running on Intel(R) 64, Version 2021.1
NextGen Build 20200304
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Intel(R) C Compiler for applications running on Intel(R) 64, Version 2021.1
NextGen Build 20200304
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

=====
C++, C | 511.povray_r(peak)

Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.1.1.217 Build 20200306
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.1.1.217 Build 20200306
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

=====
C++, C | 511.povray_r(base) 526.blender_r(base, peak)

Intel(R) C++ Compiler for applications running on Intel(R) 64, Version 2021.1
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Compiler Version Notes (Continued)

=====
C++, C | 511.povray_r(peak)

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Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.1.1.217 Build 20200306
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

=====
C++, C, Fortran | 507.cactuBSSN_r(base, peak)

Intel(R) C++ Compiler for applications running on Intel(R) 64, Version 2021.1
NextGen Build 20200304
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Intel(R) C Compiler for applications running on Intel(R) 64, Version 2021.1
NextGen Build 20200304
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
64, Version 19.1.1.217 Build 20200306
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

=====
Fortran | 503.bwaves_r(base, peak) 549.fotonik3d_r(base, peak)
554.roms_r(base, peak)

Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
64, Version 19.1.1.217 Build 20200306
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

=====
Fortran, C | 521.wrf_r(base) 527.cam4_r(base, peak)

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=====
Fortran, C | 521.wrf_r(peak)

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=====
Fortran, C | 521.wrf_r(base) 527.cam4_r(base, peak)

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Fortran, C | 521.wrf_r(peak)

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Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.1.1.217 Build 20200306
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Base Compiler Invocation

C benchmarks:
icc

C++ benchmarks:
icpc

Fortran benchmarks:
ifort

Benchmarks using both Fortran and C:
ifort icc

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Base Compiler Invocation (Continued)

Benchmarks using both C and C++:

icpc icc

Benchmarks using Fortran, C, and C++:

icpc icc ifort

Base Portability Flags

503.bwaves_r: -DSPEC_LP64
 507.cactuBSSN_r: -DSPEC_LP64
 508.namd_r: -DSPEC_LP64
 510.parest_r: -DSPEC_LP64
 511.povray_r: -DSPEC_LP64
 519.lbm_r: -DSPEC_LP64
 521.wrf_r: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
 526.blender_r: -DSPEC_LP64 -DSPEC_LINUX -funsigned-char
 527.cam4_r: -DSPEC_LP64 -DSPEC_CASE_FLAG
 538.imagick_r: -DSPEC_LP64
 544.nab_r: -DSPEC_LP64
 549.fotonik3d_r: -DSPEC_LP64
 554.roms_r: -DSPEC_LP64

Base Optimization Flags

C benchmarks:

-m64 -qnextgen -std=c11
 -Wl,-plugin-opt=-x86-branches-within-32B-boundaries -Wl,-z,muldefs
 -fuse-ld=gold -xCORE-AVX512 -Ofast -ffast-math -flto -mfpmath=sse
 -funroll-loops -qopt-mem-layout-trans=4 -L/usr/local/je5.0.1-64/lib
 -ljemalloc

C++ benchmarks:

-m64 -qnextgen -Wl,-plugin-opt=-x86-branches-within-32B-boundaries
 -Wl,-z,muldefs -fuse-ld=gold -xCORE-AVX512 -Ofast -ffast-math -flto
 -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
 -L/usr/local/je5.0.1-64/lib -ljemalloc

Fortran benchmarks:

-m64 -Wl,-plugin-opt=-x86-branches-within-32B-boundaries -Wl,-z,muldefs
 -fuse-ld=gold -xCORE-AVX512 -O3 -ipo -no-prec-div -qopt-prefetch
 -ffinite-math-only -qopt-multiple-gather-scatter-by-shuffles
 -qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte

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Base Optimization Flags (Continued)

Fortran benchmarks (continued):

```
-auto -mbranches-within-32B-boundaries -L/usr/local/je5.0.1-64/lib  
-ljemalloc
```

Benchmarks using both Fortran and C:

```
-m64 -qnextgen -std=c11  
-Wl,-plugin-opt=-x86-branches-within-32B-boundaries -Wl,-z,muldefs  
-fuse-ld=gold -xCORE-AVX512 -Ofast -ffast-math -flto -mfpmath=sse  
-funroll-loops -qopt-mem-layout-trans=4 -O3 -ipo -no-prec-div  
-qopt-prefetch -ffinite-math-only  
-qopt-multiple-gather-scatter-by-shuffles -nostandard-realloc-lhs  
-align array32byte -auto -mbranches-within-32B-boundaries  
-L/usr/local/je5.0.1-64/lib -ljemalloc
```

Benchmarks using both C and C++:

```
-m64 -qnextgen -std=c11  
-Wl,-plugin-opt=-x86-branches-within-32B-boundaries -Wl,-z,muldefs  
-fuse-ld=gold -xCORE-AVX512 -Ofast -ffast-math -flto -mfpmath=sse  
-funroll-loops -qopt-mem-layout-trans=4 -L/usr/local/je5.0.1-64/lib  
-ljemalloc
```

Benchmarks using Fortran, C, and C++:

```
-m64 -qnextgen -std=c11  
-Wl,-plugin-opt=-x86-branches-within-32B-boundaries -Wl,-z,muldefs  
-fuse-ld=gold -xCORE-AVX512 -Ofast -ffast-math -flto -mfpmath=sse  
-funroll-loops -qopt-mem-layout-trans=4 -O3 -ipo -no-prec-div  
-qopt-prefetch -ffinite-math-only  
-qopt-multiple-gather-scatter-by-shuffles -nostandard-realloc-lhs  
-align array32byte -auto -mbranches-within-32B-boundaries  
-L/usr/local/je5.0.1-64/lib -ljemalloc
```

Peak Compiler Invocation

C benchmarks:

```
icc
```

C++ benchmarks:

```
icpc
```

Fortran benchmarks:

```
ifort
```

Benchmarks using both Fortran and C:

```
ifort icc
```

(Continued on next page)



SPEC CPU®2017 Floating Point Rate Result

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Tyrone Systems

(Test Sponsor: Netweb Pte Ltd)

Tyrone Camarero DS400E1U-224R4
(2.10 GHz, Intel Xeon Gold 6252)

SPECrate®2017_fp_base = 241

SPECrate®2017_fp_peak = 244

CPU2017 License: 006042

Test Sponsor: Netweb Pte Ltd

Tested by: Tyrone Systems

Test Date: Feb-2021

Hardware Availability: Aug-2020

Software Availability: Dec-2020

Peak Compiler Invocation (Continued)

Benchmarks using both C and C++:

```
icpc icc
```

Benchmarks using Fortran, C, and C++:

```
icpc icc ifort
```

Peak Portability Flags

Same as Base Portability Flags

Peak Optimization Flags

C benchmarks:

```
519.lbm_r: basepeak = yes
```

```
538.imagick_r: basepeak = yes
```

```
544.nab_r: basepeak = yes
```

C++ benchmarks:

```
508.namd_r: basepeak = yes
```

```
510.parest_r: -m64 -qnextgen
```

```
-Wl,-plugin-opt=-x86-branches-within-32B-boundaries  
-Wl,-z,muldefs -fuse-ld=gold -xCORE-AVX512 -Ofast  
-ffast-math -flto -mfpmath=sse -funroll-loops  
-qopt-mem-layout-trans=4 -L/usr/local/je5.0.1-64/lib  
-ljemalloc
```

Fortran benchmarks:

```
503.bwaves_r: -m64 -Wl,-plugin-opt=-x86-branches-within-32B-boundaries  
-Wl,-z,muldefs -fuse-ld=gold -xCORE-AVX512 -O3 -ipo  
-no-prec-div -qopt-prefetch -ffinite-math-only  
-qopt-multiple-gather-scatter-by-shuffles  
-qopt-mem-layout-trans=4 -nostandard-realloc-lhs  
-align array32byte -auto -mbranches-within-32B-boundaries  
-L/usr/local/je5.0.1-64/lib -ljemalloc
```

(Continued on next page)



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Hardware Availability: Aug-2020

Software Availability: Dec-2020

Peak Optimization Flags (Continued)

549.fotonik3d_r: basepeak = yes

554.roms_r: Same as 503.bwaves_r

Benchmarks using both Fortran and C:

```
521.wrf_r: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX512 -O3
-ipo -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles
-qopt-mem-layout-trans=4 -mbranches-within-32B-boundaries
-nostandard-realloc-lhs -align array32byte -auto
-L/usr/local/je5.0.1-64/lib -ljemalloc
```

527.cam4_r: basepeak = yes

Benchmarks using both C and C++:

```
511.povray_r: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX512 -O3
-ipo -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles
-qopt-mem-layout-trans=4 -mbranches-within-32B-boundaries
-L/usr/local/je5.0.1-64/lib -ljemalloc
```

526.blender_r: basepeak = yes

Benchmarks using Fortran, C, and C++:

507.cactuBSSN_r: basepeak = yes

The flags files that were used to format this result can be browsed at

http://www.spec.org/cpu2017/flags/Intel-ic19.1ul-official-linux64_revA.html

<http://www.spec.org/cpu2017/flags/Tyrone-Platform-Settings-V1.2-CLX-revB.html>

You can also download the XML flags sources by saving the following links:

http://www.spec.org/cpu2017/flags/Intel-ic19.1ul-official-linux64_revA.xml

<http://www.spec.org/cpu2017/flags/Tyrone-Platform-Settings-V1.2-CLX-revB.xml>

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