



# SPEC CPU®2017 Floating Point Rate Result

Copyright 2017-2021 Standard Performance Evaluation Corporation

**Huawei**  
(Test Sponsor: China Academy of Information and Communications Technology)

SPECrate®2017\_fp\_base = 250

**Huawei 1288H V5 (Intel Xeon Gold 6246R)**

SPECrate®2017\_fp\_peak = Not Run

CPU2017 License: 6177

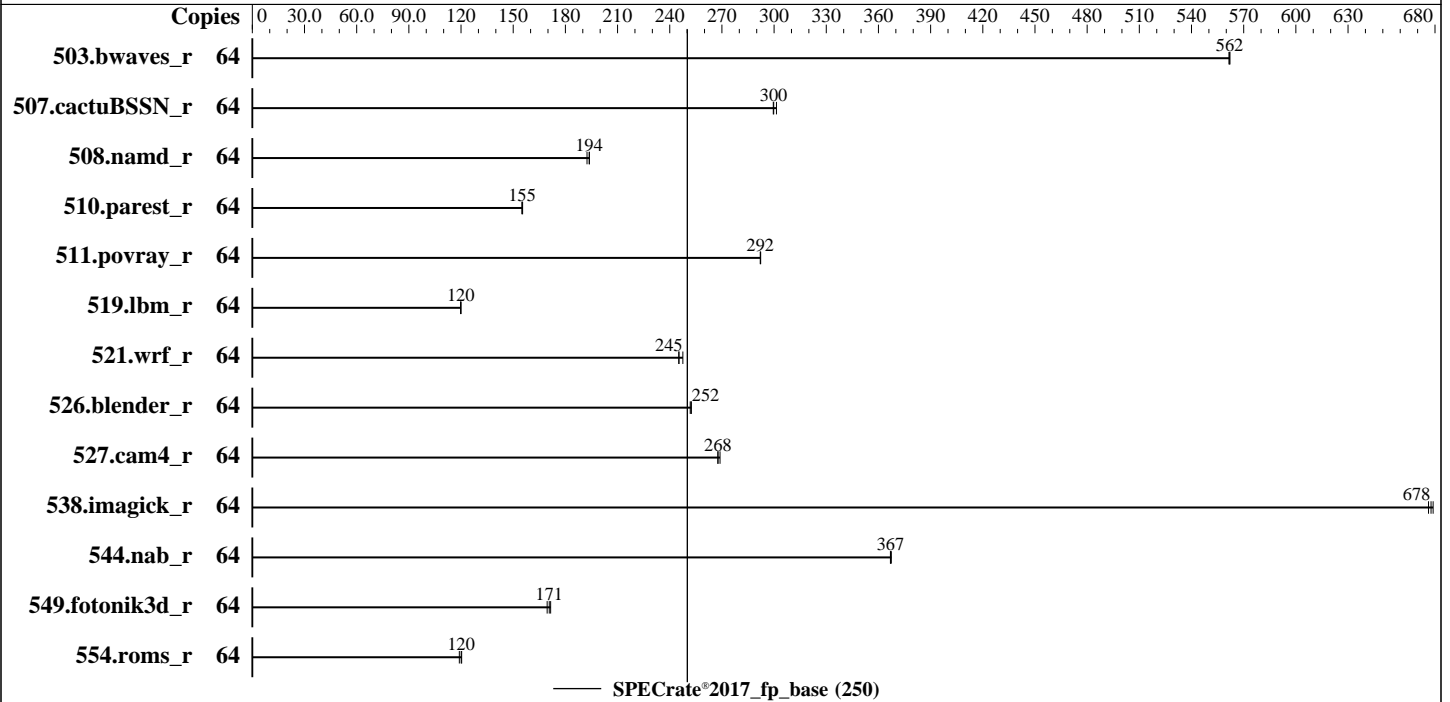
Test Date: Jan-2021

Test Sponsor: China Academy of Information and Communications Technology

Hardware Availability: Feb-2020

Tested by: China Academy of Information and Communications Technology

Software Availability: Apr-2020



## Hardware

CPU Name: Intel Xeon Gold 6246R  
 Max MHz: 4100  
 Nominal: 3400  
 Enabled: 32 cores, 2 chips, 2 threads/core  
 Orderable: 1,2 chips  
 Cache L1: 32 KB I + 32 KB D on chip per core  
 L2: 1 MB I+D on chip per core  
 L3: 35.75 MB I+D on chip per chip  
 Other: None  
 Memory: 768 GB (24 x 32 GB 2Rx4 PC4-2933Y-R)  
 Storage: 1 x 960 GB SAS SSD  
 Other: None

## Software

OS: SUSE Linux Enterprise Server 12 SP4 (x86\_64)  
 Kernel 4.12.14-94.41-default  
 Compiler: C/C++: Version 19.1.1.217 of Intel C/C++ Compiler for Linux;  
 Fortran: Version 19.1.1.217 of Intel Fortran Compiler for Linux  
 Parallel: No  
 Firmware: Version 6.83 released Jun-2019  
 File System: xfs  
 System State: Run level 3 (multi-user)  
 Base Pointers: 64-bit  
 Peak Pointers: Not Applicable  
 Other: jemalloc memory allocator V5.0.1  
 Power Management: BIOS set to prefer performance at the cost of additional power usage.



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## Results Table

Benchmark	Base							Peak						
	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
503.bwaves_r	64	1142	562	1143	562	<u>1142</u>	<u>562</u>							
507.cactuBSSN_r	64	<u>270</u>	<u>300</u>	269	301	271	300							
508.namd_r	64	<u>314</u>	<u>194</u>	316	192	314	194							
510.parest_r	64	1077	155	<u>1079</u>	<u>155</u>	1080	155							
511.povray_r	64	511	292	<u>512</u>	<u>292</u>	512	292							
519.lbm_r	64	<u>563</u>	<u>120</u>	562	120	563	120							
521.wrf_r	64	<u>584</u>	<u>245</u>	585	245	579	248							
526.blender_r	64	<u>386</u>	<u>252</u>	387	252	386	252							
527.cam4_r	64	418	268	416	269	<u>418</u>	<u>268</u>							
538.imagick_r	64	234	679	235	676	<u>235</u>	<u>678</u>							
544.nab_r	64	<u>294</u>	<u>367</u>	293	367	294	367							
549.fotonik3d_r	64	1471	170	1454	172	<u>1461</u>	<u>171</u>							
554.roms_r	64	<u>847</u>	<u>120</u>	845	120	854	119							

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Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

## Compiler Notes

The inconsistent Compiler version information under Compiler Version section is due to a discrepancy in Intel Compiler. The correct version of C/C++ compiler is: Version 19.1.1.217 Build 20200306 Compiler for Linux. The correct version of Fortran compiler is: Version 19.1.1.217 Build 20200306 Compiler for Linux.

## Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

## Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

## Environment Variables Notes

Environment variables set by runcpu before the start of the run:  
LD\_LIBRARY\_PATH =  
"/opt/intel/compilers\_and\_libraries\_2020.1.217/linux/compiler/lib/intel64:/usr/local/jemalloc64-5.0.1"  
MALLOCONF = "retain:true"



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## General Notes

Transparent Huge Pages enabled by default  
 Prior to runcpu invocation  
 Filesystem page cache synced and cleared with:  
`sync; echo 3> /proc/sys/vm/drop_caches`  
 runcpu command invoked through numactl i.e.:  
`numactl --interleave=all runcpu <etc>`  
 NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.  
 Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.  
 Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.  
 jemalloc, a general purpose malloc implementation  
 built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5  
 sources available from jemalloc.net or <https://github.com/jemalloc/jemalloc/releases>

## Platform Notes

BIOS configuration:  
 Power Policy Set to Performance  
 SNC Set to Enabled  
 IMC Interleaving Set to 1-way Interleave  
 XPT Prefetch Set to Enabled

Sysinfo program /spec2017/bin/sysinfo  
 Rev: r6365 of 2019-08-21 295195f888a3d7edble6e46a485a0011  
 running on linux-j3dr Fri Jan 15 20:44:43 2021

SUT (System Under Test) info as seen by some common utilities.  
 For more information on this section, see  
<https://www.spec.org/cpu2017/Docs/config.html#sysinfo>

From /proc/cpuinfo  
 model name : Intel(R) Xeon(R) Gold 6246R CPU @ 3.40GHz  
 2 "physical id"s (chips)  
 64 "processors"  
 cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)  
 cpu cores : 16  
 siblings : 32  
 physical 0: cores 0 2 3 5 6 9 10 12 13 16 18 20 21 24 27 29  
 physical 1: cores 0 2 3 5 6 9 10 12 13 16 18 20 21 24 27 29

From lscpu:  
 Architecture: x86\_64  
 CPU op-mode(s): 32-bit, 64-bit

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## Platform Notes (Continued)

```

Byte Order:                Little Endian
CPU(s):                    64
On-line CPU(s) list:      0-63
Thread(s) per core:       2
Core(s) per socket:      16
Socket(s):                 2
NUMA node(s):             4
Vendor ID:                 GenuineIntel
CPU family:                6
Model:                     85
Model name:                Intel(R) Xeon(R) Gold 6246R CPU @ 3.40GHz
Stepping:                  7
CPU MHz:                   3400.000
CPU max MHz:               4100.0000
CPU min MHz:               1200.0000
BogoMIPS:                  6800.00
Virtualization:           VT-x
L1d cache:                 32K
L1i cache:                 32K
L2 cache:                  1024K
L3 cache:                  36608K
NUMA node0 CPU(s):        0-2,5,6,9,10,13,32-34,37,38,41,42,45
NUMA node1 CPU(s):        3,4,7,8,11,12,14,15,35,36,39,40,43,44,46,47
NUMA node2 CPU(s):        16-18,21,22,25,26,29,48-50,53,54,57,58,61
NUMA node3 CPU(s):        19,20,23,24,27,28,30,31,51,52,55,56,59,60,62,63
Flags:                     fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
aperfmpperf pni pclmulqdq dtes64 ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm
pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c
rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_l3 cdp_l3 invpcid_single ssbd
mba ibrs ibpb stibp tpr_shadow vnmi flexpriority ept vpid fsgsbase tsc_adjust bml
hle avx2 smep bmi2 erms invpcid rtm cqm mpx rdt_a avx512f avx512dq rdseed adx smap
clflushopt clwb intel_pt avx512cd avx512bw avx512vl xsaveopt xsavec xgetbv1 xsave
cqm_llc cqm_occup_llc cqm_mbm_total cqm_mbm_local dtherm ida arat pln pts pku ospke
avx512_vnni flush_lld arch_capabilities

```

```

/proc/cpuinfo cache data
cache size : 36608 KB

```

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.

```

available: 4 nodes (0-3)
node 0 cpus: 0 1 2 5 6 9 10 13 32 33 34 37 38 41 42 45
node 0 size: 192046 MB
node 0 free: 186507 MB
node 1 cpus: 3 4 7 8 11 12 14 15 35 36 39 40 43 44 46 47

```

(Continued on next page)



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## Platform Notes (Continued)

```

node 1 size: 193532 MB
node 1 free: 189752 MB
node 2 cpus: 16 17 18 21 22 25 26 29 48 49 50 53 54 57 58 61
node 2 size: 193503 MB
node 2 free: 189782 MB
node 3 cpus: 19 20 23 24 27 28 30 31 51 52 55 56 59 60 62 63
node 3 size: 193531 MB
node 3 free: 189793 MB
node distances:
node  0  1  2  3
  0:  10  11  21  21
  1:  11  10  21  21
  2:  21  21  10  11
  3:  21  21  11  10

```

```

From /proc/meminfo
MemTotal:      791158076 kB
HugePages_Total:      0
Hugepagesize:    2048 kB

```

```

From /etc/*release* /etc/*version*
SuSE-release:
  SUSE Linux Enterprise Server 12 (x86_64)
  VERSION = 12
  PATCHLEVEL = 4
  # This file is deprecated and will be removed in a future service pack or release.
  # Please check /etc/os-release for details about this release.
os-release:
  NAME="SLES"
  VERSION="12-SP4"
  VERSION_ID="12.4"
  PRETTY_NAME="SUSE Linux Enterprise Server 12 SP4"
  ID="sles"
  ANSI_COLOR="0;32"
  CPE_NAME="cpe:/o:suse:sles:12:sp4"

```

```

uname -a:
Linux linux-j3dr 4.12.14-94.41-default #1 SMP Wed Oct 31 12:25:04 UTC 2018 (3090901)
x86_64 x86_64 x86_64 GNU/Linux

```

Kernel self-reported vulnerability status:

```

CVE-2018-3620 (L1 Terminal Fault):      Not affected
Microarchitectural Data Sampling:      No status reported
CVE-2017-5754 (Meltdown):              Not affected
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled
                                          via prctl and seccomp

```

(Continued on next page)



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## Platform Notes (Continued)

CVE-2017-5753 (Spectre variant 1):	Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2):	Mitigation: Indirect Branch Restricted Speculation, IBPB, IBRS_FW

run-level 3 Jan 15 17:30

SPEC is set to: /spec2017

Filesystem	Type	Size	Used	Avail	Use%	Mounted on
/dev/sda3	xfs	734G	68G	667G	10%	/

```

From /sys/devices/virtual/dmi/id
  BIOS:      INSYDE Corp. 6.83 06/29/2019
  Vendor:    Huawei
  Product:   1288H V5
  Product Family: Purley
  Serial:    Serial Number

```

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

```

Memory:
  24x Samsung M393A4K40CB2-CVF 32 GB 2 rank 2933

```

(End of data from sysinfo program)

## Compiler Version Notes

```

=====
C | 519.lbm_r(base) 538.imagick_r(base) 544.nab_r(base)
-----

```

```

Intel(R) C Compiler for applications running on Intel(R) 64, Version 2021.1
  NextGen Build 20200304
  Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
-----

```

```

=====
C++ | 508.namd_r(base) 510.parest_r(base)
-----

```

```

Intel(R) C++ Compiler for applications running on Intel(R) 64, Version 2021.1
  NextGen Build 20200304
  Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
-----

```

```

=====
C++, C | 511.povray_r(base) 526.blender_r(base)
-----

```

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## Compiler Version Notes (Continued)

```
-----
Intel(R) C++ Compiler for applications running on Intel(R) 64, Version 2021.1
  NextGen Build 20200304
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Intel(R) C Compiler for applications running on Intel(R) 64, Version 2021.1
  NextGen Build 20200304
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
-----
```

```
=====
C++, C, Fortran | 507.cactuBSSN_r(base)
-----
```

```
Intel(R) C++ Compiler for applications running on Intel(R) 64, Version 2021.1
  NextGen Build 20200304
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Intel(R) C Compiler for applications running on Intel(R) 64, Version 2021.1
  NextGen Build 20200304
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
  64, Version 19.1.1.217 Build 20200306
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
-----
```

```
=====
Fortran | 503.bwaves_r(base) 549.fotonik3d_r(base) 554.roms_r(base)
-----
```

```
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
  64, Version 19.1.1.217 Build 20200306
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
-----
```

```
=====
Fortran, C | 521.wrf_r(base) 527.cam4_r(base)
-----
```

```
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
  64, Version 19.1.1.217 Build 20200306
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Intel(R) C Compiler for applications running on Intel(R) 64, Version 2021.1
  NextGen Build 20200304
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-----
```

## Base Compiler Invocation

C benchmarks:  
icc

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## Base Compiler Invocation (Continued)

C++ benchmarks:

icpc

Fortran benchmarks:

ifort

Benchmarks using both Fortran and C:

ifort icc

Benchmarks using both C and C++:

icpc icc

Benchmarks using Fortran, C, and C++:

icpc icc ifort

## Base Portability Flags

```
503.bwaves_r: -DSPEC_LP64
507.cactuBSSN_r: -DSPEC_LP64
508.namd_r: -DSPEC_LP64
510.parest_r: -DSPEC_LP64
511.povray_r: -DSPEC_LP64
519.lbm_r: -DSPEC_LP64
521.wrf_r: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
526.blender_r: -DSPEC_LP64 -DSPEC_LINUX -funsigned-char
527.cam4_r: -DSPEC_LP64 -DSPEC_CASE_FLAG
538.imagick_r: -DSPEC_LP64
544.nab_r: -DSPEC_LP64
549.fotonik3d_r: -DSPEC_LP64
554.roms_r: -DSPEC_LP64
```

## Base Optimization Flags

C benchmarks:

```
-m64 -qnextgen -std=c11
-Wl,-plugin-opt=-x86-branches-within-32B-boundaries -Wl,-z,muldefs
-fuse-ld=gold -xCORE-AVX2 -Ofast -ffast-math -flto -mfpmath=sse
-funroll-loops -qopt-mem-layout-trans=4 -L/usr/local/jemalloc64-5.0.1/
-ljemalloc
```

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## Base Optimization Flags (Continued)

### C++ benchmarks:

```
-m64 -qnextgen -Wl,-plugin-opt=-x86-branches-within-32B-boundaries
-Wl,-z,muldefs -fuse-ld=gold -xCORE-AVX2 -Ofast -ffast-math -flto
-mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-L/usr/local/jemalloc64-5.0.1/ -ljemalloc
```

### Fortran benchmarks:

```
-m64 -Wl,-plugin-opt=-x86-branches-within-32B-boundaries -Wl,-z,muldefs
-fuse-ld=gold -xCORE-AVX2 -O3 -ipo -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-multiple-gather-scatter-by-shuffles
-qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte
-auto -mbranches-within-32B-boundaries -L/usr/local/jemalloc64-5.0.1/
-ljemalloc
```

### Benchmarks using both Fortran and C:

```
-m64 -qnextgen -std=c11
-Wl,-plugin-opt=-x86-branches-within-32B-boundaries -Wl,-z,muldefs
-fuse-ld=gold -xCORE-AVX2 -Ofast -ffast-math -flto -mfpmath=sse
-funroll-loops -qopt-mem-layout-trans=4 -O3 -ipo -no-prec-div
-qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles -nostandard-realloc-lhs
-align array32byte -auto -mbranches-within-32B-boundaries
-L/usr/local/jemalloc64-5.0.1/ -ljemalloc
```

### Benchmarks using both C and C++:

```
-m64 -qnextgen -std=c11
-Wl,-plugin-opt=-x86-branches-within-32B-boundaries -Wl,-z,muldefs
-fuse-ld=gold -xCORE-AVX2 -Ofast -ffast-math -flto -mfpmath=sse
-funroll-loops -qopt-mem-layout-trans=4 -L/usr/local/jemalloc64-5.0.1/
-ljemalloc
```

### Benchmarks using Fortran, C, and C++:

```
-m64 -qnextgen -std=c11
-Wl,-plugin-opt=-x86-branches-within-32B-boundaries -Wl,-z,muldefs
-fuse-ld=gold -xCORE-AVX2 -Ofast -ffast-math -flto -mfpmath=sse
-funroll-loops -qopt-mem-layout-trans=4 -O3 -ipo -no-prec-div
-qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles -nostandard-realloc-lhs
-align array32byte -auto -mbranches-within-32B-boundaries
-L/usr/local/jemalloc64-5.0.1/ -ljemalloc
```

The flags files that were used to format this result can be browsed at

[http://www.spec.org/cpu2017/flags/Intel-ic19.1u1-official-linux64\\_revB.html](http://www.spec.org/cpu2017/flags/Intel-ic19.1u1-official-linux64_revB.html)

<http://www.spec.org/cpu2017/flags/CAICT-Platform-Settings-V1.3.html>



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You can also download the XML flags sources by saving the following links:

[http://www.spec.org/cpu2017/flags/Intel-ic19.1u1-official-linux64\\_revB.xml](http://www.spec.org/cpu2017/flags/Intel-ic19.1u1-official-linux64_revB.xml)

<http://www.spec.org/cpu2017/flags/CAICT-Platform-Settings-V1.3.xml>

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For questions about this result, please contact the tester. For other inquiries, please contact [info@spec.org](mailto:info@spec.org).

Tested with SPEC CPU®2017 v1.1.0 on 2021-01-15 07:44:43-0500.

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