



# SPEC CPU®2017 Integer Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

## Huawei

(Test Sponsor: China Academy of Information and Communications Technology)

SPECrate®2017\_int\_base = 160

SPECrate®2017\_int\_peak = 165

### Huawei 2288H V5 (Intel Xeon Silver 4214R)

CPU2017 License: 6177

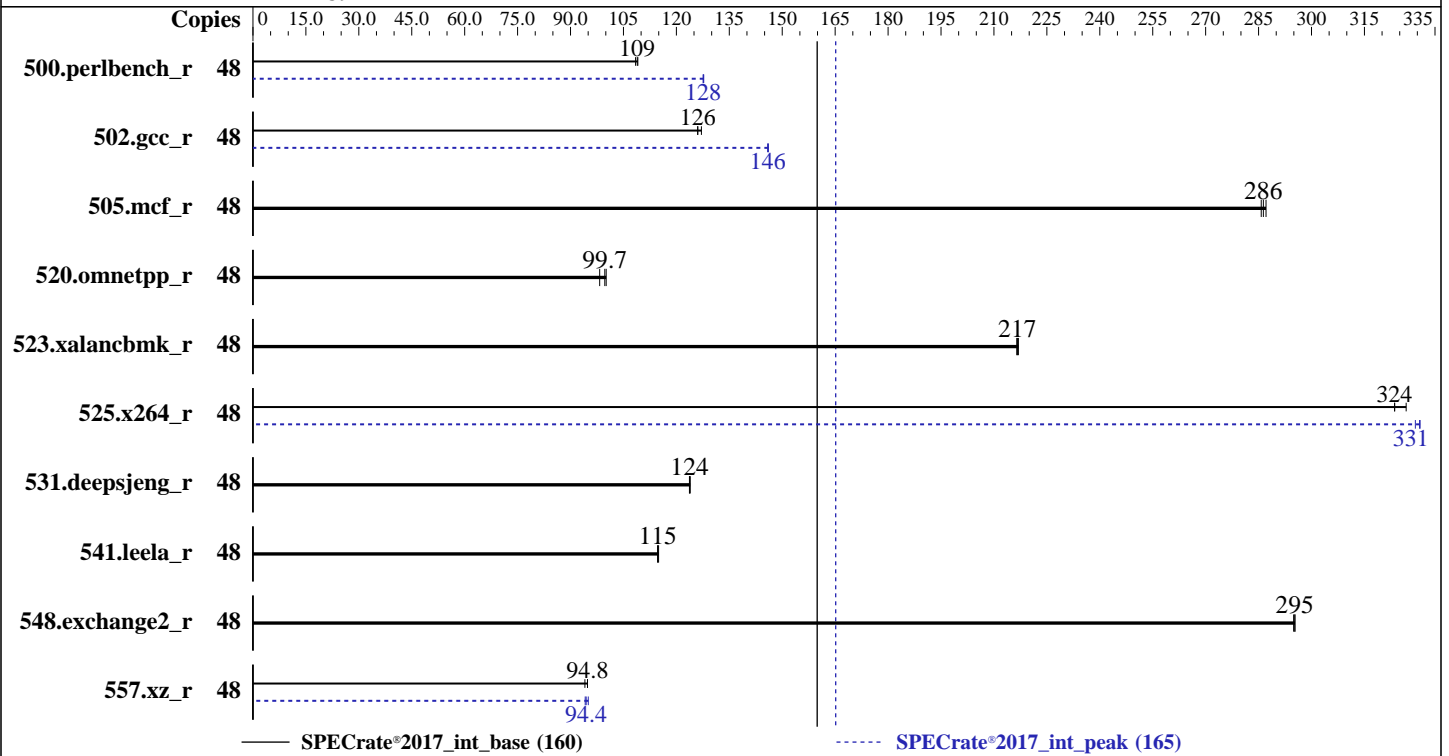
Test Sponsor: China Academy of Information and Communications Technology

Tested by: China Academy of Information and Communications Technology

Test Date: Jul-2020

Hardware Availability: Mar-2020

Software Availability: Apr-2020



### Hardware

CPU Name: Intel Xeon Silver 4214R  
 Max MHz: 3500  
 Nominal: 2400  
 Enabled: 24 cores, 2 chips, 2 threads/core  
 Orderable: 1,2 chips  
 Cache L1: 32 KB I + 32 KB D on chip per core  
 L2: 1 MB I+D on chip per core  
 L3: 16.5 MB I+D on chip per chip  
 Other: None  
 Memory: 768 GB (24 x 32 GB 2Rx4 PC4-2933Y-R, running at 2400)  
 Storage: 1 x 800 GB SAS SSD  
 Other: None

### Software

OS: SUSE Linux Enterprise Server 12 SP4 (x86\_64)  
 Kernel 4.12.14-94.41-default  
 Compiler: C/C++: Version 19.1.1.217 of Intel C/C++ Compiler for Linux;  
 Fortran: Version 19.1.1.217 of Intel Fortran Compiler for Linux  
 Parallel: No  
 Firmware: Version 6.83 released Jun-2019  
 File System: xfs  
 System State: Run level 3 (multi-user)  
 Base Pointers: 64-bit  
 Peak Pointers: 32/64-bit  
 Other: jemalloc memory allocator V5.0.1  
 Power Management: BIOS set to prefer performance at the cost of additional power usage.



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## Results Table

Benchmark	Base							Peak						
	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
500.perlbench_r	48	705	108	<b><u>702</u></b>	<b><u>109</u></b>	701	109	48	598	128	<b><u>599</u></b>	<b><u>128</u></b>	599	128
502.gcc_r	48	<b><u>539</u></b>	<b><u>126</u></b>	535	127	539	126	48	<b><u>466</u></b>	<b><u>146</u></b>	465	146	466	146
505.mcf_r	48	271	286	<b><u>271</u></b>	<b><u>286</u></b>	270	287	48	271	286	<b><u>271</u></b>	<b><u>286</u></b>	270	287
520.omnetpp_r	48	641	98.3	629	100	<b><u>632</u></b>	<b><u>99.7</u></b>	48	641	98.3	629	100	<b><u>632</u></b>	<b><u>99.7</u></b>
523.xalancbmk_r	48	234	216	234	217	<b><u>234</u></b>	<b><u>217</u></b>	48	234	216	234	217	<b><u>234</u></b>	<b><u>217</u></b>
525.x264_r	48	<b><u>260</u></b>	<b><u>324</u></b>	260	324	257	327	48	<b><u>254</u></b>	<b><u>331</u></b>	254	331	255	329
531.deepsjeng_r	48	<b><u>444</u></b>	<b><u>124</u></b>	445	124	444	124	48	<b><u>444</u></b>	<b><u>124</u></b>	445	124	444	124
541.leela_r	48	693	115	691	115	<b><u>693</u></b>	<b><u>115</u></b>	48	693	115	691	115	<b><u>693</u></b>	<b><u>115</u></b>
548.exchange2_r	48	426	295	<b><u>426</u></b>	<b><u>295</u></b>	426	295	48	426	295	<b><u>426</u></b>	<b><u>295</u></b>	426	295
557.xz_r	48	<b><u>547</u></b>	<b><u>94.8</u></b>	547	94.8	551	94.1	48	551	94.2	545	95.0	<b><u>549</u></b>	<b><u>94.4</u></b>

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Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

## Compiler Notes

The inconsistent Compiler version information under Compiler Version section is due to a discrepancy in Intel Compiler. The correct version of C/C++ compiler is: Version 19.1.1.217 Build 20200306 Compiler for Linux. The correct version of Fortran compiler is: Version 19.1.1.217 Build 20200306 Compiler for Linux. SPEC has learned that this result, which used an evaluation compiler, was submitted contrary to the compiler license terms. Intel has granted a one-time waiver for this result.

## Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

## Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

## Environment Variables Notes

Environment variables set by runcpu before the start of the run:  
LD\_LIBRARY\_PATH =  
"/opt/intel/compilers\_and\_libraries\_2020.1.217/linux/compiler/lib/intel64  
4:/opt/intel/compilers\_and\_libraries\_2020.1.217/linux/compiler/lib/ia32:  
/usr/local/jemalloc32-5.0.1"

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## Environment Variables Notes (Continued)

MALLOC\_CONF = "retain:true"

## General Notes

Transparent Huge Pages enabled by default  
 Prior to runcpu invocation  
 Filesystem page cache synced and cleared with:  
 sync; echo 3> /proc/sys/vm/drop\_caches  
 runcpu command invoked through numactl i.e.:  
 numactl --interleave=all runcpu <etc>  
 NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.  
 Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.  
 Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.  
 jemalloc, a general purpose malloc implementation  
 built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5  
 sources available from jemalloc.net or <https://github.com/jemalloc/jemalloc/releases>

## Platform Notes

BIOS configuration:  
 Power Policy Set to Performance  
 SNC Set to Enabled  
 IMC Interleaving Set to 1-way Interleave  
 XPT Prefetch Set to Enabled

Sysinfo program /spec2017/bin/sysinfo  
 Rev: r6365 of 2019-08-21 295195f888a3d7edble6e46a485a0011  
 running on linux-r48i Wed Jul 22 15:29:01 2020

SUT (System Under Test) info as seen by some common utilities.  
 For more information on this section, see  
<https://www.spec.org/cpu2017/Docs/config.html#sysinfo>

From /proc/cpuinfo  
 model name : Intel(R) Xeon(R) Silver 4214R CPU @ 2.40GHz  
 2 "physical id"s (chips)  
 48 "processors"  
 cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)  
 cpu cores : 12

(Continued on next page)



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## Platform Notes (Continued)

```
siblings : 24
physical 0: cores 0 1 2 3 4 5 8 9 10 11 12 13
physical 1: cores 0 1 2 3 4 5 8 9 10 11 12 13
```

From lscpu:

```
Architecture:          x86_64
CPU op-mode(s):        32-bit, 64-bit
Byte Order:            Little Endian
CPU(s):                48
On-line CPU(s) list:   0-47
Thread(s) per core:    2
Core(s) per socket:    12
Socket(s):              2
NUMA node(s):          4
Vendor ID:              GenuineIntel
CPU family:             6
Model:                 85
Model name:             Intel(R) Xeon(R) Silver 4214R CPU @ 2.40GHz
Stepping:               7
CPU MHz:               2400.000
CPU max MHz:           3500.0000
CPU min MHz:           1000.0000
BogoMIPS:              4800.00
Virtualization:        VT-x
L1d cache:             32K
L1i cache:             32K
L2 cache:              1024K
L3 cache:              16896K
NUMA node0 CPU(s):    0-2,6-8,24-26,30-32
NUMA node1 CPU(s):    3-5,9-11,27-29,33-35
NUMA node2 CPU(s):    12-14,18-20,36-38,42-44
NUMA node3 CPU(s):    15-17,21-23,39-41,45-47
Flags:                 fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
aperfmpperf pni pclmulqdq dtes64 ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm
pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c
rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_l3 cdp_l3 invpcid_single ssbd
mba ibrs ibpb stibp tpr_shadow vnmi flexpriority ept vpid fsgsbase tsc_adjust bml
hle avx2 smep bmi2 erms invpcid rtm cqm mpx rdt_a avx512f avx512dq rdseed adx smap
clflushopt clwb intel_pt avx512cd avx512bw avx512vl xsaveopt xsavec xgetbv1 xsaves
cqm_llc cqm_occup_llc cqm_mbm_total cqm_mbm_local dtherm ida arat pln pts pku ospke
avx512_vnni flush_l1d arch_capabilities
```

/proc/cpuinfo cache data

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## Platform Notes (Continued)

cache size : 16896 KB

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.

```

available: 4 nodes (0-3)
node 0 cpus: 0 1 2 6 7 8 24 25 26 30 31 32
node 0 size: 191975 MB
node 0 free: 191551 MB
node 1 cpus: 3 4 5 9 10 11 27 28 29 33 34 35
node 1 size: 193533 MB
node 1 free: 193303 MB
node 2 cpus: 12 13 14 18 19 20 36 37 38 42 43 44
node 2 size: 193533 MB
node 2 free: 193268 MB
node 3 cpus: 15 16 17 21 22 23 39 40 41 45 46 47
node 3 size: 193295 MB
node 3 free: 193066 MB
node distances:
node  0  1  2  3
  0: 10 11 21 21
  1: 11 10 21 21
  2: 21 21 10 11
  3: 21 21 11 10

```

```

From /proc/meminfo
MemTotal:      790872868 kB
HugePages_Total:      0
Hugepagesize:    2048 kB

```

```

From /etc/*release* /etc/*version*
SuSE-release:
  SUSE Linux Enterprise Server 12 (x86_64)
  VERSION = 12
  PATCHLEVEL = 4
  # This file is deprecated and will be removed in a future service pack or release.
  # Please check /etc/os-release for details about this release.
os-release:
NAME="SLES"
VERSION="12-SP4"
VERSION_ID="12.4"
PRETTY_NAME="SUSE Linux Enterprise Server 12 SP4"
ID="sles"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:12:sp4"

```

(Continued on next page)



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## Platform Notes (Continued)

uname -a:

```
Linux linux-r48i 4.12.14-94.41-default #1 SMP Wed Oct 31 12:25:04 UTC 2018 (3090901)
x86_64 x86_64 x86_64 GNU/Linux
```

Kernel self-reported vulnerability status:

CVE-2018-3620 (L1 Terminal Fault):	Not affected
Microarchitectural Data Sampling:	No status reported
CVE-2017-5754 (Meltdown):	Not affected
CVE-2018-3639 (Speculative Store Bypass):	Mitigation: Speculative Store Bypass disabled via prctl and seccomp
CVE-2017-5753 (Spectre variant 1):	Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2):	Mitigation: Indirect Branch Restricted Speculation, IBPB, IBRS_FW

run-level 3 Jul 22 12:03

SPEC is set to: /spec2017

Filesystem	Type	Size	Used	Avail	Use%	Mounted on
/dev/sda3	xfs	730G	119G	612G	17%	/

From /sys/devices/virtual/dmi/id

```
BIOS:      INSYDE Corp. 6.83 06/29/2019
Vendor:    Huawei
Product:   2288H V5
Product Family: Purley
Serial:    Huawei
```

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

Memory:

24x Samsung M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2400

(End of data from sysinfo program)

## Compiler Version Notes

C | 502.gcc\_r(peak)

Intel(R) C Compiler for applications running on IA-32, Version 2021.1 NextGen  
Build 20200304

(Continued on next page)



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**Software Availability:** Apr-2020

## Compiler Version Notes (Continued)

Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

```

=====
C          | 500.perlbench_r(base) 502.gcc_r(base) 505.mcf_r(base, peak)
          | 525.x264_r(base, peak) 557.xz_r(base)
=====

```

```

Intel(R) C Compiler for applications running on Intel(R) 64, Version 2021.1
NextGen Build 20200304
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
=====

```

```

=====
C          | 557.xz_r(peak)
=====

```

```

Intel(R) C Compiler for applications running on Intel(R) 64, Version 2021.1
NextGen Build 20200304
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
icc (NextGen): command line warning #10430: Unsupported command line options
encountered
These options as listed are not supported with the compiler selected.
For more information, use '-qnextgen-diag'.
option list:
-no-prec-div
=====

```

```

=====
C          | 500.perlbench_r(peak)
=====

```

```

Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.1.1.217 Build 20200306
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
icc: NOTE: The evaluation period for this product ends on 30-jul-2020 UTC.
=====

```

```

=====
C          | 502.gcc_r(peak)
=====

```

```

Intel(R) C Compiler for applications running on IA-32, Version 2021.1 NextGen
Build 20200304
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
=====

```

```

=====
C          | 500.perlbench_r(base) 502.gcc_r(base) 505.mcf_r(base, peak)
=====

```

(Continued on next page)



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## Compiler Version Notes (Continued)

| 525.x264\_r(base, peak) 557.xz\_r(base)

-----  
Intel(R) C Compiler for applications running on Intel(R) 64, Version 2021.1  
NextGen Build 20200304  
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.  
-----

=====  
C | 557.xz\_r(peak)

-----  
Intel(R) C Compiler for applications running on Intel(R) 64, Version 2021.1  
NextGen Build 20200304  
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.  
icc (NextGen): command line warning #10430: Unsupported command line options  
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These options as listed are not supported with the compiler selected.  
For more information, use '-qnextgen-diag'.  
option list:  
-no-prec-div  
-----

=====  
C | 500.perlbench\_r(peak)

-----  
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,  
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-----

=====  
C | 502.gcc\_r(peak)

-----  
Intel(R) C Compiler for applications running on IA-32, Version 2021.1 NextGen  
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Copyright (C) 1985-2020 Intel Corporation. All rights reserved.  
-----

=====  
C | 500.perlbench\_r(base) 502.gcc\_r(base) 505.mcf\_r(base, peak)  
| 525.x264\_r(base, peak) 557.xz\_r(base)

-----  
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## Compiler Version Notes (Continued)

=====  
C | 557.xz\_r(peak)  
=====

Intel(R) C Compiler for applications running on Intel(R) 64, Version 2021.1  
NextGen Build 20200304  
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.  
icc (NextGen): command line warning #10430: Unsupported command line options  
encountered  
These options as listed are not supported with the compiler selected.  
For more information, use '-qnextgen-diag'.  
option list:  
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=====

=====  
C | 500.perlbench\_r(peak)  
=====

Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,  
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=====

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C | 502.gcc\_r(peak)  
=====

Intel(R) C Compiler for applications running on IA-32, Version 2021.1 NextGen  
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Copyright (C) 1985-2020 Intel Corporation. All rights reserved.  
=====

=====  
C | 500.perlbench\_r(base) 502.gcc\_r(base) 505.mcf\_r(base, peak)  
| 525.x264\_r(base, peak) 557.xz\_r(base)  
=====

Intel(R) C Compiler for applications running on Intel(R) 64, Version 2021.1  
NextGen Build 20200304  
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.  
=====

=====  
C | 557.xz\_r(peak)  
=====

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## Compiler Version Notes (Continued)

Intel(R) C Compiler for applications running on Intel(R) 64, Version 2021.1  
NextGen Build 20200304

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icc (NextGen): command line warning #10430: Unsupported command line options encountered

These options as listed are not supported with the compiler selected.

For more information, use '-qnextgen-diag'.

option list:

-no-prec-div

=====  
C | 500.perlbench\_r(peak)

=====  
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,  
Version 19.1.1.217 Build 20200306

Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

icc: NOTE: The evaluation period for this product ends on 30-jul-2020 UTC.

=====  
C++ | 520.omnetpp\_r(base, peak) 523.xalancbmk\_r(base, peak)  
| 531.deepsjeng\_r(base, peak) 541.leela\_r(base, peak)

=====  
Intel(R) C++ Compiler for applications running on Intel(R) 64, Version 2021.1  
NextGen Build 20200304

Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

=====  
Fortran | 548.exchange2\_r(base, peak)

=====  
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)  
64, Version 19.1.1.217 Build 20200306

Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

ifort: NOTE: The evaluation period for this product ends on 30-jul-2020 UTC.

## Base Compiler Invocation

C benchmarks:

icc

(Continued on next page)



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## Base Compiler Invocation (Continued)

C++ benchmarks:

icpc

Fortran benchmarks:

ifort

## Base Portability Flags

```
500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -DSPEC_LP64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64
```

## Base Optimization Flags

C benchmarks:

```
-m64 -qnextgen -std=c11
-Wl,-plugin-opt=-x86-branches-within-32B-boundaries -Wl,-z,muldefs
-xCORE-AVX512 -O3 -ffast-math -flto -mfpmath=sse -funroll-loops
-fuse-ld=gold -qopt-mem-layout-trans=4
-L/opt/intel/compilers_and_libraries_2020.1.217/linux/compiler/lib/intel64_lin
-lqkmalloc
```

C++ benchmarks:

```
-m64 -qnextgen -Wl,-plugin-opt=-x86-branches-within-32B-boundaries
-Wl,-z,muldefs -xCORE-AVX512 -O3 -ffast-math -flto -mfpmath=sse
-funroll-loops -fuse-ld=gold -qopt-mem-layout-trans=4
-L/opt/intel/compilers_and_libraries_2020.1.217/linux/compiler/lib/intel64_lin
-lqkmalloc
```

Fortran benchmarks:

```
-m64 -Wl,-plugin-opt=-x86-branches-within-32B-boundaries -Wl,-z,muldefs
-xCORE-AVX512 -O3 -ipo -no-prec-div -qopt-mem-layout-trans=4
-nostandard-realloc-lhs -align array32byte -auto
```

(Continued on next page)



# SPEC CPU®2017 Integer Rate Result

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**Huawei**

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SPECrate®2017\_int\_base = 160

Huawei 2288H V5 (Intel Xeon Silver 4214R)

SPECrate®2017\_int\_peak = 165

**CPU2017 License:** 6177

**Test Sponsor:** China Academy of Information and Communications Technology

**Tested by:** China Academy of Information and Communications Technology

**Test Date:** Jul-2020

**Hardware Availability:** Mar-2020

**Software Availability:** Apr-2020

## Base Optimization Flags (Continued)

Fortran benchmarks (continued):

```
-mbranches-within-32B-boundaries
-L/opt/intel/compilers_and_libraries_2020.1.217/linux/compiler/lib/intel64_lin
-lqkmallocc
```

## Peak Compiler Invocation

C benchmarks:

```
icc
```

C++ benchmarks:

```
icpc
```

Fortran benchmarks:

```
ifort
```

## Peak Portability Flags

```
500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -D_FILE_OFFSET_BITS=64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64
```

## Peak Optimization Flags

C benchmarks:

```
500.perlbench_r: -w1, -z, muldefs -prof-gen(pass 1) -prof-use(pass 2)
-xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -fno-strict-overflow
-mbranches-within-32B-boundaries
```

(Continued on next page)



# SPEC CPU®2017 Integer Rate Result

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SPECrate®2017\_int\_base = 160

SPECrate®2017\_int\_peak = 165

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**Hardware Availability:** Mar-2020

**Software Availability:** Apr-2020

## Peak Optimization Flags (Continued)

500.perlbench\_r (continued):

```
-L/opt/intel/compilers_and_libraries_2020.1.217/linux/compiler/lib/intel64_lin
-lqkmalloc
```

502.gcc\_r: -m32

```
-L/opt/intel/compilers_and_libraries_2020.1.217/linux/compiler/lib/ia32_lin
-std=gnu89
-Wl,-plugin-opt=-x86-branches-within-32B-boundaries
-Wl,-z,muldefs -fprofile-generate(pass 1)
-fprofile-use=default.profddata(pass 2) -xCORE-AVX512 -flto
-Ofast(pass 1) -O3 -ffast-math -qnextgen -fuse-ld=gold
-qopt-mem-layout-trans=4 -L/usr/local/jemalloc32-5.0.1/
-ljemalloc
```

505.mcf\_r: basepeak = yes

525.x264\_r: -m64 -qnextgen -std=c11

```
-Wl,-plugin-opt=-x86-branches-within-32B-boundaries
-Wl,-z,muldefs -xCORE-AVX512 -flto -O3 -ffast-math
-fuse-ld=gold -qopt-mem-layout-trans=4 -fno-alias
-L/opt/intel/compilers_and_libraries_2020.1.217/linux/compiler/lib/intel64_lin
-lqkmalloc
```

557.xz\_r: -m64 -qnextgen -std=c11

```
-Wl,-plugin-opt=-x86-branches-within-32B-boundaries
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/opt/intel/compilers_and_libraries_2020.1.217/linux/compiler/lib/intel64_lin
-lqkmalloc
```

C++ benchmarks:

520.omnetpp\_r: basepeak = yes

523.xalancbmk\_r: basepeak = yes

531.deepsjeng\_r: basepeak = yes

541.leela\_r: basepeak = yes

Fortran benchmarks:

548.exchange2\_r: basepeak = yes



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SPECrate®2017\_int\_peak = 165

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**Test Date:** Jul-2020

**Hardware Availability:** Mar-2020

**Software Availability:** Apr-2020

The flags files that were used to format this result can be browsed at

[http://www.spec.org/cpu2017/flags/Intel-ic19.1u1-official-linux64\\_revB.html](http://www.spec.org/cpu2017/flags/Intel-ic19.1u1-official-linux64_revB.html)

<http://www.spec.org/cpu2017/flags/CAICT-Platform-Settings-V1.0.2020-08-21.html>

You can also download the XML flags sources by saving the following links:

[http://www.spec.org/cpu2017/flags/Intel-ic19.1u1-official-linux64\\_revB.xml](http://www.spec.org/cpu2017/flags/Intel-ic19.1u1-official-linux64_revB.xml)

<http://www.spec.org/cpu2017/flags/CAICT-Platform-Settings-V1.0.2020-08-21.xml>

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