



SPEC CPU®2017 Floating Point Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

Lenovo Global Technology

ThinkSystem ST250
(3.80 GHz, Intel Xeon E-2244G)

SPECrate®2017_fp_base = 33.4

SPECrate®2017_fp_peak = 35.1

CPU2017 License: 9017

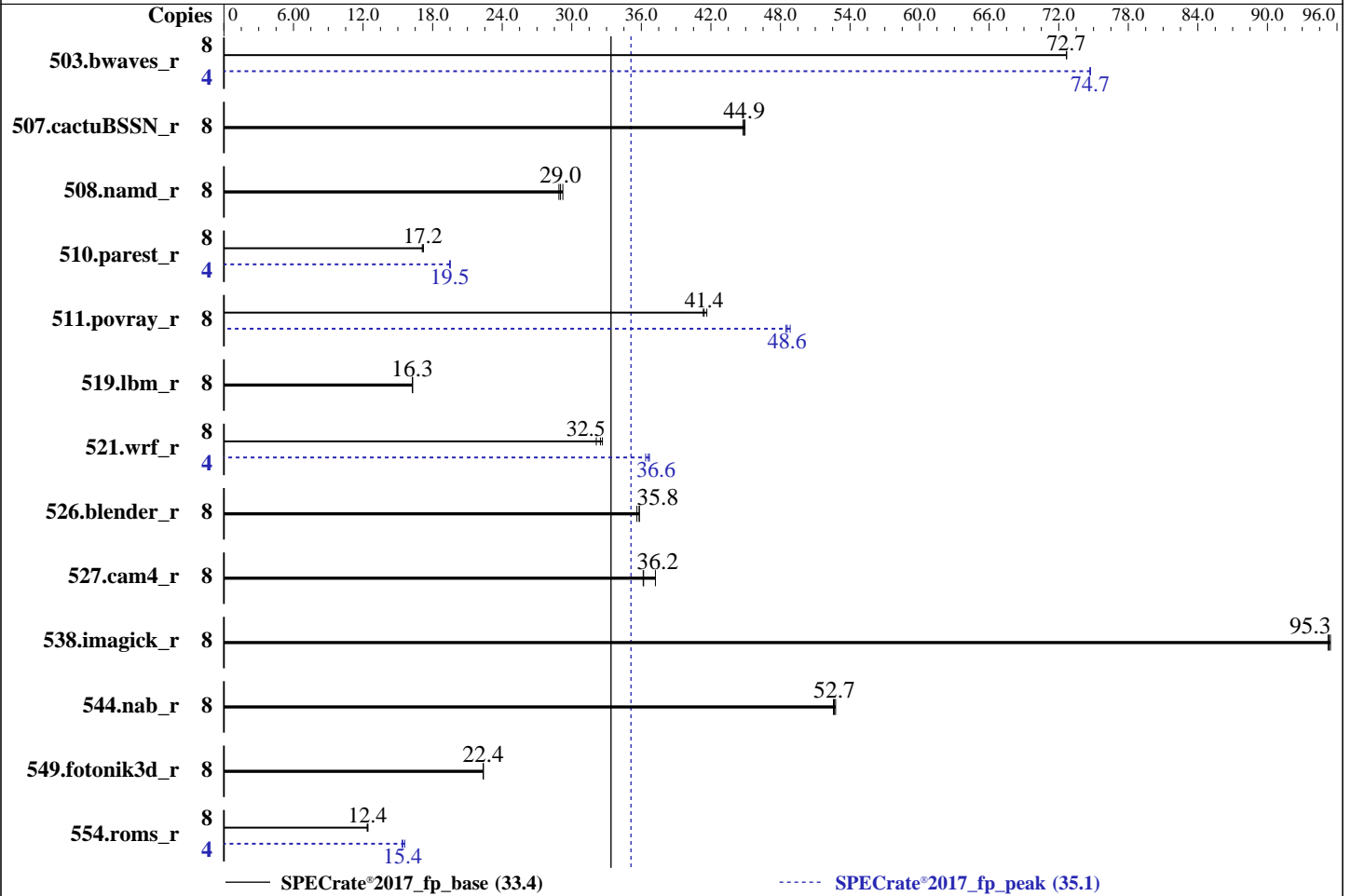
Test Sponsor: Lenovo Global Technology

Tested by: Lenovo Global Technology

Test Date: Jun-2020

Hardware Availability: Mar-2020

Software Availability: Apr-2020



Hardware

CPU Name: Intel Xeon E-2244G
 Max MHz: 4800
 Nominal: 3800
 Enabled: 4 cores, 1 chip, 2 threads/core
 Orderable: 1 chip
 Cache L1: 32 KB I + 32 KB D on chip per core
 L2: 256 KB I+D on chip per core
 L3: 8 MB I+D on chip per chip
 Other: None
 Memory: 128 GB (4 x 32 GB 2Rx4 PC4-2666V-E)
 Storage: 1 x 960 GB SATA SSD
 Other: None

Software

OS: SUSE Linux Enterprise Server 12 SP5 (x86_64)
 Kernel 4.12.14-120-default
 Compiler: C/C++: Version 19.1.1.217 of Intel C/C++
 Compiler for Linux;
 Fortran: Version 19.1.1.217 of Intel Fortran
 Compiler for Linux
 Parallel: No
 Firmware: Lenovo BIOS Version ISE115D 2.10 released Apr-2020
 File System: xfs
 System State: Run level 3 (multi-user)
 Base Pointers: 64-bit
 Peak Pointers: 64-bit
 Other: jemalloc memory allocator V5.0.1
 Power Management: BIOS set to prefer performance at the cost of additional power usage



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Results Table

Benchmark	Base							Peak						
	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
503.bwaves_r	8	1104	72.7	1104	72.7	1104	72.7	4	537	74.7	537	74.7	537	74.7
507.cactuBSSN_r	8	226	44.9	225	44.9	226	44.8	8	226	44.9	225	44.9	226	44.8
508.namd_r	8	263	28.9	262	29.0	260	29.2	8	263	28.9	262	29.0	260	29.2
510.parest_r	8	1216	17.2	1223	17.1	1219	17.2	4	536	19.5	537	19.5	537	19.5
511.povray_r	8	451	41.4	452	41.3	448	41.7	8	385	48.6	385	48.5	382	48.8
519.lbm_r	8	519	16.3	519	16.3	518	16.3	8	519	16.3	519	16.3	518	16.3
521.wrf_r	8	549	32.6	552	32.5	558	32.1	4	245	36.6	244	36.7	246	36.4
526.blender_r	8	340	35.8	342	35.6	340	35.8	8	340	35.8	342	35.6	340	35.8
527.cam4_r	8	387	36.2	387	36.2	376	37.2	8	387	36.2	387	36.2	376	37.2
538.imagick_r	8	208	95.4	209	95.3	209	95.2	8	208	95.4	209	95.3	209	95.2
544.nab_r	8	256	52.6	255	52.8	256	52.7	8	256	52.6	255	52.8	256	52.7
549.fotonik3d_r	8	1394	22.4	1394	22.4	1394	22.4	8	1394	22.4	1394	22.4	1394	22.4
554.roms_r	8	1023	12.4	1028	12.4	1027	12.4	4	408	15.6	412	15.4	414	15.4

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Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Compiler Notes

The inconsistent Compiler version information under Compiler Version section is due to a discrepancy in Intel Compiler. The correct version of C/C++ compiler is: Version 19.1.1.217 Build 20200306 Compiler for Linux. The correct version of Fortran compiler is: Version 19.1.1.217 Build 20200306 Compiler for Linux.

Submit Notes

The taskset mechanism was used to bind copies to processors. The config file option 'submit' was used to generate taskset commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

Environment Variables Notes

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH =
"/home/cpu2017-1.1.0-ic19.1.1/lib/intel64:/home/cpu2017-1.1.0-ic19.1.1/j
e5.0.1-64"
MALLOC_CONF = "retain:true"



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General Notes

Binaries compiled on a system with 1x Intel Core i9-7980XE CPU + 64GB RAM memory using Redhat Enterprise Linux 8.0
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3> /proc/sys/vm/drop_caches
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.
jemalloc, a general purpose malloc implementation built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5 sources available from jemalloc.net or <https://github.com/jemalloc/jemalloc/releases>

Platform Notes

BIOS configuration:
Choose Operating Mode set to Maximum Performance

Sysinfo program /home/cpu2017-1.1.0-ic19.1.1/bin/sysinfo
Rev: r6365 of 2019-08-21 295195f888a3d7edble6e46a485a0011
running on linux-tzna Wed Jun 24 06:16:50 2020

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
<https://www.spec.org/cpu2017/Docs/config.html#sysinfo>

From /proc/cpuinfo
model name : Intel(R) Xeon(R) E-2244G CPU @ 3.80GHz
1 "physical id"s (chips)
8 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 4
siblings : 8
physical 0: cores 0 1 2 3

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
Address sizes: 39 bits physical, 48 bits virtual
CPU(s): 8
On-line CPU(s) list: 0-7

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Platform Notes (Continued)

```

Thread(s) per core: 2
Core(s) per socket: 4
Socket(s): 1
NUMA node(s): 1
Vendor ID: GenuineIntel
CPU family: 6
Model: 158
Model name: Intel(R) Xeon(R) E-2244G CPU @ 3.80GHz
Stepping: 10
CPU MHz: 3800.000
CPU max MHz: 4800.0000
CPU min MHz: 800.0000
BogoMIPS: 7584.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 256K
L3 cache: 8192K
NUMA node0 CPU(s): 0-7
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
aperfmpperf tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3
sdbg fma cx16 xtpr pdcm pcid sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer
aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb invpcid_single
pti ssbd ibrs ibpb stibp tpr_shadow vnmi flexpriority ept vpid fsgsbase tsc_adjust
bmi1 hle avx2 smep bmi2 erms invpcid rtm mpx rdseed adx smap clflushopt intel_pt
xsaveopt xsavec xgetbv1 xsaves dtherm ida arat pln pts hwp hwp_notify hwp_act_window
hwp_epp md_clear flush_l1d

```

```

/proc/cpuinfo cache data
cache size : 8192 KB

```

```

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a
physical chip.

```

```

available: 1 nodes (0)
node 0 cpus: 0 1 2 3 4 5 6 7
node 0 size: 128866 MB
node 0 free: 128349 MB
node distances:
node 0
0: 10

```

```

From /proc/meminfo
MemTotal: 131959308 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

```

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Platform Notes (Continued)

```

From /etc/*release* /etc/*version*
SuSE-release:
    SUSE Linux Enterprise Server 12 (x86_64)
    VERSION = 12
    PATCHLEVEL = 5
    # This file is deprecated and will be removed in a future service pack or release.
    # Please check /etc/os-release for details about this release.
os-release:
    NAME="SLES"
    VERSION="12-SP5"
    VERSION_ID="12.5"
    PRETTY_NAME="SUSE Linux Enterprise Server 12 SP5"
    ID="sles"
    ANSI_COLOR="0;32"
    CPE_NAME="cpe:/o:suse:sles:12:sp5"

uname -a:
    Linux linux-tzna 4.12.14-120-default #1 SMP Thu Nov 7 16:39:09 UTC 2019 (fd9dc36)
    x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

itlb_multihit:           KVM: Mitigation: Split huge pages
CVE-2018-3620 (L1 Terminal Fault): Mitigation: PTE Inversion; VMX: conditional
                             cache flushes, SMT vulnerable
Microarchitectural Data Sampling: Mitigation: Clear CPU buffers; SMT vulnerable
CVE-2017-5754 (Meltdown):      Mitigation: PTI
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled
                             via prctl and seccomp
CVE-2017-5753 (Spectre variant 1): Mitigation: usercopy/swaps barriers and __user
                             pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Full generic retpoline, IBPB:
                             conditional, IBRS_FW, STIBP: conditional, RSB
                             filling
tsx_async_abort:           Mitigation: Clear CPU buffers; SMT vulnerable

run-level 3 Jun 24 06:15

SPEC is set to: /home/cpu2017-1.1.0-ic19.1.1
Filesystem      Type  Size  Used Avail Use% Mounted on
/dev/sdb3       xfs   893G   64G  829G   8% /

From /sys/devices/virtual/dmi/id
BIOS:      Lenovo  -[ISE115D-2.10]- 04/24/2020
Vendor:    Lenovo
Product:   ThinkSystem ST250  -[7Y45CTO0WW]-

```

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Platform Notes (Continued)

Product Family: ThinkSystem
Serial: 1234567890

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

Memory:
4x SK Hynix HMAA4GU7AJR8N-VK 32767 MB 2 rank 2666

(End of data from sysinfo program)

Compiler Version Notes

```
=====
C                | 519.lbm_r(base, peak) 538.imagick_r(base, peak)
                  | 544.nab_r(base, peak)
-----
```

```
Intel(R) C Compiler for applications running on Intel(R) 64, Version 2021.1
NextGen Build 20200304
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
-----
```

```
=====
C++              | 508.namd_r(base, peak) 510.parest_r(base, peak)
-----
```

```
Intel(R) C++ Compiler for applications running on Intel(R) 64, Version 2021.1
NextGen Build 20200304
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
-----
```

```
=====
C++, C           | 511.povray_r(base) 526.blender_r(base, peak)
-----
```

```
Intel(R) C++ Compiler for applications running on Intel(R) 64, Version 2021.1
NextGen Build 20200304
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Intel(R) C Compiler for applications running on Intel(R) 64, Version 2021.1
NextGen Build 20200304
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
-----
```

```
=====
C++, C           | 511.povray_r(peak)
-----
```

```
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
```

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Compiler Version Notes (Continued)

Version 19.1.1.217 Build 20200306
 Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
 Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
 Version 19.1.1.217 Build 20200306
 Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

=====
 C++, C | 511.povray_r(base) 526.blender_r(base, peak)
 =====

Intel(R) C++ Compiler for applications running on Intel(R) 64, Version 2021.1
 NextGen Build 20200304
 Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
 Intel(R) C Compiler for applications running on Intel(R) 64, Version 2021.1
 NextGen Build 20200304
 Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

=====
 C++, C | 511.povray_r(peak)
 =====

Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
 Version 19.1.1.217 Build 20200306
 Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
 Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
 Version 19.1.1.217 Build 20200306
 Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

=====
 C++, C, Fortran | 507.cactuBSSN_r(base, peak)
 =====

Intel(R) C++ Compiler for applications running on Intel(R) 64, Version 2021.1
 NextGen Build 20200304
 Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
 Intel(R) C Compiler for applications running on Intel(R) 64, Version 2021.1
 NextGen Build 20200304
 Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
 Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
 64, Version 19.1.1.217 Build 20200306
 Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

=====
 Fortran | 503.bwaves_r(base, peak) 549.fotonik3d_r(base, peak)
 | 554.roms_r(base, peak)
 =====

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Compiler Version Notes (Continued)

Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.1.1.217 Build 20200306
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

=====
Fortran, C | 521.wrf_r(base) 527.cam4_r(base, peak)

Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.1.1.217 Build 20200306
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Intel(R) C Compiler for applications running on Intel(R) 64, Version 2021.1 NextGen Build 20200304
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

=====
Fortran, C | 521.wrf_r(peak)

Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.1.1.217 Build 20200306
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.1.1.217 Build 20200306
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

=====
Fortran, C | 521.wrf_r(base) 527.cam4_r(base, peak)

Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.1.1.217 Build 20200306
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Intel(R) C Compiler for applications running on Intel(R) 64, Version 2021.1 NextGen Build 20200304
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

=====
Fortran, C | 521.wrf_r(peak)

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Compiler Version Notes (Continued)

Base Compiler Invocation

C benchmarks:

icc

C++ benchmarks:

icpc

Fortran benchmarks:

ifort

Benchmarks using both Fortran and C:

ifort icc

Benchmarks using both C and C++:

icpc icc

Benchmarks using Fortran, C, and C++:

icpc icc ifort

Base Portability Flags

503.bwaves_r: -DSPEC_LP64

507.cactuBSSN_r: -DSPEC_LP64

508.namd_r: -DSPEC_LP64

510.parest_r: -DSPEC_LP64

511.povray_r: -DSPEC_LP64

519.lbm_r: -DSPEC_LP64

521.wrf_r: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian

526.blender_r: -DSPEC_LP64 -DSPEC_LINUX -funsigned-char

527.cam4_r: -DSPEC_LP64 -DSPEC_CASE_FLAG

538.imagick_r: -DSPEC_LP64

544.nab_r: -DSPEC_LP64

549.fotonik3d_r: -DSPEC_LP64

554.roms_r: -DSPEC_LP64



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Base Optimization Flags

C benchmarks:

```
-m64 -qnextgen -std=c11
-Wl,-plugin-opt=-x86-branches-within-32B-boundaries -Wl,-z,muldefs
-fuse-ld=gold -xCORE-AVX2 -Ofast -ffast-math -flto -mfpmath=sse
-funroll-loops -qopt-mem-layout-trans=4
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc
```

C++ benchmarks:

```
-m64 -qnextgen -Wl,-plugin-opt=-x86-branches-within-32B-boundaries
-Wl,-z,muldefs -fuse-ld=gold -xCORE-AVX2 -Ofast -ffast-math -flto
-mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc
```

Fortran benchmarks:

```
-m64 -Wl,-plugin-opt=-x86-branches-within-32B-boundaries -Wl,-z,muldefs
-fuse-ld=gold -xCORE-AVX2 -O3 -ipo -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-multiple-gather-scatter-by-shuffles
-qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte
-auto -mbranches-within-32B-boundaries
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc
```

Benchmarks using both Fortran and C:

```
-m64 -qnextgen -std=c11
-Wl,-plugin-opt=-x86-branches-within-32B-boundaries -Wl,-z,muldefs
-fuse-ld=gold -xCORE-AVX2 -Ofast -ffast-math -flto -mfpmath=sse
-funroll-loops -qopt-mem-layout-trans=4 -O3 -ipo -no-prec-div
-qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles -nostandard-realloc-lhs
-align array32byte -auto -mbranches-within-32B-boundaries
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc
```

Benchmarks using both C and C++:

```
-m64 -qnextgen -std=c11
-Wl,-plugin-opt=-x86-branches-within-32B-boundaries -Wl,-z,muldefs
-fuse-ld=gold -xCORE-AVX2 -Ofast -ffast-math -flto -mfpmath=sse
-funroll-loops -qopt-mem-layout-trans=4
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc
```

Benchmarks using Fortran, C, and C++:

```
-m64 -qnextgen -std=c11
-Wl,-plugin-opt=-x86-branches-within-32B-boundaries -Wl,-z,muldefs
-fuse-ld=gold -xCORE-AVX2 -Ofast -ffast-math -flto -mfpmath=sse
-funroll-loops -qopt-mem-layout-trans=4 -O3 -ipo -no-prec-div
-qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles -nostandard-realloc-lhs
-align array32byte -auto -mbranches-within-32B-boundaries
```

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Base Optimization Flags (Continued)

Benchmarks using Fortran, C, and C++ (continued):

-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

Peak Compiler Invocation

C benchmarks:

icc

C++ benchmarks:

icpc

Fortran benchmarks:

ifort

Benchmarks using both Fortran and C:

ifort icc

Benchmarks using both C and C++:

icpc icc

Benchmarks using Fortran, C, and C++:

icpc icc ifort

Peak Portability Flags

Same as Base Portability Flags

Peak Optimization Flags

C benchmarks:

519.lbm_r: basepeak = yes

538.imagick_r: basepeak = yes

544.nab_r: basepeak = yes

C++ benchmarks:

(Continued on next page)



SPEC CPU®2017 Floating Point Rate Result

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SPECrate®2017_fp_base = 33.4

ThinkSystem ST250
(3.80 GHz, Intel Xeon E-2244G)

SPECrate®2017_fp_peak = 35.1

CPU2017 License: 9017

Test Sponsor: Lenovo Global Technology

Tested by: Lenovo Global Technology

Test Date: Jun-2020

Hardware Availability: Mar-2020

Software Availability: Apr-2020

Peak Optimization Flags (Continued)

508.namd_r: basepeak = yes

510.parest_r: -m64 -qnextgen

```
-Wl,-plugin-opt=-x86-branches-within-32B-boundaries  
-Wl,-z,muldefs -fuse-ld=gold -xCORE-AVX2 -Ofast  
-ffast-math -flto -mfpmath=sse -funroll-loops  
-qopt-mem-layout-trans=4 -L/usr/local/jemalloc64-5.0.1/lib  
-ljemalloc
```

Fortran benchmarks:

```
503.bwaves_r: -m64 -Wl,-plugin-opt=-x86-branches-within-32B-boundaries  
-Wl,-z,muldefs -fuse-ld=gold -xCORE-AVX2 -O3 -ipo  
-no-prec-div -qopt-prefetch -ffinite-math-only  
-qopt-multiple-gather-scatter-by-shuffles  
-qopt-mem-layout-trans=4 -nostandard-realloc-lhs  
-align array32byte -auto -mbranches-within-32B-boundaries  
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc
```

549.fotonik3d_r: basepeak = yes

554.roms_r: Same as 503.bwaves_r

Benchmarks using both Fortran and C:

```
521.wrf_r: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX2 -O3 -ipo  
-no-prec-div -qopt-prefetch -ffinite-math-only  
-qopt-multiple-gather-scatter-by-shuffles  
-qopt-mem-layout-trans=4 -mbranches-within-32B-boundaries  
-nostandard-realloc-lhs -align array32byte -auto  
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc
```

527.cam4_r: basepeak = yes

Benchmarks using both C and C++:

```
511.povray_r: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX2 -O3 -ipo  
-no-prec-div -qopt-prefetch -ffinite-math-only  
-qopt-multiple-gather-scatter-by-shuffles  
-qopt-mem-layout-trans=4 -mbranches-within-32B-boundaries  
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc
```

526.blender_r: basepeak = yes

Benchmarks using Fortran, C, and C++:

(Continued on next page)



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Peak Optimization Flags (Continued)

507.cactuBSSN_r: basepeak = yes

The flags files that were used to format this result can be browsed at

http://www.spec.org/cpu2017/flags/Intel-ic19.1ul-official-linux64_revA.html

<http://www.spec.org/cpu2017/flags/Lenovo-Platform-SPECcpu2017-Flags-V1.2-SKL-J.html>

You can also download the XML flags sources by saving the following links:

http://www.spec.org/cpu2017/flags/Intel-ic19.1ul-official-linux64_revA.xml

<http://www.spec.org/cpu2017/flags/Lenovo-Platform-SPECcpu2017-Flags-V1.2-SKL-J.xml>

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