



# SPEC CPU®2017 Floating Point Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

## Dell Inc.

SPECrate®2017\_fp\_base = 117

PowerEdge R440 (Intel Xeon Gold 5217, 3.00 GHz)

SPECrate®2017\_fp\_peak = 121

CPU2017 License: 55

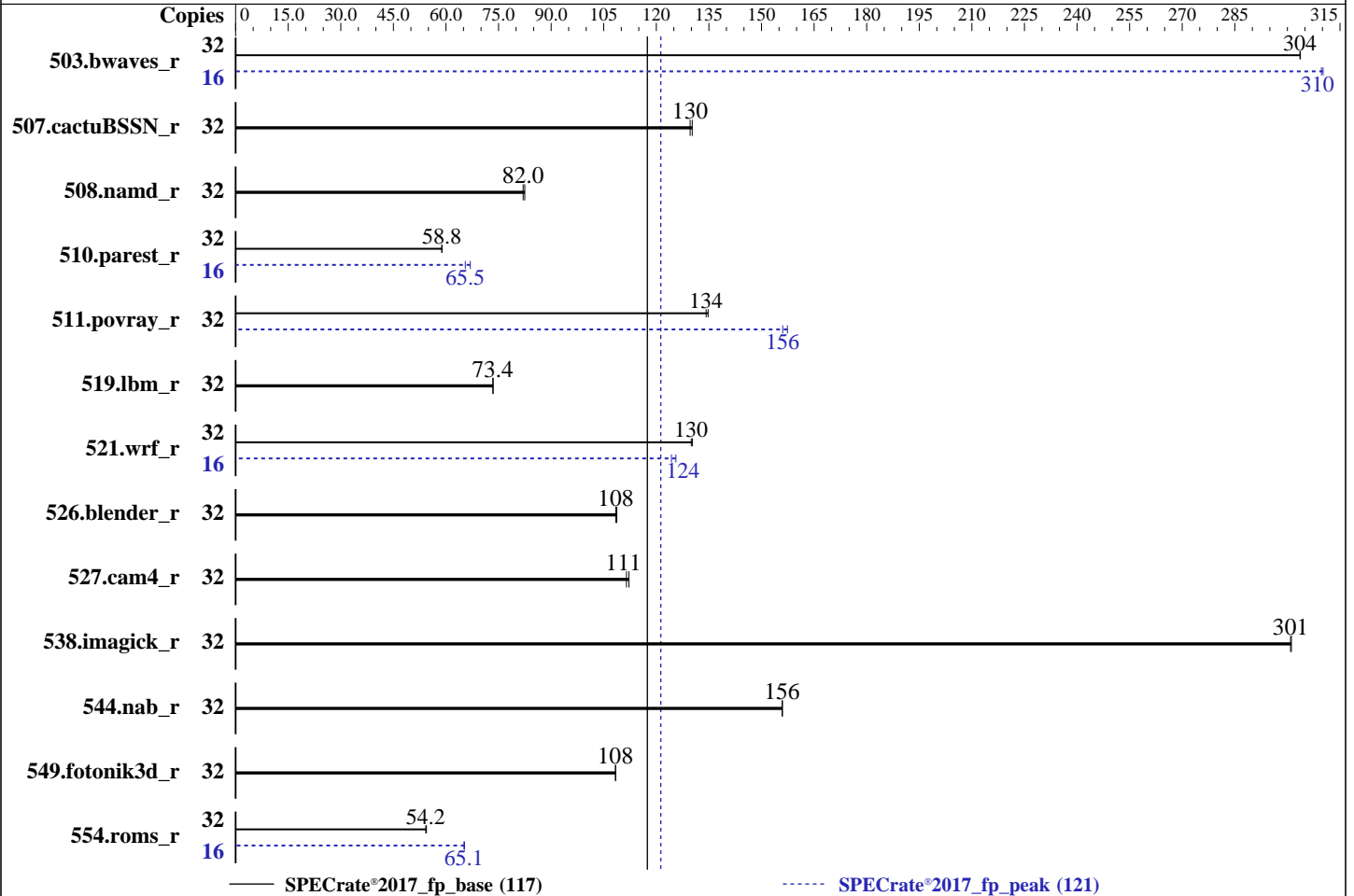
Test Date: Apr-2020

Test Sponsor: Dell Inc.

Hardware Availability: Feb-2020

Tested by: Dell Inc.

Software Availability: Apr-2020



### Hardware

CPU Name: Intel Xeon Gold 5217  
 Max MHz: 3700  
 Nominal: 3000  
 Enabled: 32 cores, 2 chips  
 Orderable: 1,2 chips  
 Cache L1: 32 KB I + 32 KB D on chip per core  
 L2: 1 MB I+D on chip per core  
 L3: 11 MB I+D on chip per chip  
 Other: None  
 Memory: 384 GB (12 x 32 GB 2Rx8 PC4-3200V-R, running at 2933)  
 Storage: 1 x 1.92 TB SATA SSD  
 Other: None

### Software

OS: Red Hat Enterprise Linux 8.1  
 kernel 4.18.0-147.el8.x86\_64  
 Compiler: C/C++: Version 19.1.1.217 of Intel C/C++ Compiler for Linux;  
 Fortran: Version 19.1.1.217 of Intel Fortran Compiler for Linux  
 Parallel: No  
 Firmware: Version 2.7.7 released May-2020  
 File System: xfs  
 System State: Run level 3 (multi-user)  
 Base Pointers: 64-bit  
 Peak Pointers: 64-bit  
 Other: None  
 jemalloc memory allocator V5.0.1  
 Power Management: BIOS set to prefer performance at the cost of additional power usage.



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## Results Table

Benchmark	Base							Peak						
	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
503.bwaves_r	32	<b><u>1057</u></b>	<b><u>304</u></b>	1057	304			16	517	310	<b><u>518</u></b>	<b><u>310</u></b>		
507.cactuBSSN_r	32	311	130	<b><u>312</u></b>	<b><u>130</u></b>			32	311	130	<b><u>312</u></b>	<b><u>130</u></b>		
508.namd_r	32	<b><u>371</u></b>	<b><u>82.0</u></b>	369	82.5			32	<b><u>371</u></b>	<b><u>82.0</u></b>	369	82.5		
510.parest_r	32	<b><u>1424</u></b>	<b><u>58.8</u></b>	1422	58.9			16	625	66.9	<b><u>639</u></b>	<b><u>65.5</u></b>		
511.povray_r	32	554	135	<b><u>557</u></b>	<b><u>134</u></b>			32	<b><u>479</u></b>	<b><u>156</u></b>	475	157		
519.lbm_r	32	<b><u>460</u></b>	<b><u>73.4</u></b>	459	73.5			32	<b><u>460</u></b>	<b><u>73.4</u></b>	459	73.5		
521.wrf_r	32	550	130	<b><u>552</u></b>	<b><u>130</u></b>			16	285	126	<b><u>288</u></b>	<b><u>124</u></b>		
526.blender_r	32	448	109	<b><u>450</u></b>	<b><u>108</u></b>			32	448	109	<b><u>450</u></b>	<b><u>108</u></b>		
527.cam4_r	32	499	112	<b><u>502</u></b>	<b><u>111</u></b>			32	499	112	<b><u>502</u></b>	<b><u>111</u></b>		
538.imagick_r	32	<b><u>264</u></b>	<b><u>301</u></b>	264	301			32	<b><u>264</u></b>	<b><u>301</u></b>	264	301		
544.nab_r	32	345	156	<b><u>346</u></b>	<b><u>156</u></b>			32	345	156	<b><u>346</u></b>	<b><u>156</u></b>		
549.fotonik3d_r	32	1150	108	<b><u>1151</u></b>	<b><u>108</u></b>			32	1150	108	<b><u>1151</u></b>	<b><u>108</u></b>		
554.roms_r	32	934	54.4	<b><u>937</u></b>	<b><u>54.2</u></b>			16	389	65.3	<b><u>390</u></b>	<b><u>65.1</u></b>		

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Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

## Compiler Notes

The inconsistent Compiler version information under Compiler Version section is due to a discrepancy in Intel Compiler. The correct version of C/C++ compiler is: Version 19.1.1.217 Build 20200306 Compiler for Linux  
The correct version of Fortran compiler is: Version 19.1.1.217 Build 20200306 Compiler for Linux

## Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

## Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

## Environment Variables Notes

Environment variables set by runcpu before the start of the run:  
LD\_LIBRARY\_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-64"  
MALLOCONF = "retain:true"



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## General Notes

Binaries compiled on a system with 1x Intel Core i9-9900K CPU + 64GB RAM memory using Redhat Enterprise Linux 8.0

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

Transparent Huge Pages enabled by default

Prior to runcpu invocation

Filesystem page cache synced and cleared with:

```
sync; echo 3> /proc/sys/vm/drop_caches
```

runcpu command invoked through numactl i.e.:

```
numactl --interleave=all runcpu <etc>
```

jemalloc, a general purpose malloc implementation

built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5

sources available from jemalloc.net or <https://github.com/jemalloc/jemalloc/releases>

## Platform Notes

BIOS settings:

Virtualization Technology disabled

System Profile set to Custom

CPU Performance set to Maximum Performance

C States set to Autonomous

C1E disabled

Uncore Frequency set to Dynamic

Energy Efficiency Policy set to Performance

Memory Patrol Scrub set to standard

Logical Processor disabled

CPU Interconnect Bus Link Power Management disabled

PCI ASPM L1 Link Power Management disabled

UPI Prefetch enabled

LLC Prefetch disabled

Dead Line LLC Alloc enabled

Directory AtoS disabled

Sysinfo program /home/cpu2017/bin/sysinfo

Rev: r6365 of 2019-08-21 295195f888a3d7edble6e46a485a0011

running on localhost.localdomain Tue Jun 2 14:19:50 2020

SUT (System Under Test) info as seen by some common utilities.

For more information on this section, see

<https://www.spec.org/cpu2017/Docs/config.html#sysinfo>

From /proc/cpuinfo

(Continued on next page)



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## Platform Notes (Continued)

```

model name : Intel(R) Xeon(R) Gold 5217 CPU @ 3.00GHz
  2 "physical id"s (chips)
  32 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following
excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
  cpu cores : 8
  siblings  : 16
  physical 0: cores 0 1 2 3 4 5 6 7
  physical 1: cores 0 1 2 3 4 5 6 7

```

From lscpu:

```

Architecture:          x86_64
CPU op-mode(s):        32-bit, 64-bit
Byte Order:            Little Endian
CPU(s):                32
On-line CPU(s) list:  0-31
Thread(s) per core:    2
Core(s) per socket:    8
Socket(s):              2
NUMA node(s):          2
Vendor ID:              GenuineIntel
CPU family:             6
Model:                  85
Model name:             Intel(R) Xeon(R) Gold 5217 CPU @ 3.00GHz
Stepping:               6
CPU MHz:                1200.055
CPU max MHz:           3700.0000
CPU min MHz:           1200.0000
BogoMIPS:               6000.00
Virtualization:        VT-x
L1d cache:             32K
L1i cache:             32K
L2 cache:              1024K
L3 cache:              11264K
NUMA node0 CPU(s):    0,2,4,6,8,10,12,14,16,18,20,22,24,26,28,30
NUMA node1 CPU(s):    1,3,5,7,9,11,13,15,17,19,21,23,25,27,29,31
Flags:                  fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
aperfmpperf pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16
xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave
avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_l3 cdp_l3
invpcid_single intel_ppin ssbd mba ibrs ibpb stibp ibrs_enhanced tpr_shadow vnmi
flexpriority ept vpid fsgsbase tsc_adjust bmil hle avx2 smep bmi2 erms invpcid rtm
cqm mpx rdt_a avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd
avx512bw avx512vl xsaveopt xsavec xgetbv1 xsaves cqm_llc cqm_occup_llc cqm_mbm_total
cqm_mbm_local dtherm ida arat pln pts pku ospke avx512_vnni md_clear flush_l1d

```

(Continued on next page)



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## Platform Notes (Continued)

arch\_capabilities

/proc/cpuinfo cache data  
cache size : 11264 KB

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.

```
available: 2 nodes (0-1)
node 0 cpus: 0 2 4 6 8 10 12 14 16 18 20 22 24 26 28 30
node 0 size: 192074 MB
node 0 free: 190767 MB
node 1 cpus: 1 3 5 7 9 11 13 15 17 19 21 23 25 27 29 31
node 1 size: 193506 MB
node 1 free: 192207 MB
node distances:
node 0 1
  0: 10 21
  1: 21 10
```

From /proc/meminfo  
MemTotal: 394835328 kB  
HugePages\_Total: 0  
Hugepagesize: 2048 kB

From /etc/\*release\* /etc/\*version\*  
os-release:  
NAME="Red Hat Enterprise Linux"  
VERSION="8.1 (Ootpa)"  
ID="rhel"  
ID\_LIKE="fedora"  
VERSION\_ID="8.1"  
PLATFORM\_ID="platform:el8"  
PRETTY\_NAME="Red Hat Enterprise Linux 8.1 (Ootpa)"  
ANSI\_COLOR="0;31"  
redhat-release: Red Hat Enterprise Linux release 8.1 (Ootpa)  
system-release: Red Hat Enterprise Linux release 8.1 (Ootpa)  
system-release-cpe: cpe:/o:redhat:enterprise\_linux:8.1:ga

uname -a:  
Linux localhost.localdomain 4.18.0-147.el8.x86\_64 #1 SMP Thu Sep 26 15:52:44 UTC 2019  
x86\_64 x86\_64 x86\_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2018-3620 (L1 Terminal Fault): Not affected  
Microarchitectural Data Sampling: Not affected  
CVE-2017-5754 (Meltdown): Not affected

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## Platform Notes (Continued)

CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled via prctl and seccomp

CVE-2017-5753 (Spectre variant 1): Mitigation: usercopy/swaps barriers and \_\_user pointer sanitization

CVE-2017-5715 (Spectre variant 2): Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling

run-level 3 Jun 2 09:18 last=5

SPEC is set to: /home/cpu2017

Filesystem	Type	Size	Used	Avail	Use%	Mounted on
/dev/mapper/rhel-home	xfs	1.7T	23G	1.7T	2%	/home

From /sys/devices/virtual/dmi/id

BIOS: Dell Inc. 2.7.7 05/06/2020

Vendor: Dell Inc.

Product: PowerEdge R440

Product Family: PowerEdge

Serial: F9TD613

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

Memory:

12x 002C069D002C 36ASF4G72PZ-3G2E2 32 GB 2 rank 3200

4x Not Specified Not Specified

(End of data from sysinfo program)

## Compiler Version Notes

```
=====
C          | 519.lbm_r(base, peak) 538.imagick_r(base, peak)
          | 544.nab_r(base, peak)
-----
```

Intel(R) C Compiler for applications running on Intel(R) 64, Version 2021.1

NextGen Build 20200304

Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

```
=====
C++       | 508.namd_r(base, peak) 510.parest_r(base, peak)
-----
```

Intel(R) C++ Compiler for applications running on Intel(R) 64, Version 2021.1

NextGen Build 20200304

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## Compiler Version Notes (Continued)

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=====  
C++, C | 511.povray\_r(base) 526.blender\_r(base, peak)  
=====

Intel(R) C++ Compiler for applications running on Intel(R) 64, Version 2021.1  
NextGen Build 20200304

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Intel(R) C Compiler for applications running on Intel(R) 64, Version 2021.1  
NextGen Build 20200304

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=====  
C++, C | 511.povray\_r(peak)  
=====

Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,  
Version 19.1.1.217 Build 20200306

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Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,  
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=====  
C++, C | 511.povray\_r(base) 526.blender\_r(base, peak)  
=====

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=====  
C++, C | 511.povray\_r(peak)  
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## Compiler Version Notes (Continued)

=====  
C++, C, Fortran | 507.cactuBSSN\_r(base, peak)  
-----

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NextGen Build 20200304

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Intel(R) C Compiler for applications running on Intel(R) 64, Version 2021.1  
NextGen Build 20200304

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Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)  
64, Version 19.1.1.217 Build 20200306

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-----

=====  
Fortran | 503.bwaves\_r(base, peak) 549.fotonik3d\_r(base, peak)  
554.roms\_r(base, peak)

Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)  
64, Version 19.1.1.217 Build 20200306

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-----

=====  
Fortran, C | 521.wrf\_r(base) 527.cam4\_r(base, peak)  
-----

Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)  
64, Version 19.1.1.217 Build 20200306

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Intel(R) C Compiler for applications running on Intel(R) 64, Version 2021.1  
NextGen Build 20200304

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-----

=====  
Fortran, C | 521.wrf\_r(peak)  
-----

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Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,  
Version 19.1.1.217 Build 20200306

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-----

=====  
Fortran, C | 521.wrf\_r(base) 527.cam4\_r(base, peak)  
-----

(Continued on next page)





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## Compiler Version Notes (Continued)

```
-----
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
 64, Version 19.1.1.217 Build 20200306
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Intel(R) C Compiler for applications running on Intel(R) 64, Version 2021.1
  NextGen Build 20200304
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
-----
```

```
=====
Fortran, C      | 521.wrf_r(peak)
-----
```

```
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
 64, Version 19.1.1.217 Build 20200306
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
  Version 19.1.1.217 Build 20200306
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
-----
```

## Base Compiler Invocation

C benchmarks:

icc

C++ benchmarks:

icpc

Fortran benchmarks:

ifort

Benchmarks using both Fortran and C:

ifort icc

Benchmarks using both C and C++:

icpc icc

Benchmarks using Fortran, C, and C++:

icpc icc ifort

## Base Portability Flags

503.bwaves\_r: -DSPEC\_LP64

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## Base Portability Flags (Continued)

```

507.cactuBSSN_r: -DSPEC_LP64
508.namd_r: -DSPEC_LP64
510.parest_r: -DSPEC_LP64
511.povray_r: -DSPEC_LP64
519.lbm_r: -DSPEC_LP64
521.wrf_r: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
526.blender_r: -DSPEC_LP64 -DSPEC_LINUX -funsigned-char
527.cam4_r: -DSPEC_LP64 -DSPEC_CASE_FLAG
538.imagick_r: -DSPEC_LP64
544.nab_r: -DSPEC_LP64
549.fotonik3d_r: -DSPEC_LP64
554.roms_r: -DSPEC_LP64

```

## Base Optimization Flags

### C benchmarks:

```

-m64 -qnextgen -std=c11
-Wl,-plugin-opt=-x86-branches-within-32B-boundaries -Wl,-z,muldefs
-fuse-ld=gold -xCORE-AVX2 -Ofast -ffast-math -flto -mfpmath=sse
-funroll-loops -qopt-mem-layout-trans=4
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

```

### C++ benchmarks:

```

-m64 -qnextgen -Wl,-plugin-opt=-x86-branches-within-32B-boundaries
-Wl,-z,muldefs -fuse-ld=gold -xCORE-AVX2 -Ofast -ffast-math -flto
-mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

```

### Fortran benchmarks:

```

-m64 -Wl,-plugin-opt=-x86-branches-within-32B-boundaries -Wl,-z,muldefs
-fuse-ld=gold -xCORE-AVX2 -O3 -ipo -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-multiple-gather-scatter-by-shuffles
-qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte
-auto -mbranches-within-32B-boundaries
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

```

### Benchmarks using both Fortran and C:

```

-m64 -qnextgen -std=c11
-Wl,-plugin-opt=-x86-branches-within-32B-boundaries -Wl,-z,muldefs
-fuse-ld=gold -xCORE-AVX2 -Ofast -ffast-math -flto -mfpmath=sse
-funroll-loops -qopt-mem-layout-trans=4 -O3 -ipo -no-prec-div
-qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles -nostandard-realloc-lhs
-align array32byte -auto -mbranches-within-32B-boundaries

```

(Continued on next page)



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Hardware Availability: Feb-2020

Software Availability: Apr-2020

## Base Optimization Flags (Continued)

Benchmarks using both Fortran and C (continued):

```
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc
```

Benchmarks using both C and C++:

```
-m64 -qnextgen -std=c11
-Wl,-plugin-opt=-x86-branches-within-32B-boundaries -Wl,-z,muldefs
-fuse-ld=gold -xCORE-AVX2 -Ofast -ffast-math -flto -mfpmath=sse
-funroll-loops -qopt-mem-layout-trans=4
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc
```

Benchmarks using Fortran, C, and C++:

```
-m64 -qnextgen -std=c11
-Wl,-plugin-opt=-x86-branches-within-32B-boundaries -Wl,-z,muldefs
-fuse-ld=gold -xCORE-AVX2 -Ofast -ffast-math -flto -mfpmath=sse
-funroll-loops -qopt-mem-layout-trans=4 -O3 -ipo -no-prec-div
-qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles -nostandard-realloc-lhs
-align array32byte -auto -mbranches-within-32B-boundaries
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc
```

## Peak Compiler Invocation

C benchmarks:

```
icc
```

C++ benchmarks:

```
icpc
```

Fortran benchmarks:

```
ifort
```

Benchmarks using both Fortran and C:

```
ifort icc
```

Benchmarks using both C and C++:

```
icpc icc
```

Benchmarks using Fortran, C, and C++:

```
icpc icc ifort
```



# SPEC CPU®2017 Floating Point Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

Dell Inc.

SPECrate®2017\_fp\_base = 117

PowerEdge R440 (Intel Xeon Gold 5217, 3.00 GHz)

SPECrate®2017\_fp\_peak = 121

CPU2017 License: 55

Test Sponsor: Dell Inc.

Tested by: Dell Inc.

Test Date: Apr-2020

Hardware Availability: Feb-2020

Software Availability: Apr-2020

## Peak Portability Flags

Same as Base Portability Flags

## Peak Optimization Flags

C benchmarks:

519.lbm\_r: basepeak = yes

538.imagick\_r: basepeak = yes

544.nab\_r: basepeak = yes

C++ benchmarks:

508.namd\_r: basepeak = yes

510.parest\_r: -m64 -qnextgen

-Wl,-plugin-opt=-x86-branches-within-32B-boundaries

-Wl,-z,muldefs -fuse-ld=gold -xCORE-AVX2 -Ofast

-ffast-math -flto -mfpmath=sse -funroll-loops

-qopt-mem-layout-trans=4 -L/usr/local/jemalloc64-5.0.1/lib

-ljemalloc

Fortran benchmarks:

503.bwaves\_r: -m64 -Wl,-plugin-opt=-x86-branches-within-32B-boundaries

-Wl,-z,muldefs -fuse-ld=gold -xCORE-AVX2 -O3 -ipo

-no-prec-div -qopt-prefetch -ffinite-math-only

-qopt-multiple-gather-scatter-by-shuffles

-qopt-mem-layout-trans=4 -nostandard-realloc-lhs

-align array32byte -auto -mbranches-within-32B-boundaries

-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

549.fotonik3d\_r: basepeak = yes

554.roms\_r: Same as 503.bwaves\_r

Benchmarks using both Fortran and C:

521.wrf\_r: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX2 -O3 -ipo

-no-prec-div -qopt-prefetch -ffinite-math-only

-qopt-multiple-gather-scatter-by-shuffles

-qopt-mem-layout-trans=4 -mbranches-within-32B-boundaries

-nostandard-realloc-lhs -align array32byte -auto

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# SPEC CPU®2017 Floating Point Rate Result

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## Peak Optimization Flags (Continued)

521.wrf\_r (continued):

```
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc
```

527.cam4\_r: basepeak = yes

Benchmarks using both C and C++:

```
511.povray_r: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX2 -O3 -ipo
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles
-qopt-mem-layout-trans=4 -mbranches-within-32B-boundaries
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc
```

526.blender\_r: basepeak = yes

Benchmarks using Fortran, C, and C++:

507.cactuBSSN\_r: basepeak = yes

The flags files that were used to format this result can be browsed at

[http://www.spec.org/cpu2017/flags/Intel-ic19.1u1-official-linux64\\_revA.html](http://www.spec.org/cpu2017/flags/Intel-ic19.1u1-official-linux64_revA.html)

<http://www.spec.org/cpu2017/flags/Dell-Platform-Flags-PowerEdge-revE10.html>

You can also download the XML flags sources by saving the following links:

[http://www.spec.org/cpu2017/flags/Intel-ic19.1u1-official-linux64\\_revA.xml](http://www.spec.org/cpu2017/flags/Intel-ic19.1u1-official-linux64_revA.xml)

<http://www.spec.org/cpu2017/flags/Dell-Platform-Flags-PowerEdge-revE10.xml>

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