



# SPEC CPU®2017 Floating Point Speed Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS C240 M5 (Intel Xeon Gold 5220R, 2.20GHz)

SPECspeed®2017\_fp\_base = 140

SPECspeed®2017\_fp\_peak = 141

CPU2017 License: 9019

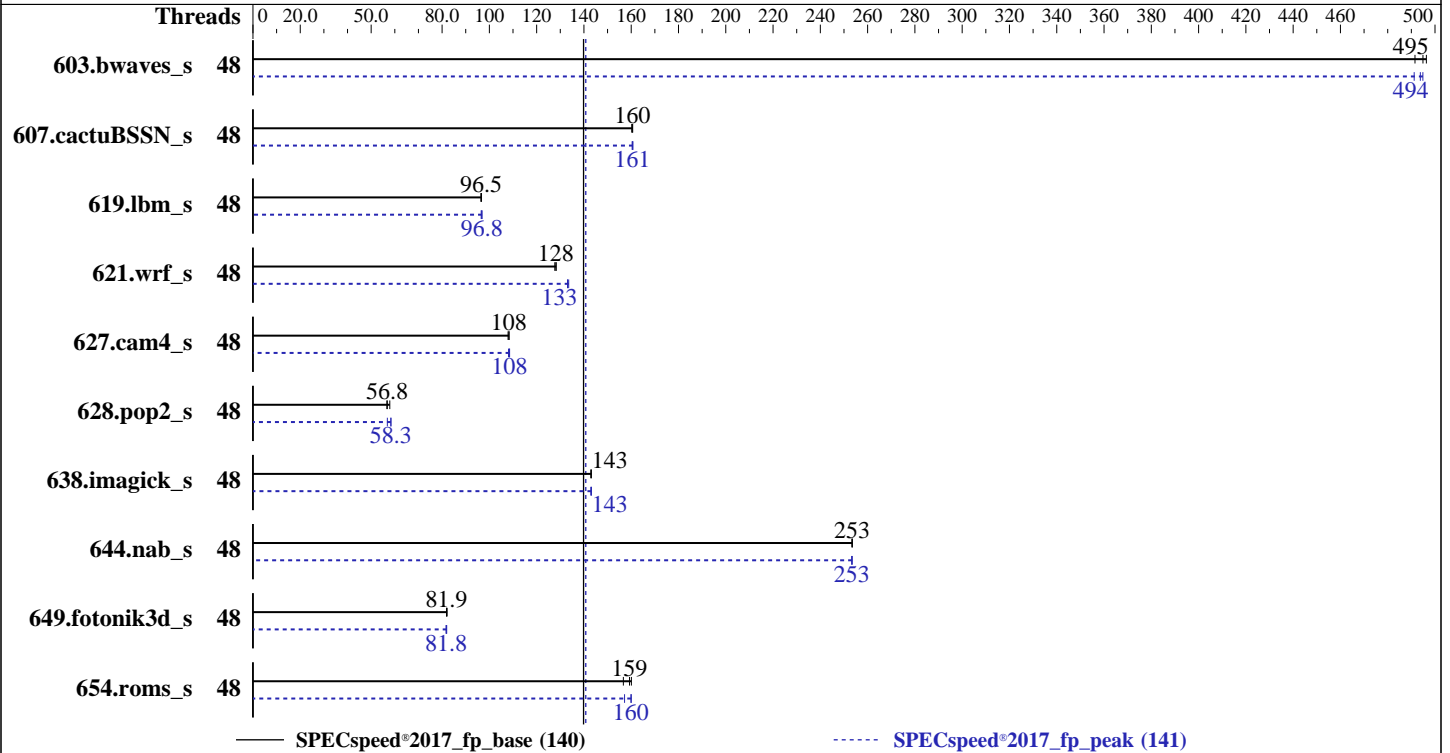
Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Feb-2020

Hardware Availability: Feb-2020

Software Availability: May-2019



### Hardware

CPU Name: Intel Xeon Gold 5220R  
 Max MHz: 4000  
 Nominal: 2200  
 Enabled: 48 cores, 2 chips  
 Orderable: 1,2 Chips  
 Cache L1: 32 KB I + 32 KB D on chip per core  
 L2: 1 MB I+D on chip per core  
 L3: 35.75 MB I+D on chip per chip  
 Other: None  
 Memory: 768 GB (24 x 32 GB 2Rx4 PC4-2933V-R, running at 2666)  
 Storage: 1 x 960 GB SSD SAS  
 Other: None

### Software

OS: SUSE Linux Enterprise Server 15 (x86\_64) 4.12.14-23-default  
 Compiler: C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux;  
 Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux  
 Parallel: Yes  
 Firmware: Version 4.0.4j released Aug-2019  
 File System: btrfs  
 System State: Run level 3 (multi-user)  
 Base Pointers: 64-bit  
 Peak Pointers: 64-bit  
 Other: None  
 Power Management: BIOS set to prefer performance at the cost of additional power usage



# SPEC CPU®2017 Floating Point Speed Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS C240 M5 (Intel Xeon Gold 5220R, 2.20GHz)

SPECSpeed®2017\_fp\_base = 140

SPECSpeed®2017\_fp\_peak = 141

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems

**Test Date:** Feb-2020  
**Hardware Availability:** Feb-2020  
**Software Availability:** May-2019

## Results Table

Benchmark	Base							Peak						
	Threads	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Threads	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
603.bwaves_s	48	120	492	119	496	<u>119</u>	<u>495</u>	48	119	495	120	491	<u>119</u>	<u>494</u>
607.cactuBSSN_s	48	<b>104</b>	<b>160</b>	104	161	104	160	48	104	161	104	160	<b>104</b>	<b>161</b>
619.lbm_s	48	<u>54.3</u>	<u>96.5</u>	54.3	96.5	54.2	96.7	48	54.3	96.5	54.1	96.9	<u>54.1</u>	<u>96.8</u>
621.wrf_s	48	<b>103</b>	<b>128</b>	104	128	103	128	48	<u>99.4</u>	<u>133</u>	99.0	134	99.4	133
627.cam4_s	48	81.8	108	<b>81.9</b>	<b>108</b>	82.1	108	48	<u>81.7</u>	<u>108</u>	82.0	108	81.6	109
628.pop2_s	48	210	56.6	<b>209</b>	<b>56.8</b>	205	57.9	48	<b>204</b>	<b>58.3</b>	209	56.8	203	58.4
638.imagick_s	48	<b>101</b>	<b>143</b>	101	143	101	143	48	<u>101</u>	<u>143</u>	101	143	101	143
644.nab_s	48	<b>68.9</b>	<b>253</b>	68.9	253	68.9	253	48	68.9	253	<b>69.0</b>	<b>253</b>	69.0	253
649.fotonik3d_s	48	111	81.9	111	82.1	<u>111</u>	<u>81.9</u>	48	<u>111</u>	<u>81.8</u>	112	81.7	111	82.0
654.roms_s	48	100	157	98.4	160	<b>98.8</b>	<b>159</b>	48	100	157	<b>98.5</b>	<b>160</b>	98.4	160

SPECSpeed®2017\_fp\_base = **140**

SPECSpeed®2017\_fp\_peak = **141**

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

## Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

## Environment Variables Notes

Environment variables set by runcpu before the start of the run:  
KMP\_AFFINITY = "granularity=fine,compact"  
LD\_LIBRARY\_PATH = "/home/cpu2017/lib/intel64"  
OMP\_STACKSIZE = "192M"

## General Notes

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM memory using Redhat Enterprise Linux 7.5  
Transparent Huge Pages enabled by default  
Prior to runcpu invocation  
Filesystem page cache synced and cleared with:  
sync; echo 3> /proc/sys/vm/drop\_caches  
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.  
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.  
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.



# SPEC CPU®2017 Floating Point Speed Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS C240 M5 (Intel Xeon Gold 5220R, 2.20GHz)

SPECspeed®2017\_fp\_base = 140

SPECspeed®2017\_fp\_peak = 141

**CPU2017 License:** 9019

**Test Sponsor:** Cisco Systems

**Tested by:** Cisco Systems

**Test Date:** Feb-2020

**Hardware Availability:** Feb-2020

**Software Availability:** May-2019

## Platform Notes

BIOS Settings:

Intel HyperThreading Technology set to Disabled

CPU performance set to Enterprise

SNC set to Disabled

Patrol Scrub set to Disabled

Sysinfo program /home/cpu2017/bin/sysinfo

Rev: r6365 of 2019-08-21 295195f888a3d7edble6e46a485a0011

running on linux-dit3 Mon Feb 17 03:14:58 2020

SUT (System Under Test) info as seen by some common utilities.

For more information on this section, see

<https://www.spec.org/cpu2017/Docs/config.html#sysinfo>

From /proc/cpuinfo

model name : Intel(R) Xeon(R) Gold 5220R CPU @ 2.20GHz

2 "physical id"s (chips)

48 "processors"

cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)

cpu cores : 24

siblings : 24

physical 0: cores 0 1 2 3 4 5 6 9 10 11 12 13 16 17 18 19 20 21 24 25 26 27 28 29

physical 1: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 16 17 18 19 20 21 25 26 27 28 29

From lscpu:

Architecture: x86\_64

CPU op-mode(s): 32-bit, 64-bit

Byte Order: Little Endian

CPU(s): 48

On-line CPU(s) list: 0-47

Thread(s) per core: 1

Core(s) per socket: 24

Socket(s): 2

NUMA node(s): 2

Vendor ID: GenuineIntel

CPU family: 6

Model: 85

Model name: Intel(R) Xeon(R) Gold 5220R CPU @ 2.20GHz

Stepping: 7

CPU MHz: 2200.000

CPU max MHz: 4000.0000

CPU min MHz: 1000.0000

BogoMIPS: 4400.00

Virtualization: VT-x

L1d cache: 32K

L1i cache: 32K

(Continued on next page)



# SPEC CPU®2017 Floating Point Speed Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS C240 M5 (Intel Xeon Gold 5220R, 2.20GHz)

SPECspeed®2017\_fp\_base = 140

SPECspeed®2017\_fp\_peak = 141

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems

**Test Date:** Feb-2020  
**Hardware Availability:** Feb-2020  
**Software Availability:** May-2019

### Platform Notes (Continued)

```

L2 cache:          1024K
L3 cache:          36608K
NUMA node0 CPU(s): 0-23
NUMA node1 CPU(s): 24-47
Flags:             fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
aperfperf tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3
sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt
tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault
epb cat_l3 cdp_l3 invpcid_single intel_ppin mba tpr_shadow vnmi flexpriority ept
vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm cqm mpx rdt_a
avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl
xsaveopt xsavec xgetbv1 xsaves cqm_llc cqm_occup_llc cqm_mbm_total cqm_mbm_local
ibpb ibrs stibp dtherm ida arat pln pts hwp hwp_act_window hwp_epp hwp_pkg_req pku
ospke avx512_vnni arch_capabilities ssbd

```

```

/proc/cpuinfo cache data
cache size : 36608 KB

```

```

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a
physical chip.
available: 2 nodes (0-1)
node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23
node 0 size: 385603 MB
node 0 free: 384260 MB
node 1 cpus: 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47
node 1 size: 387055 MB
node 1 free: 379580 MB
node distances:
node  0  1
 0:  10  21
 1:  21  10

```

```

From /proc/meminfo
MemTotal:      791203088 kB
HugePages_Total:      0
Hugepagesize:    2048 kB

```

```

From /etc/*release* /etc/*version*
os-release:
NAME="SLES"
VERSION="15"
VERSION_ID="15"
PRETTY_NAME="SUSE Linux Enterprise Server 15"
ID="sles"
ID_LIKE="suse"

```

(Continued on next page)



# SPEC CPU®2017 Floating Point Speed Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS C240 M5 (Intel Xeon Gold 5220R, 2.20GHz)

SPECspeed®2017\_fp\_base = 140

SPECspeed®2017\_fp\_peak = 141

CPU2017 License: 9019

Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Feb-2020

Hardware Availability: Feb-2020

Software Availability: May-2019

### Platform Notes (Continued)

```
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15"
```

```
uname -a:
Linux linux-dit3 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
x86_64 x86_64 x86_64 GNU/Linux
```

Kernel self-reported vulnerability status:

```
CVE-2018-3620 (L1 Terminal Fault): No status reported
Microarchitectural Data Sampling: No status reported
CVE-2017-5754 (Meltdown): Not affected
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled
via prctl and seccomp
CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Indirect Branch Restricted
Speculation, IBPB, IBRS_FW
```

```
run-level 3 Feb 16 22:40
```

```
SPEC is set to: /home/cpu2017
Filesystem Type Size Used Avail Use% Mounted on
/dev/sda1 btrfs 894G 16G 878G 2% /home
```

```
From /sys/devices/virtual/dmi/id
BIOS: Cisco Systems, Inc. C240M5.4.0.4j.0.0831191216 08/31/2019
Vendor: Cisco Systems Inc
Product: UCSC-C240-M5L
Serial: WZP223909M5
```

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

```
Memory:
24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2666
```

(End of data from sysinfo program)

### Compiler Version Notes

```
=====  
C | 619.lbm_s(base, peak) 638.imagick_s(base, peak)  
 | 644.nab_s(base, peak)  
=====
```

Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,

(Continued on next page)



# SPEC CPU®2017 Floating Point Speed Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS C240 M5 (Intel Xeon Gold 5220R, 2.20GHz)

SPECspeed®2017\_fp\_base = 140

SPECspeed®2017\_fp\_peak = 141

CPU2017 License: 9019

Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Feb-2020

Hardware Availability: Feb-2020

Software Availability: May-2019

### Compiler Version Notes (Continued)

Version 19.0.4.227 Build 20190416  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

=====  
C++, C, Fortran | 607.cactuBSSN\_s(base, peak)

-----  
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,  
Version 19.0.4.227 Build 20190416  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.  
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,  
Version 19.0.4.227 Build 20190416  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.  
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)  
64, Version 19.0.4.227 Build 20190416  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

=====  
Fortran | 603.bwaves\_s(base, peak) 649.fotonik3d\_s(base, peak)  
| 654.roms\_s(base, peak)

-----  
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)  
64, Version 19.0.4.227 Build 20190416  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

=====  
Fortran, C | 621.wrf\_s(base, peak) 627.cam4\_s(base, peak)  
| 628.pop2\_s(base, peak)

-----  
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)  
64, Version 19.0.4.227 Build 20190416  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.  
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,  
Version 19.0.4.227 Build 20190416  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

### Base Compiler Invocation

C benchmarks:  
icc -m64 -std=c11

Fortran benchmarks:  
ifort -m64

(Continued on next page)



# SPEC CPU®2017 Floating Point Speed Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS C240 M5 (Intel Xeon Gold 5220R, 2.20GHz)

SPECspeed®2017\_fp\_base = 140

SPECspeed®2017\_fp\_peak = 141

**CPU2017 License:** 9019

**Test Sponsor:** Cisco Systems

**Tested by:** Cisco Systems

**Test Date:** Feb-2020

**Hardware Availability:** Feb-2020

**Software Availability:** May-2019

## Base Compiler Invocation (Continued)

Benchmarks using both Fortran and C:

```
ifort -m64 icc -m64 -std=c11
```

Benchmarks using Fortran, C, and C++:

```
icpc -m64 icc -m64 -std=c11 ifort -m64
```

## Base Portability Flags

```
603.bwaves_s: -DSPEC_LP64
607.cactuBSSN_s: -DSPEC_LP64
619.lbm_s: -DSPEC_LP64
621.wrf_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
627.cam4_s: -DSPEC_LP64 -DSPEC_CASE_FLAG
628.pop2_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
-assume byterecl
638.imagick_s: -DSPEC_LP64
644.nab_s: -DSPEC_LP64
649.fotonik3d_s: -DSPEC_LP64
654.roms_s: -DSPEC_LP64
```

## Base Optimization Flags

C benchmarks:

```
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP
```

Fortran benchmarks:

```
-DSPEC_OPENMP -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp
-nostandard-realloc-lhs
```

Benchmarks using both Fortran and C:

```
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP
-nostandard-realloc-lhs
```

Benchmarks using Fortran, C, and C++:

```
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP
-nostandard-realloc-lhs
```



# SPEC CPU®2017 Floating Point Speed Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

**Cisco Systems**

Cisco UCS C240 M5 (Intel Xeon Gold 5220R,  
2.20GHz)

SPECspeed®2017\_fp\_base = 140

SPECspeed®2017\_fp\_peak = 141

**CPU2017 License:** 9019

**Test Sponsor:** Cisco Systems

**Tested by:** Cisco Systems

**Test Date:** Feb-2020

**Hardware Availability:** Feb-2020

**Software Availability:** May-2019

## Peak Compiler Invocation

C benchmarks:

```
icc -m64 -std=c11
```

Fortran benchmarks:

```
ifort -m64
```

Benchmarks using both Fortran and C:

```
ifort -m64 icc -m64 -std=c11
```

Benchmarks using Fortran, C, and C++:

```
icpc -m64 icc -m64 -std=c11 ifort -m64
```

## Peak Portability Flags

Same as Base Portability Flags

## Peak Optimization Flags

C benchmarks:

```
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch  
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP
```

Fortran benchmarks:

```
603.bwaves_s: -prof-gen(pass 1) -prof-use(pass 2) -DSPEC_SUPPRESS_OPENMP  
-DSPEC_OPENMP -O2 -xCORE-AVX512 -qopt-prefetch -ipo -O3  
-ffinite-math-only -no-prec-div -qopt-mem-layout-trans=4  
-qopenmp -nostandard-realloc-lhs
```

649.fotonik3d\_s: Same as 603.bwaves\_s

```
654.roms_s: -DSPEC_OPENMP -xCORE-AVX512 -ipo -O3 -no-prec-div  
-qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4  
-qopenmp -nostandard-realloc-lhs
```

Benchmarks using both Fortran and C:

```
621.wrf_s: -prof-gen(pass 1) -prof-use(pass 2) -O2 -xCORE-AVX512  
-qopt-prefetch -ipo -O3 -ffinite-math-only -no-prec-div  
-qopt-mem-layout-trans=4 -DSPEC_SUPPRESS_OPENMP -qopenmp  
-DSPEC_OPENMP -nostandard-realloc-lhs
```

(Continued on next page)





# SPEC CPU®2017 Floating Point Speed Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS C240 M5 (Intel Xeon Gold 5220R,  
2.20GHz)

SPECspeed®2017\_fp\_base = 140

SPECspeed®2017\_fp\_peak = 141

**CPU2017 License:** 9019

**Test Sponsor:** Cisco Systems

**Tested by:** Cisco Systems

**Test Date:** Feb-2020

**Hardware Availability:** Feb-2020

**Software Availability:** May-2019

## Peak Optimization Flags (Continued)

```
627.cam4_s: -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp
-DSPEC_OPENMP -nostandard-realloc-lhs
```

628.pop2\_s: Same as 621.wrf\_s

Benchmarks using Fortran, C, and C++:

```
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP
-nostandard-realloc-lhs
```

The flags files that were used to format this result can be browsed at

<http://www.spec.org/cpu2017/flags/Intel-ic19.0u1-official-linux64.2019-07-09.html>

<http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revJ.html>

You can also download the XML flags sources by saving the following links:

<http://www.spec.org/cpu2017/flags/Intel-ic19.0u1-official-linux64.2019-07-09.xml>

<http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revJ.xml>

SPEC CPU and SPECspeed are registered trademarks of the Standard Performance Evaluation Corporation. All other brand and product names appearing in this result are trademarks or registered trademarks of their respective holders.

For questions about this result, please contact the tester. For other inquiries, please contact [info@spec.org](mailto:info@spec.org).

Tested with SPEC CPU®2017 v1.1.0 on 2020-02-17 03:14:58-0500.

Report generated on 2020-03-17 16:20:26 by CPU2017 PDF formatter v6255.

Originally published on 2020-03-17.