



# SPEC CPU®2017 Floating Point Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS B200 M5 (Intel Xeon Gold 6240, 2.60GHz)

SPECrate®2017\_fp\_base = 213

SPECrate®2017\_fp\_peak = 216

CPU2017 License: 9019

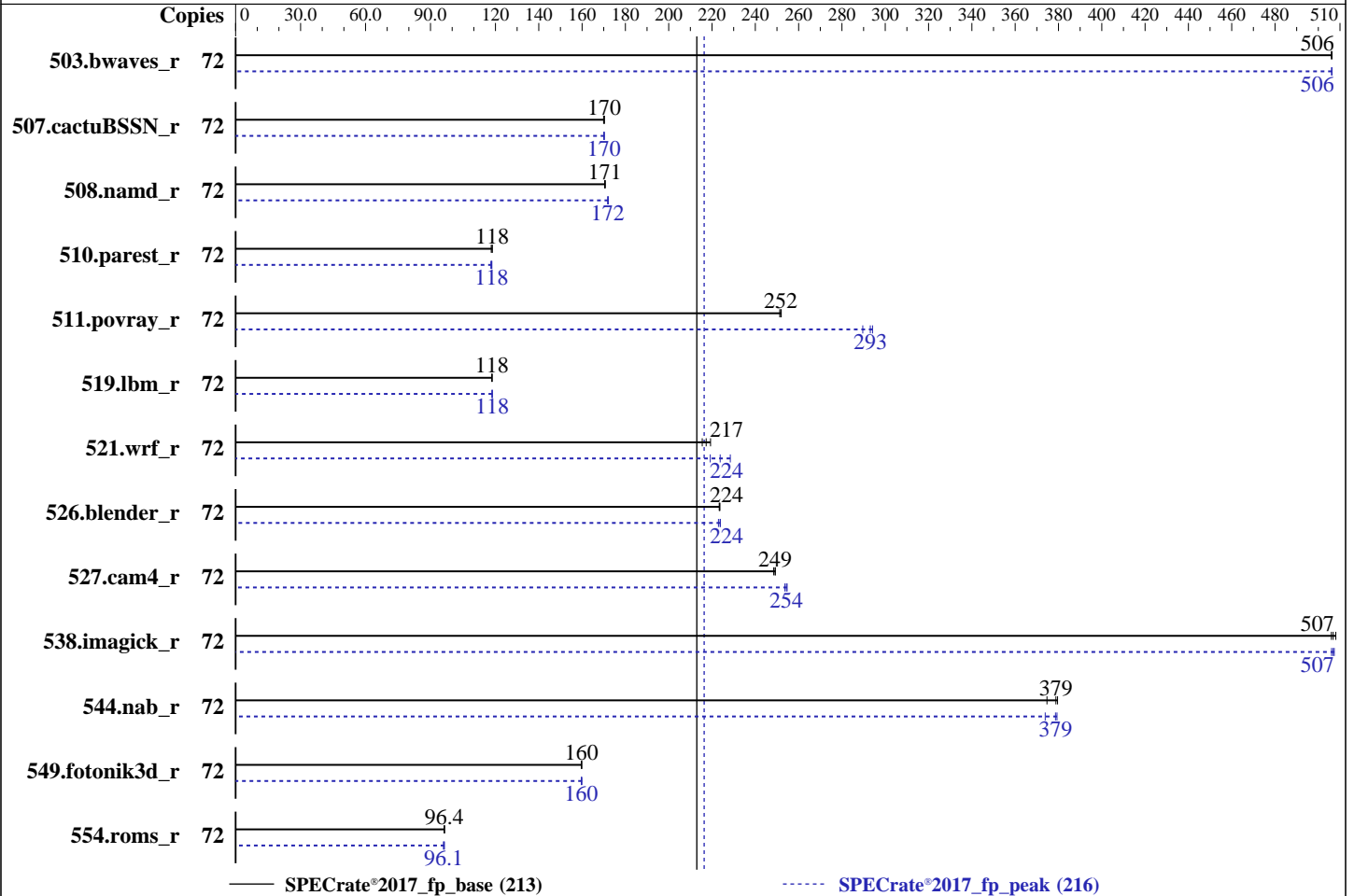
Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Jun-2019

Hardware Availability: Apr-2019

Software Availability: May-2019



### Hardware

CPU Name: Intel Xeon Gold 6240  
 Max MHz: 3900  
 Nominal: 2600  
 Enabled: 36 cores, 2 chips, 2 threads/core  
 Orderable: 1,2 Chips  
 Cache L1: 32 KB I + 32 KB D on chip per core  
 L2: 1 MB I+D on chip per core  
 L3: 24.75 MB I+D on chip per chip  
 Other: None  
 Memory: 768 GB (24 x 32 GB 2Rx4 PC4-2933V-R)  
 Storage: 1 x 1.9 TB SSD SAS  
 Other: None

### Software

OS: SUSE Linux Enterprise Server 15 (x86\_64) 4.12.14-23-default  
 Compiler: C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux;  
 Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux  
 Parallel: No  
 Firmware: Version 4.0.4b released Apr-2019  
 File System: btrfs  
 System State: Run level 3 (multi-user)  
 Base Pointers: 64-bit  
 Peak Pointers: 64-bit  
 Other: None  
 Power Management: --



# SPEC CPU®2017 Floating Point Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS B200 M5 (Intel Xeon Gold 6240, 2.60GHz)

SPECrate®2017\_fp\_base = 213

SPECrate®2017\_fp\_peak = 216

CPU2017 License: 9019  
Test Sponsor: Cisco Systems  
Tested by: Cisco Systems

Test Date: Jun-2019  
Hardware Availability: Apr-2019  
Software Availability: May-2019

### Results Table

Benchmark	Base							Peak						
	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
503.bwaves_r	72	1426	506	<b>1426</b>	<b>506</b>	1427	506	72	<b>1426</b>	<b>506</b>	1426	506	1426	506
507.cactuBSSN_r	72	536	170	535	170	<b>535</b>	<b>170</b>	72	536	170	535	170	<b>536</b>	<b>170</b>
508.namd_r	72	401	171	401	170	<b>401</b>	<b>171</b>	72	<b>398</b>	<b>172</b>	398	172	397	172
510.parest_r	72	<b>1590</b>	<b>118</b>	1589	119	1596	118	72	<b>1593</b>	<b>118</b>	1598	118	1592	118
511.povray_r	72	669	251	667	252	<b>668</b>	<b>252</b>	72	<b>574</b>	<b>293</b>	580	290	572	294
519.lbm_r	72	641	118	<b>641</b>	<b>118</b>	641	118	72	640	118	<b>641</b>	<b>118</b>	641	118
521.wrf_r	72	748	215	<b>742</b>	<b>217</b>	735	219	72	736	219	706	228	<b>721</b>	<b>224</b>
526.blender_r	72	<b>491</b>	<b>224</b>	491	223	490	224	72	492	223	<b>490</b>	<b>224</b>	490	224
527.cam4_r	72	<b>505</b>	<b>249</b>	505	249	507	248	72	494	255	496	254	<b>495</b>	<b>254</b>
538.imagick_r	72	352	508	<b>353</b>	<b>507</b>	354	506	72	353	507	<b>353</b>	<b>507</b>	354	506
544.nab_r	72	<b>320</b>	<b>379</b>	323	375	319	380	72	<b>320</b>	<b>379</b>	319	379	324	374
549.fotonik3d_r	72	1757	160	<b>1756</b>	<b>160</b>	1756	160	72	1754	160	<b>1757</b>	<b>160</b>	1758	160
554.roms_r	72	1186	96.5	1187	96.4	<b>1187</b>	<b>96.4</b>	72	<b>1191</b>	<b>96.1</b>	1191	96.0	1186	96.4

SPECrate®2017\_fp\_base = 213

SPECrate®2017\_fp\_peak = 216

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

### Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

### Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

### General Notes

Environment variables set by runcpu before the start of the run:  
LD\_LIBRARY\_PATH = "/home/cpu2017/lib/intel64"

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM memory using Redhat Enterprise Linux 7.5  
Transparent Huge Pages enabled by default  
Prior to runcpu invocation  
Filesystem page cache synced and cleared with:  
sync; echo 3> /proc/sys/vm/drop\_caches  
runcpu command invoked through numactl i.e.:  
numactl --interleave=all runcpu <etc>

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

(Continued on next page)



# SPEC CPU®2017 Floating Point Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS B200 M5 (Intel Xeon Gold 6240, 2.60GHz)

SPECrate®2017\_fp\_base = 213

SPECrate®2017\_fp\_peak = 216

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems

**Test Date:** Jun-2019  
**Hardware Availability:** Apr-2019  
**Software Availability:** May-2019

### General Notes (Continued)

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

### Platform Notes

BIOS Settings:

Intel HyperThreading Technology set to Enabled  
SNC set to Enabled  
IMC Interleaving set to 1-way Interleave  
Patrol Scrub set to Disabled  
Sysinfo program /home/cpu2017/bin/sysinfo  
Rev: r5974 of 2018-05-19 9bcde8f2999c33d61f64985e45859ea9  
running on linux-eqmk Tue Jun 25 17:36:25 2019

SUT (System Under Test) info as seen by some common utilities.

For more information on this section, see  
<https://www.spec.org/cpu2017/Docs/config.html#sysinfo>

From /proc/cpuinfo

```
model name      : Intel(R) Xeon(R) Gold 6240 CPU @ 2.60GHz
 2 "physical id"s (chips)
 72 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following
excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores      : 18
siblings       : 36
physical 0:    cores 0 1 2 3 4 8 9 10 11 16 17 18 19 20 24 25 26 27
physical 1:    cores 0 1 2 3 4 8 9 10 11 16 17 18 19 20 24 25 26 27
```

From lscpu:

```
Architecture:    x86_64
CPU op-mode(s):  32-bit, 64-bit
Byte Order:      Little Endian
CPU(s):          72
On-line CPU(s) list: 0-71
Thread(s) per core: 2
Core(s) per socket: 18
Socket(s):       2
NUMA node(s):   4
Vendor ID:      GenuineIntel
CPU family:      6
Model:          85
Model name:     Intel(R) Xeon(R) Gold 6240 CPU @ 2.60GHz
Stepping:       6
```

(Continued on next page)



# SPEC CPU®2017 Floating Point Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS B200 M5 (Intel Xeon Gold 6240, 2.60GHz)

SPECrate®2017\_fp\_base = 213

SPECrate®2017\_fp\_peak = 216

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems

**Test Date:** Jun-2019  
**Hardware Availability:** Apr-2019  
**Software Availability:** May-2019

### Platform Notes (Continued)

```

CPU MHz: 2600.000
CPU max MHz: 3900.0000
CPU min MHz: 1000.0000
BogoMIPS: 5200.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 25344K
NUMA node0 CPU(s): 0-2,5,6,9,10,14,15,36-38,41,42,45,46,50,51
NUMA node1 CPU(s): 3,4,7,8,11-13,16,17,39,40,43,44,47-49,52,53
NUMA node2 CPU(s): 18-20,23,24,27,28,32,33,54-56,59,60,63,64,68,69
NUMA node3 CPU(s): 21,22,25,26,29-31,34,35,57,58,61,62,65-67,70,71
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
aperfmpperf tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3
sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt
tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault
epb cat_l3 cdp_l3 invpcid_single intel_ppin mba tpr_shadow vnmi flexpriority ept
vpid fsgsbase tsc_adjust bml hle avx2 smep bmi2 erms invpcid rtm cqm mpx rdt_a
avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl
xsaveopt xsavec xgetbv1 xsaves cqm_llc cqm_occup_llc cqm_mbm_total cqm_mbm_local
ibpb ibrs stibp dtherm ida arat pln pts hwp hwp_act_window hwp_epp hwp_pkg_req pku
ospke avx512_vnni arch_capabilities ssbd

```

```

/proc/cpuinfo cache data
cache size : 25344 KB

```

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.

```

available: 4 nodes (0-3)
node 0 cpus: 0 1 2 5 6 9 10 14 15 36 37 38 41 42 45 46 50 51
node 0 size: 192094 MB
node 0 free: 191316 MB
node 1 cpus: 3 4 7 8 11 12 13 16 17 39 40 43 44 47 48 49 52 53
node 1 size: 193525 MB
node 1 free: 192953 MB
node 2 cpus: 18 19 20 23 24 27 28 32 33 54 55 56 59 60 63 64 68 69
node 2 size: 193525 MB
node 2 free: 192961 MB
node 3 cpus: 21 22 25 26 29 30 31 34 35 57 58 61 62 65 66 67 70 71
node 3 size: 193494 MB
node 3 free: 192834 MB
node distances:
node  0  1  2  3
0:  10  11  21  21

```

(Continued on next page)



# SPEC CPU®2017 Floating Point Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS B200 M5 (Intel Xeon Gold 6240, 2.60GHz)

SPECrate®2017\_fp\_base = 213

SPECrate®2017\_fp\_peak = 216

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems

**Test Date:** Jun-2019  
**Hardware Availability:** Apr-2019  
**Software Availability:** May-2019

### Platform Notes (Continued)

```
1: 11 10 21 21
2: 21 21 10 11
3: 21 21 11 10
```

```
From /proc/meminfo
MemTotal:      791182452 kB
HugePages_Total:      0
Hugepagesize:    2048 kB
```

```
From /etc/*release* /etc/*version*
os-release:
NAME="SLES"
VERSION="15"
VERSION_ID="15"
PRETTY_NAME="SUSE Linux Enterprise Server 15"
ID="sles"
ID_LIKE="suse"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15"
```

```
uname -a:
Linux linux-eqnk 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
x86_64 x86_64 x86_64 GNU/Linux
```

Kernel self-reported vulnerability status:

```
CVE-2017-5754 (Meltdown):      Not affected
CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Indirect Branch Restricted Speculation, IBPB, IBRS_FW
```

```
run-level 3 Jun 25 13:26
```

```
SPEC is set to: /home/cpu2017
Filesystem      Type      Size      Used Avail Use% Mounted on
/dev/sdb2       btrfs    221G      66G  155G  30% /home
```

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

```
BIOS Cisco Systems, Inc. B200M5.4.0.4b.0.0407191258 04/07/2019
Memory:
24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2934
```

(End of data from sysinfo program)



# SPEC CPU®2017 Floating Point Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS B200 M5 (Intel Xeon Gold 6240, 2.60GHz)

SPECrate®2017\_fp\_base = 213

SPECrate®2017\_fp\_peak = 216

**CPU2017 License:** 9019

**Test Sponsor:** Cisco Systems

**Tested by:** Cisco Systems

**Test Date:** Jun-2019

**Hardware Availability:** Apr-2019

**Software Availability:** May-2019

### Compiler Version Notes

```
=====
C | 519.lbm_r(base, peak) 538.imagick_r(base, peak)
  | 544.nab_r(base, peak)
=====
```

```
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
=====
```

```
=====
C++ | 508.namd_r(base, peak) 510.parest_r(base, peak)
=====
```

```
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
=====
```

```
=====
C++, C | 511.povray_r(base, peak) 526.blender_r(base, peak)
=====
```

```
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
=====
```

```
=====
C++, C, Fortran | 507.cactuBSSN_r(base, peak)
=====
```

```
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
=====
```

```
=====
Fortran | 503.bwaves_r(base, peak) 549.fotonik3d_r(base, peak)
         | 554.roms_r(base, peak)
=====
```

```
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
```

(Continued on next page)



# SPEC CPU®2017 Floating Point Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS B200 M5 (Intel Xeon Gold 6240, 2.60GHz)

SPECrate®2017\_fp\_base = 213

SPECrate®2017\_fp\_peak = 216

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems

**Test Date:** Jun-2019  
**Hardware Availability:** Apr-2019  
**Software Availability:** May-2019

### Compiler Version Notes (Continued)

64, Version 19.0.4.227 Build 20190416  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

-----  
=====  
Fortran, C | 521.wrf\_r(base, peak) 527.cam4\_r(base, peak)  
-----

Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)  
64, Version 19.0.4.227 Build 20190416  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.  
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,  
Version 19.0.4.227 Build 20190416  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.  
-----

### Base Compiler Invocation

C benchmarks:

icc -m64 -std=c11

C++ benchmarks:

icpc -m64

Fortran benchmarks:

ifort -m64

Benchmarks using both Fortran and C:

ifort -m64 icc -m64 -std=c11

Benchmarks using both C and C++:

icpc -m64 icc -m64 -std=c11

Benchmarks using Fortran, C, and C++:

icpc -m64 icc -m64 -std=c11 ifort -m64

### Base Portability Flags

503.bwaves\_r: -DSPEC\_LP64  
507.cactuBSSN\_r: -DSPEC\_LP64  
508.namd\_r: -DSPEC\_LP64  
510.parest\_r: -DSPEC\_LP64  
511.povray\_r: -DSPEC\_LP64  
519.lbm\_r: -DSPEC\_LP64

(Continued on next page)



# SPEC CPU®2017 Floating Point Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS B200 M5 (Intel Xeon Gold 6240, 2.60GHz)

SPECrate®2017\_fp\_base = 213

SPECrate®2017\_fp\_peak = 216

CPU2017 License: 9019

Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Jun-2019

Hardware Availability: Apr-2019

Software Availability: May-2019

## Base Portability Flags (Continued)

```
521.wrf_r: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
526.blender_r: -DSPEC_LP64 -DSPEC_LINUX -funsigned-char
527.cam4_r: -DSPEC_LP64 -DSPEC_CASE_FLAG
538.imagick_r: -DSPEC_LP64
544.nab_r: -DSPEC_LP64
549.fotonik3d_r: -DSPEC_LP64
554.roms_r: -DSPEC_LP64
```

## Base Optimization Flags

C benchmarks:

```
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4
```

C++ benchmarks:

```
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4
```

Fortran benchmarks:

```
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte
```

Benchmarks using both Fortran and C:

```
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte
```

Benchmarks using both C and C++:

```
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4
```

Benchmarks using Fortran, C, and C++:

```
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte
```

## Peak Compiler Invocation

C benchmarks:

```
icc -m64 -std=c11
```

(Continued on next page)





# SPEC CPU®2017 Floating Point Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

**Cisco Systems**

Cisco UCS B200 M5 (Intel Xeon Gold 6240, 2.60GHz)

SPECrate®2017\_fp\_base = 213

SPECrate®2017\_fp\_peak = 216

**CPU2017 License:** 9019

**Test Sponsor:** Cisco Systems

**Tested by:** Cisco Systems

**Test Date:** Jun-2019

**Hardware Availability:** Apr-2019

**Software Availability:** May-2019

## Peak Compiler Invocation (Continued)

C++ benchmarks:

icpc -m64

Fortran benchmarks:

ifort -m64

Benchmarks using both Fortran and C:

ifort -m64 icc -m64 -std=c11

Benchmarks using both C and C++:

icpc -m64 icc -m64 -std=c11

Benchmarks using Fortran, C, and C++:

icpc -m64 icc -m64 -std=c11 ifort -m64

## Peak Portability Flags

Same as Base Portability Flags

## Peak Optimization Flags

C benchmarks:

519.lbm\_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512  
-O3 -no-prec-div -qopt-prefetch -ffinite-math-only  
-qopt-mem-layout-trans=4

538.imagick\_r: -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch  
-ffinite-math-only -qopt-mem-layout-trans=4

544.nab\_r: Same as 538.imagick\_r

C++ benchmarks:

508.namd\_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512  
-O3 -no-prec-div -qopt-prefetch -ffinite-math-only  
-qopt-mem-layout-trans=4

510.parest\_r: -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch  
-ffinite-math-only -qopt-mem-layout-trans=4

(Continued on next page)



# SPEC CPU®2017 Floating Point Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS B200 M5 (Intel Xeon Gold 6240, 2.60GHz)

SPECrate®2017\_fp\_base = 213

SPECrate®2017\_fp\_peak = 216

**CPU2017 License:** 9019

**Test Sponsor:** Cisco Systems

**Tested by:** Cisco Systems

**Test Date:** Jun-2019

**Hardware Availability:** Apr-2019

**Software Availability:** May-2019

## Peak Optimization Flags (Continued)

Fortran benchmarks:

```
503.bwaves_r: -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte
```

549.fotonik3d\_r: Same as 503.bwaves\_r

```
554.roms_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512
-O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4 -auto -nostandard-realloc-lhs
-align array32byte
```

Benchmarks using both Fortran and C:

```
-prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512 -O3
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4 -auto -nostandard-realloc-lhs
-align array32byte
```

Benchmarks using both C and C++:

```
511.povray_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512
-O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4
```

```
526.blender_r: -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4
```

Benchmarks using Fortran, C, and C++:

```
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte
```

The flags files that were used to format this result can be browsed at

<http://www.spec.org/cpu2017/flags/Intel-ic19.0u1-official-linux64.2019-07-09.html>

<http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revH.2019-07-31.html>

You can also download the XML flags sources by saving the following links:

<http://www.spec.org/cpu2017/flags/Intel-ic19.0u1-official-linux64.2019-07-09.xml>

<http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revH.2019-07-31.xml>



# SPEC CPU®2017 Floating Point Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS B200 M5 (Intel Xeon Gold 6240, 2.60GHz)

SPECrate®2017\_fp\_base = 213

SPECrate®2017\_fp\_peak = 216

**CPU2017 License:** 9019

**Test Sponsor:** Cisco Systems

**Tested by:** Cisco Systems

**Test Date:** Jun-2019

**Hardware Availability:** Apr-2019

**Software Availability:** May-2019

SPEC CPU and SPECrate are registered trademarks of the Standard Performance Evaluation Corporation. All other brand and product names appearing in this result are trademarks or registered trademarks of their respective holders.

For questions about this result, please contact the tester. For other inquiries, please contact [info@spec.org](mailto:info@spec.org).

Tested with SPEC CPU®2017 v1.0.5 on 2019-06-25 20:36:24-0400.

Report generated on 2020-07-01 18:34:30 by CPU2017 PDF formatter v6255.

Originally published on 2019-07-31.