



# SPEC CPU®2017 Integer Speed Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS C480 M5 (Intel Xeon Gold 6126, 2.60 GHz)

SPECspeed®2017\_int\_base = 8.84

SPECspeed®2017\_int\_peak = 9.18

CPU2017 License: 9019

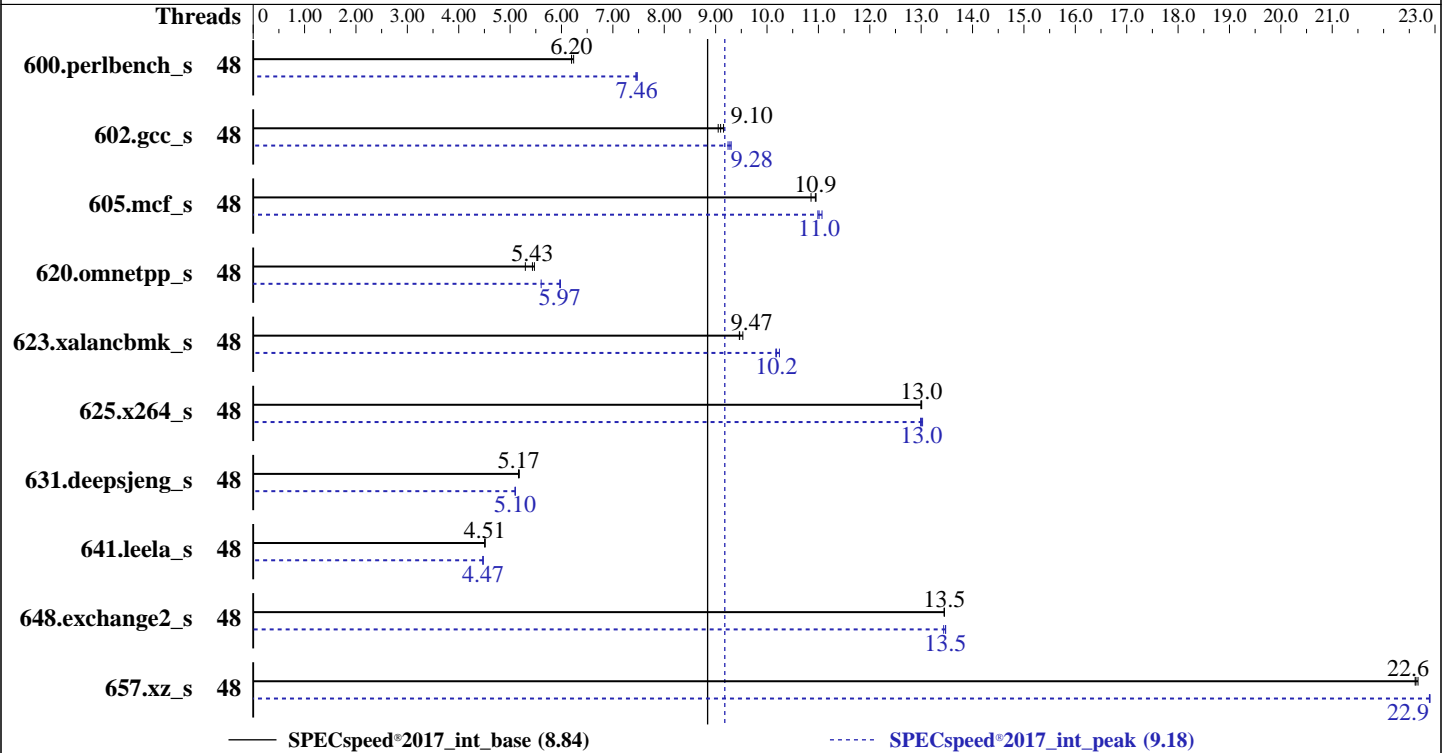
Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Jan-2019

Hardware Availability: Aug-2017

Software Availability: Oct-2018



### Hardware

CPU Name: Intel Xeon Gold 6126  
 Max MHz: 3700  
 Nominal: 2600  
 Enabled: 48 cores, 4 chips  
 Orderable: 2,4 Chips  
 Cache L1: 32 KB I + 32 KB D on chip per core  
 L2: 1 MB I+D on chip per core  
 L3: 19.25 MB I+D on chip per chip  
 Other: None  
 Memory: 1536 GB (48 x 32 GB 2Rx4 PC4-2666V-R)  
 Storage: 1 x 1 TB HDD, 7.2K RPM  
 Other: None

### Software

OS: SUSE Linux Enterprise Server 12 SP2 (x86\_64) 4.4.120-92.70-default  
 Compiler: C/C++: Version 19.0.0.117 of Intel C/C++ Compiler for Linux;  
 Fortran: Version 19.0.0.117 of Intel Fortran Compiler for Linux  
 Parallel: Yes  
 Firmware: Version 3.1.3e released Jun-2018  
 File System: xfs  
 System State: Run level 3 (multi-user)  
 Base Pointers: 64-bit  
 Peak Pointers: 32/64-bit  
 Other: jemalloc memory allocator V5.0.1  
 Power Management: --



# SPEC CPU®2017 Integer Speed Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS C480 M5 (Intel Xeon Gold 6126, 2.60 GHz)

SPECspeed®2017\_int\_base = 8.84

SPECspeed®2017\_int\_peak = 9.18

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems

**Test Date:** Jan-2019  
**Hardware Availability:** Aug-2017  
**Software Availability:** Oct-2018

## Results Table

Benchmark	Base						Peak							
	Threads	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Threads	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
600.perlbench_s	48	285	6.24	<b><u>286</u></b>	<b><u>6.20</u></b>	286	6.20	48	<b><u>238</u></b>	<b><u>7.46</u></b>	238	7.45	237	7.47
602.gcc_s	48	435	9.15	<b><u>438</u></b>	<b><u>9.10</u></b>	440	9.05	48	<b><u>429</u></b>	<b><u>9.28</u></b>	431	9.24	428	9.30
605.mcf_s	48	431	11.0	<b><u>431</u></b>	<b><u>10.9</u></b>	435	10.9	48	430	11.0	<b><u>429</u></b>	<b><u>11.0</u></b>	426	11.1
620.omnetpp_s	48	298	5.47	<b><u>300</u></b>	<b><u>5.43</u></b>	308	5.30	48	<b><u>273</u></b>	<b><u>5.97</u></b>	291	5.60	273	5.98
623.xalancbmk_s	48	149	9.53	<b><u>150</u></b>	<b><u>9.47</u></b>	150	9.46	48	139	10.2	<b><u>139</u></b>	<b><u>10.2</u></b>	138	10.2
625.x264_s	48	<b><u>136</u></b>	<b><u>13.0</u></b>	136	13.0	136	13.0	48	136	13.0	135	13.0	<b><u>136</u></b>	<b><u>13.0</u></b>
631.deepsjeng_s	48	<b><u>277</u></b>	<b><u>5.17</u></b>	277	5.18	278	5.16	48	281	5.10	281	5.10	<b><u>281</u></b>	<b><u>5.10</u></b>
641.leela_s	48	378	4.51	<b><u>378</u></b>	<b><u>4.51</u></b>	378	4.51	48	<b><u>381</u></b>	<b><u>4.47</u></b>	381	4.48	382	4.47
648.exchange2_s	48	219	13.5	<b><u>219</u></b>	<b><u>13.5</u></b>	219	13.4	48	218	13.5	<b><u>218</u></b>	<b><u>13.5</u></b>	219	13.4
657.xz_s	48	<b><u>273</u></b>	<b><u>22.6</u></b>	273	22.6	273	22.7	48	<b><u>270</u></b>	<b><u>22.9</u></b>	270	22.9	270	22.9

SPECspeed®2017\_int\_base = **8.84**

SPECspeed®2017\_int\_peak = **9.18**

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

## Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

## General Notes

Environment variables set by runcpu before the start of the run:  
KMP\_AFFINITY = "granularity=fine,scatter"  
LD\_LIBRARY\_PATH = "/home/cpu2017/lib/ia32:/home/cpu2017/lib/intel64"  
OMP\_STACKSIZE = "192M"

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM  
memory using Redhat Enterprise Linux 7.5  
Transparent Huge Pages enabled by default  
Prior to runcpu invocation

Filesystem page cache synced and cleared with:  
sync; echo 3> /proc/sys/vm/drop\_caches

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

jemalloc, a general purpose malloc implementation  
built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5  
sources available from jemalloc.net or <https://github.com/jemalloc/jemalloc/releases>



# SPEC CPU®2017 Integer Speed Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS C480 M5 (Intel Xeon Gold 6126, 2.60 GHz)

SPECspeed®2017\_int\_base = 8.84

SPECspeed®2017\_int\_peak = 9.18

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems

**Test Date:** Jan-2019  
**Hardware Availability:** Aug-2017  
**Software Availability:** Oct-2018

### Platform Notes

#### BIOS Settings:

Intel HyperThreading Technology set to Disabled  
CPU performance set to Enterprise  
Power Performance Tuning set to OS Controls  
SNC set to Disabled  
Patrol Scrub set to Disabled  
Sysinfo program /home/cpu2017/bin/sysinfo  
Rev: r5797 of 2017-06-14 96c45e4568ad54c135fd618bcc091c0f  
running on linux-e8np Fri Jan 25 09:17:01 2019

SUT (System Under Test) info as seen by some common utilities.  
For more information on this section, see  
<https://www.spec.org/cpu2017/Docs/config.html#sysinfo>

#### From /proc/cpuinfo

```
model name      : Intel(R) Xeon(R) Gold 6126 CPU @ 2.60GHz
 4 "physical id"s (chips)
 48 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following
excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores      : 12
siblings       : 12
physical 0:    cores 0 1 3 5 6 8 9 10 11 12 13 14
physical 1:    cores 0 1 3 4 5 6 8 9 10 11 12 13
physical 2:    cores 0 2 3 4 5 8 9 10 11 12 13 14
physical 3:    cores 0 1 2 3 4 6 9 10 11 12 13 14
```

#### From lscpu:

```
Architecture:    x86_64
CPU op-mode(s):  32-bit, 64-bit
Byte Order:      Little Endian
CPU(s):          48
On-line CPU(s) list:  0-47
Thread(s) per core:  1
Core(s) per socket:  12
Socket(s):       4
NUMA node(s):    4
Vendor ID:       GenuineIntel
CPU family:      6
Model:           85
Model name:      Intel(R) Xeon(R) Gold 6126 CPU @ 2.60GHz
Stepping:        4
CPU MHz:         3437.020
CPU max MHz:     3700.0000
CPU min MHz:     1000.0000
BogoMIPS:        5194.45
Virtualization:  VT-x
```

(Continued on next page)



# SPEC CPU®2017 Integer Speed Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS C480 M5 (Intel Xeon Gold 6126, 2.60 GHz)

SPECspeed®2017\_int\_base = 8.84

SPECspeed®2017\_int\_peak = 9.18

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems

**Test Date:** Jan-2019  
**Hardware Availability:** Aug-2017  
**Software Availability:** Oct-2018

### Platform Notes (Continued)

L1d cache: 32K  
L1i cache: 32K  
L2 cache: 1024K  
L3 cache: 19712K  
NUMA node0 CPU(s): 0-11  
NUMA node1 CPU(s): 12-23  
NUMA node2 CPU(s): 24-35  
NUMA node3 CPU(s): 36-47

Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant\_tsc art arch\_perfmon pebs bts rep\_good nopl xtopology nonstop\_tsc aperfmperf eagerfpu pni pclmulqdq dtes64 monitor ds\_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pcid dca sse4\_1 sse4\_2 x2apic movbe popcnt tsc\_deadline\_timer aes xsave avx f16c rdrand lahf\_lm abm 3dnowprefetch ida arat epb invpcid\_single pln pts dtherm hwp hwp\_act\_window hwp\_epp hwp\_pkg\_req intel\_pt rsb\_ctxsw spec\_ctrl stibp retpoline kaiser tpr\_shadow vnmi flexpriority ept vpid fsgsbase tsc\_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm cqm mpx avx512f avx512dq rdseed adx smap clflushopt clwb avx512cd avx512bw avx512vl xsaveopt xsavec xgetbv1 cqm\_llc cqm\_occup\_llc

```
/proc/cpuinfo cache data
cache size : 19712 KB
```

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.

```
available: 4 nodes (0-3)
node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11
node 0 size: 385624 MB
node 0 free: 385320 MB
node 1 cpus: 12 13 14 15 16 17 18 19 20 21 22 23
node 1 size: 387057 MB
node 1 free: 386813 MB
node 2 cpus: 24 25 26 27 28 29 30 31 32 33 34 35
node 2 size: 387057 MB
node 2 free: 386748 MB
node 3 cpus: 36 37 38 39 40 41 42 43 44 45 46 47
node 3 size: 387054 MB
node 3 free: 386864 MB
node distances:
node  0  1  2  3
 0:  10  21  21  21
 1:  21  10  21  21
 2:  21  21  10  21
 3:  21  21  21  10
```

```
From /proc/meminfo
MemTotal: 1583915928 kB
HugePages_Total: 0
```

(Continued on next page)



# SPEC CPU®2017 Integer Speed Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS C480 M5 (Intel Xeon Gold 6126, 2.60 GHz)

SPECspeed®2017\_int\_base = 8.84

SPECspeed®2017\_int\_peak = 9.18

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems

**Test Date:** Jan-2019  
**Hardware Availability:** Aug-2017  
**Software Availability:** Oct-2018

### Platform Notes (Continued)

Hugepagesize: 2048 kB

From /etc/\*release\* /etc/\*version\*

SuSE-release:

SUSE Linux Enterprise Server 12 (x86\_64)

VERSION = 12

PATCHLEVEL = 2

# This file is deprecated and will be removed in a future service pack or release.

# Please check /etc/os-release for details about this release.

os-release:

NAME="SLES"

VERSION="12-SP2"

VERSION\_ID="12.2"

PRETTY\_NAME="SUSE Linux Enterprise Server 12 SP2"

ID="sles"

ANSI\_COLOR="0;32"

CPE\_NAME="cpe:/o:suse:sles:12:sp2"

uname -a:

Linux linux-e8np 4.4.120-92.70-default #1 SMP Wed Mar 14 15:59:43 UTC 2018 (52a83de)  
x86\_64 x86\_64 x86\_64 GNU/Linux

run-level 3 Jan 25 03:54

SPEC is set to: /home/cpu2017

Filesystem	Type	Size	Used	Avail	Use%	Mounted on
/dev/sdal	xf	894G	120G	774G	14%	/

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

BIOS Cisco Systems, Inc. C480M5.3.1.3e.0.0613181101 06/13/2018

Memory:

48x 0xCE00 M393A4K40BB2-CTD 32 GB 2 rank 2666

(End of data from sysinfo program)

### Compiler Version Notes

```
=====  
C      | 600.perlbench_s(base, peak) 602.gcc_s(base, peak) 605.mcf_s(base,  
      | peak) 625.x264_s(base, peak) 657.xz_s(base, peak)  
-----
```

Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,  
Version 19.0.0.117 Build 20180804

(Continued on next page)



# SPEC CPU®2017 Integer Speed Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS C480 M5 (Intel Xeon Gold 6126, 2.60 GHz)

SPECspeed®2017\_int\_base = 8.84

SPECspeed®2017\_int\_peak = 9.18

**CPU2017 License:** 9019

**Test Sponsor:** Cisco Systems

**Tested by:** Cisco Systems

**Test Date:** Jan-2019

**Hardware Availability:** Aug-2017

**Software Availability:** Oct-2018

### Compiler Version Notes (Continued)

Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

=====  
C++ | 623.xalancbmk\_s(peak)  
-----

Intel(R) C++ Intel(R) 64 Compiler for applications running on IA-32, Version 19.0.0.117 Build 20180804

Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

=====  
C++ | 620.omnetpp\_s(base, peak) 623.xalancbmk\_s(base)  
631.deepsjeng\_s(base, peak) 641.leela\_s(base, peak)

Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.0.117 Build 20180804

Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

=====  
C++ | 623.xalancbmk\_s(peak)  
-----

Intel(R) C++ Intel(R) 64 Compiler for applications running on IA-32, Version 19.0.0.117 Build 20180804

Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

=====  
C++ | 620.omnetpp\_s(base, peak) 623.xalancbmk\_s(base)  
631.deepsjeng\_s(base, peak) 641.leela\_s(base, peak)

Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.0.117 Build 20180804

Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

=====  
Fortran | 648.exchange2\_s(base, peak)  
-----

Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.0.117 Build 20180804

Copyright (C) 1985-2018 Intel Corporation. All rights reserved.



# SPEC CPU®2017 Integer Speed Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS C480 M5 (Intel Xeon Gold 6126, 2.60 GHz)

SPECspeed®2017\_int\_base = 8.84

SPECspeed®2017\_int\_peak = 9.18

**CPU2017 License:** 9019

**Test Sponsor:** Cisco Systems

**Tested by:** Cisco Systems

**Test Date:** Jan-2019

**Hardware Availability:** Aug-2017

**Software Availability:** Oct-2018

## Base Compiler Invocation

C benchmarks:

```
icc -m64 -std=c11
```

C++ benchmarks:

```
icpc -m64
```

Fortran benchmarks:

```
ifort -m64
```

## Base Portability Flags

```
600.perlbench_s: -DSPEC_LP64 -DSPEC_LINUX_X64
602.gcc_s: -DSPEC_LP64
605.mcf_s: -DSPEC_LP64
620.omnetpp_s: -DSPEC_LP64
623.xalancbmk_s: -DSPEC_LP64 -DSPEC_LINUX
625.x264_s: -DSPEC_LP64
631.deepsjeng_s: -DSPEC_LP64
641.leela_s: -DSPEC_LP64
648.exchange2_s: -DSPEC_LP64
657.xz_s: -DSPEC_LP64
```

## Base Optimization Flags

C benchmarks:

```
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -qopenmp -DSPEC_OPENMP
-L/usr/local/je5.0.1-64/lib -ljemalloc
```

C++ benchmarks:

```
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -L/usr/local/je5.0.1-64/lib -ljemalloc
```

Fortran benchmarks:

```
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte
-L/usr/local/je5.0.1-64/lib -ljemalloc
```



# SPEC CPU®2017 Integer Speed Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS C480 M5 (Intel Xeon Gold 6126, 2.60 GHz)

SPECspeed®2017\_int\_base = 8.84

SPECspeed®2017\_int\_peak = 9.18

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems

**Test Date:** Jan-2019  
**Hardware Availability:** Aug-2017  
**Software Availability:** Oct-2018

## Peak Compiler Invocation

C benchmarks:

```
icc -m64 -std=c11
```

C++ benchmarks (except as noted below):

```
icpc -m64
```

```
623.xalancbmk_s: icpc -m32 -L/usr/local/IntelCompiler19/compilers_and_libraries_2019.0.117/linux/compiler/lib/ia32_lin
```

Fortran benchmarks:

```
ifort -m64
```

## Peak Portability Flags

```
600.perlbench_s: -DSPEC_LP64 -DSPEC_LINUX_X64  
602.gcc_s: -DSPEC_LP64  
605.mcf_s: -DSPEC_LP64  
620.omnetpp_s: -DSPEC_LP64  
623.xalancbmk_s: -D_FILE_OFFSET_BITS=64 -DSPEC_LINUX  
625.x264_s: -DSPEC_LP64  
631.deepsjeng_s: -DSPEC_LP64  
641.leela_s: -DSPEC_LP64  
648.exchange2_s: -DSPEC_LP64  
657.xz_s: -DSPEC_LP64
```

## Peak Optimization Flags

C benchmarks:

```
600.perlbench_s: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -O2  
-xCORE-AVX512 -qopt-mem-layout-trans=3 -ipo -O3  
-no-prec-div -DSPEC_SUPPRESS_OPENMP -qopenmp  
-DSPEC_OPENMP -fno-strict-overflow  
-L/usr/local/je5.0.1-64/lib -ljemalloc  
  
602.gcc_s: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -O2  
-xCORE-AVX512 -qopt-mem-layout-trans=3 -ipo -O3  
-no-prec-div -DSPEC_SUPPRESS_OPENMP -qopenmp  
-DSPEC_OPENMP -L/usr/local/je5.0.1-64/lib -ljemalloc  
  
605.mcf_s: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo  
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3  
-DSPEC_SUPPRESS_OPENMP -qopenmp -DSPEC_OPENMP
```

(Continued on next page)





# SPEC CPU®2017 Integer Speed Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS C480 M5 (Intel Xeon Gold 6126, 2.60 GHz)

SPECspeed®2017\_int\_base = 8.84

SPECspeed®2017\_int\_peak = 9.18

CPU2017 License: 9019

Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Jan-2019

Hardware Availability: Aug-2017

Software Availability: Oct-2018

## Peak Optimization Flags (Continued)

605.mcf\_s (continued):

```
-L/usr/local/je5.0.1-64/lib -ljemalloc
```

625.x264\_s: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div

```
-qopt-mem-layout-trans=3 -qopenmp -DSPEC_OPENMP
```

```
-L/usr/local/je5.0.1-64/lib -ljemalloc
```

657.xz\_s: Same as 602.gcc\_s

C++ benchmarks:

620.omnetpp\_s: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo

```
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3
```

```
-DSPEC_SUPPRESS_OPENMP -qopenmp -DSPEC_OPENMP
```

```
-L/usr/local/je5.0.1-64/lib -ljemalloc
```

623.xalancbmk\_s: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo

```
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3
```

```
-DSPEC_SUPPRESS_OPENMP -qopenmp -DSPEC_OPENMP
```

```
-L/usr/local/je5.0.1-32/lib -ljemalloc
```

631.deepsjeng\_s: Same as 620.omnetpp\_s

641.leela\_s: Same as 620.omnetpp\_s

Fortran benchmarks:

```
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
```

```
-qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte
```

```
-L/usr/local/je5.0.1-64/lib -ljemalloc
```

The flags files that were used to format this result can be browsed at

<http://www.spec.org/cpu2017/flags/Intel-ic19.0-official-linux64.2019-01-15.html>

<http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revH.html>

You can also download the XML flags sources by saving the following links:

<http://www.spec.org/cpu2017/flags/Intel-ic19.0-official-linux64.2019-01-15.xml>

<http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revH.xml>

SPEC CPU and SPECspeed are registered trademarks of the Standard Performance Evaluation Corporation. All other brand and product names appearing in this result are trademarks or registered trademarks of their respective holders.

For questions about this result, please contact the tester. For other inquiries, please contact [info@spec.org](mailto:info@spec.org).

Tested with SPEC CPU®2017 v1.0.2 on 2019-01-25 09:17:00-0500.

Report generated on 2020-07-01 13:41:08 by CPU2017 PDF formatter v6255.

Originally published on 2019-02-19.