



# SPEC CPU®2017 Integer Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS C240 M5 (Intel Xeon Silver 4108  
1.80 GHz)

SPECrate®2017\_int\_base = 67.4

SPECrate®2017\_int\_peak = 71.1

CPU2017 License: 9019

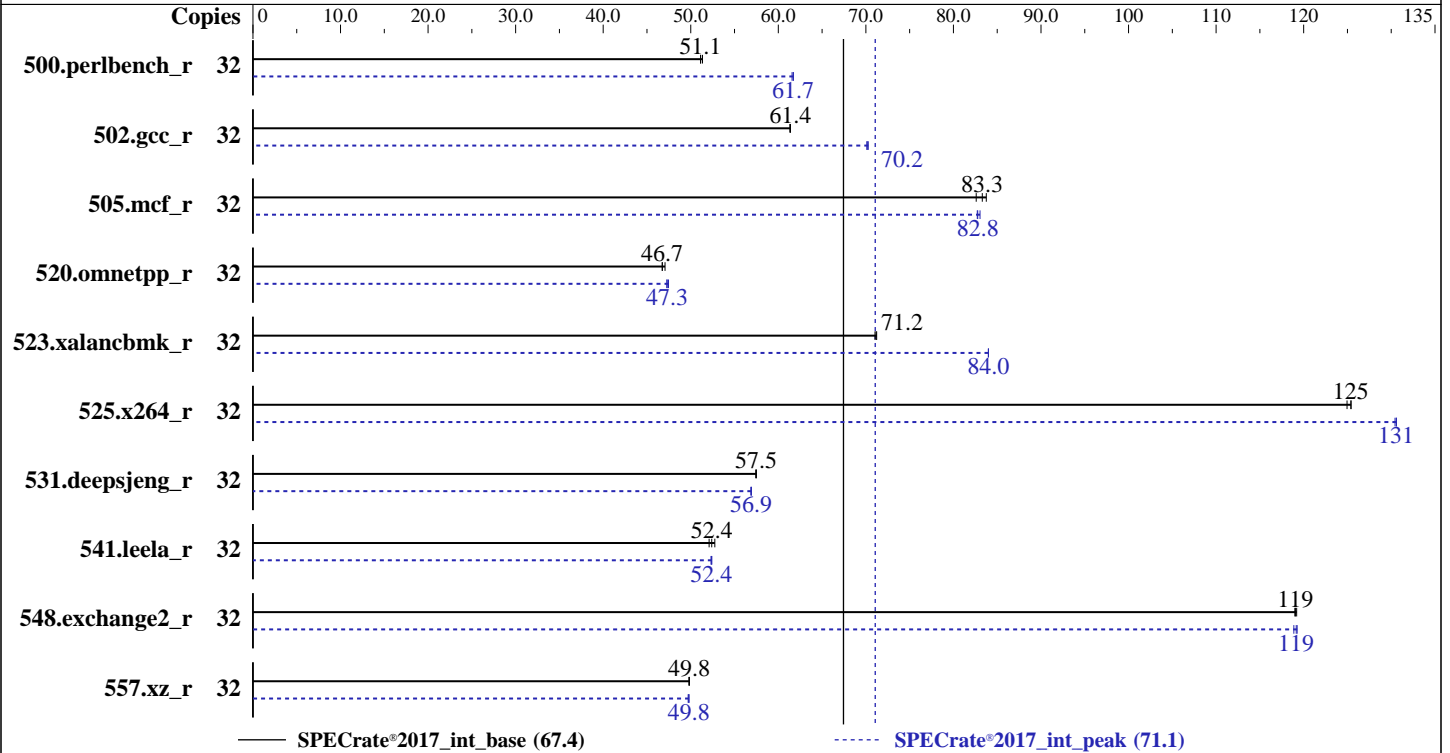
Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Dec-2018

Hardware Availability: Aug-2017

Software Availability: Oct-2018



### Hardware

CPU Name: Intel Xeon Silver 4108  
 Max MHz: 3000  
 Nominal: 1800  
 Enabled: 16 cores, 2 chips, 2 threads/core  
 Orderable: 1,2 Chips  
 Cache L1: 32 KB I + 32 KB D on chip per core  
 L2: 1 MB I+D on chip per core  
 L3: 11 MB I+D on chip per chip  
 Other: None  
 Memory: 768 GB (24 x 32 GB 2Rx4 PC4-2666V-R, running at 2400)  
 Storage: 1 x 600G SAS 10K RPM  
 Other: None

### Software

OS: SUSE Linux Enterprise Server 12 SP2 (x86\_64) 4.4.120-92.70-default  
 Compiler: C/C++: Version 19.0.1.144 of Intel C/C++ Compiler for Linux;  
 Fortran: Version 19.0.1.144 of Intel Fortran Compiler for Linux  
 Parallel: No  
 Firmware: Version 4.0.1 released Oct-2018  
 File System: xfs  
 System State: Run level 3 (multi-user)  
 Base Pointers: 64-bit  
 Peak Pointers: 32/64-bit  
 Other: jemalloc memory allocator V5.0.1  
 Power Management: --



# SPEC CPU®2017 Integer Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS C240 M5 (Intel Xeon Silver 4108  
1.80 GHz)

SPECrate®2017\_int\_base = 67.4

SPECrate®2017\_int\_peak = 71.1

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems

**Test Date:** Dec-2018  
**Hardware Availability:** Aug-2017  
**Software Availability:** Oct-2018

## Results Table

Benchmark	Base							Peak						
	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
500.perlbench_r	32	997	51.1	<b>996</b>	<b>51.1</b>	992	51.3	32	825	61.7	827	61.6	<b>826</b>	<b>61.7</b>
502.gcc_r	32	739	61.3	738	61.4	<b>738</b>	<b>61.4</b>	32	646	70.1	645	70.3	<b>646</b>	<b>70.2</b>
505.mcf_r	32	617	83.8	<b>621</b>	<b>83.3</b>	626	82.6	32	623	83.0	625	82.7	<b>625</b>	<b>82.8</b>
520.omnetpp_r	32	898	46.7	892	47.1	<b>898</b>	<b>46.7</b>	32	885	47.5	888	47.3	<b>887</b>	<b>47.3</b>
523.xalancbmk_r	32	474	71.2	<b>475</b>	<b>71.2</b>	476	71.0	32	<b>402</b>	<b>84.0</b>	402	84.0	402	84.0
525.x264_r	32	447	125	<b>447</b>	<b>125</b>	448	125	32	<b>429</b>	<b>131</b>	429	131	430	130
531.deepsjeng_r	32	638	57.5	639	57.4	<b>638</b>	<b>57.5</b>	32	645	56.9	644	56.9	<b>644</b>	<b>56.9</b>
541.leela_r	32	1005	52.7	1017	52.1	<b>1011</b>	<b>52.4</b>	32	1011	52.4	<b>1012</b>	<b>52.4</b>	1013	52.3
548.exchange2_r	32	705	119	<b>704</b>	<b>119</b>	703	119	32	<b>704</b>	<b>119</b>	703	119	705	119
557.xz_r	32	694	49.8	<b>694</b>	<b>49.8</b>	693	49.8	32	695	49.7	694	49.8	<b>694</b>	<b>49.8</b>

SPECrate®2017\_int\_base = **67.4**

SPECrate®2017\_int\_peak = **71.1**

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

## Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

## Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

## General Notes

Environment variables set by runcpu before the start of the run:

```
LD_LIBRARY_PATH = "/home/cpu2017/lib/ia32:/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-32:/home/cpu2017/je5.0.1-64"
```

Binaries compiled on a system with 1x Intel Core i7-4790 CPU + 32GB RAM  
memory using Redhat Enterprise Linux 7.4  
Transparent Huge Pages enabled by default  
Prior to runcpu invocation

Filesystem page cache synced and cleared with:  
sync; echo 3> /proc/sys/vm/drop\_caches  
runcpu command invoked through numactl i.e.:  
numactl --interleave=all runcpu <etc>

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

(Continued on next page)



# SPEC CPU®2017 Integer Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS C240 M5 (Intel Xeon Silver 4108  
1.80 GHz)

SPECrate®2017\_int\_base = 67.4

SPECrate®2017\_int\_peak = 71.1

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems

**Test Date:** Dec-2018  
**Hardware Availability:** Aug-2017  
**Software Availability:** Oct-2018

### General Notes (Continued)

jemalloc, a general purpose malloc implementation  
built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5  
sources available from jemalloc.net or <https://github.com/jemalloc/jemalloc/releases>

### Platform Notes

BIOS Settings:

Intel HyperThreading Technology set to Enabled  
CPU performance set to Enterprise  
Power Performance Tuning set to OS Controls  
SNC set to Enabled  
IMC Interleaving set to 1-way Interleave  
Patrol Scrub set to Disabled  
Sysinfo program /home/cpu2017/bin/sysinfo  
Rev: r5797 of 2017-06-14 96c45e4568ad54c135fd618bcc091c0f  
running on linux-dkz7 Wed Dec 19 08:50:21 2018

SUT (System Under Test) info as seen by some common utilities.  
For more information on this section, see  
<https://www.spec.org/cpu2017/Docs/config.html#sysinfo>

From /proc/cpuinfo

```
model name      : Intel(R) Xeon(R) Silver 4108 CPU @ 1.80GHz
 2 "physical id"s (chips)
 32 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following
excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores      : 8
siblings       : 16
physical 0:    : cores 0 1 2 3 4 5 6 7
physical 1:    : cores 0 1 2 3 4 5 6 7
```

From lscpu:

```
Architecture:    x86_64
CPU op-mode(s):  32-bit, 64-bit
Byte Order:      Little Endian
CPU(s):          32
On-line CPU(s) list:  0-31
Thread(s) per core:  2
Core(s) per socket:  8
Socket(s):       2
NUMA node(s):    2
Vendor ID:       GenuineIntel
CPU family:      6
Model:           85
Model name:      Intel(R) Xeon(R) Silver 4108 CPU @ 1.80GHz
```

(Continued on next page)



# SPEC CPU®2017 Integer Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS C240 M5 (Intel Xeon Silver 4108  
1.80 GHz)

SPECrate®2017\_int\_base = 67.4

SPECrate®2017\_int\_peak = 71.1

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems

**Test Date:** Dec-2018  
**Hardware Availability:** Aug-2017  
**Software Availability:** Oct-2018

### Platform Notes (Continued)

```
Stepping: 4
CPU MHz: 2817.576
CPU max MHz: 3000.0000
CPU min MHz: 800.0000
BogoMIPS: 3591.56
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 11264K
NUMA node0 CPU(s): 0-7,16-23
NUMA node1 CPU(s): 8-15,24-31
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc
aperfperf eagerfpu pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg
fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes
xsave avx f16c rdrand lahf_lm abm 3dnowprefetch ida arat epb invpcid_single pln pts
dtherm hwp hwp_act_window hwp_epp hwp_pkg_req intel_pt rsb_ctxsw spec_ctrl stibp
retpoline kaiser tpr_shadow vnmi flexpriority ept vpid fsgsbase tsc_adjust bmi1 hle
avx2 smep bmi2 erms invpcid rtm cqm mpx avx512f avx512dq rdseed adx smap clflushopt
clwb avx512cd avx512bw avx512vl xsaveopt xsavec xgetbv1 cqm_llc cqm_occup_llc
```

```
/proc/cpuinfo cache data
cache size : 11264 KB
```

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.

```
available: 2 nodes (0-1)
node 0 cpus: 0 1 2 3 4 5 6 7 16 17 18 19 20 21 22 23
node 0 size: 385626 MB
node 0 free: 382699 MB
node 1 cpus: 8 9 10 11 12 13 14 15 24 25 26 27 28 29 30 31
node 1 size: 387054 MB
node 1 free: 384132 MB
node distances:
node  0  1
  0:  10  21
  1:  21  10
```

```
From /proc/meminfo
MemTotal: 791225564 kB
HugePages_Total: 0
Hugepagesize: 2048 kB
```

```
From /etc/*release* /etc/*version*
SuSE-release:
```

(Continued on next page)



# SPEC CPU®2017 Integer Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS C240 M5 (Intel Xeon Silver 4108  
1.80 GHz)

SPECrate®2017\_int\_base = 67.4

SPECrate®2017\_int\_peak = 71.1

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems

**Test Date:** Dec-2018  
**Hardware Availability:** Aug-2017  
**Software Availability:** Oct-2018

### Platform Notes (Continued)

SUSE Linux Enterprise Server 12 (x86\_64)

VERSION = 12

PATCHLEVEL = 2

# This file is deprecated and will be removed in a future service pack or release.

# Please check /etc/os-release for details about this release.

os-release:

NAME="SLES"

VERSION="12-SP2"

VERSION\_ID="12.2"

PRETTY\_NAME="SUSE Linux Enterprise Server 12 SP2"

ID="sles"

ANSI\_COLOR="0;32"

CPE\_NAME="cpe:/o:suse:sles:12:sp2"

uname -a:

Linux linux-dkz7 4.4.120-92.70-default #1 SMP Wed Mar 14 15:59:43 UTC 2018 (52a83de)  
x86\_64 x86\_64 x86\_64 GNU/Linux

run-level 3 Dec 18 23:43

SPEC is set to: /home/cpu2017

Filesystem	Type	Size	Used	Avail	Use%	Mounted on
/dev/sda2	xf	500G	122G	379G	25%	/

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

BIOS Cisco Systems, Inc. C240M5.4.0.1.139.1003182220 10/03/2018

Memory:

12x 0xCE00 M393A4K40BB2-CTD 32 GB 2 rank 2666, configured at 2400

12x 0xCE00 M393A4K40CB2-CTD 32 GB 2 rank 2666, configured at 2400

(End of data from sysinfo program)

### Compiler Version Notes

```

=====
C          | 500.perlbench_r(base, peak) 502.gcc_r(base, peak) 505.mcf_r(base,
          | peak) 525.x264_r(base, peak) 557.xz_r(base, peak)
=====

```

icc (ICC) 19.0.1.144 20181018

Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

(Continued on next page)



# SPEC CPU®2017 Integer Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS C240 M5 (Intel Xeon Silver 4108  
1.80 GHz)

SPECrate®2017\_int\_base = 67.4

SPECrate®2017\_int\_peak = 71.1

**CPU2017 License:** 9019

**Test Sponsor:** Cisco Systems

**Tested by:** Cisco Systems

**Test Date:** Dec-2018

**Hardware Availability:** Aug-2017

**Software Availability:** Oct-2018

## Compiler Version Notes (Continued)

C++ | 520.omnetpp\_r(base, peak) 523.xalancbmk\_r(base, peak)  
| 531.deepsjeng\_r(base, peak) 541.leela\_r(base, peak)

-----  
icpc (ICC) 19.0.1.144 20181018

Copyright (C) 1985-2018 Intel Corporation. All rights reserved.  
-----

=====  
Fortran | 548.exchange2\_r(base, peak)

-----  
ifort (IFORT) 19.0.1.144 20181018

Copyright (C) 1985-2018 Intel Corporation. All rights reserved.  
-----

## Base Compiler Invocation

C benchmarks:

icc -m64 -std=c11

C++ benchmarks:

icpc -m64

Fortran benchmarks:

ifort -m64

## Base Portability Flags

500.perlbench\_r: -DSPEC\_LP64 -DSPEC\_LINUX\_X64

502 gcc\_r: -DSPEC\_LP64

505.mcf\_r: -DSPEC\_LP64

520.omnetpp\_r: -DSPEC\_LP64

523.xalancbmk\_r: -DSPEC\_LP64 -DSPEC\_LINUX

525.x264\_r: -DSPEC\_LP64

531.deepsjeng\_r: -DSPEC\_LP64

541.leela\_r: -DSPEC\_LP64

548.exchange2\_r: -DSPEC\_LP64

557.xz\_r: -DSPEC\_LP64



# SPEC CPU®2017 Integer Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS C240 M5 (Intel Xeon Silver 4108  
1.80 GHz)

SPECrate®2017\_int\_base = 67.4

SPECrate®2017\_int\_peak = 71.1

**CPU2017 License:** 9019

**Test Sponsor:** Cisco Systems

**Tested by:** Cisco Systems

**Test Date:** Dec-2018

**Hardware Availability:** Aug-2017

**Software Availability:** Oct-2018

## Base Optimization Flags

C benchmarks:

```
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div  
-qopt-mem-layout-trans=3 -L/home/cpu2017/je5.0.1-64/ -ljemalloc
```

C++ benchmarks:

```
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div  
-qopt-mem-layout-trans=3 -L/home/cpu2017/je5.0.1-64/ -ljemalloc
```

Fortran benchmarks:

```
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div  
-qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte  
-L/home/cpu2017/je5.0.1-64/ -ljemalloc
```

## Peak Compiler Invocation

C benchmarks (except as noted below):

```
icc -m64 -std=c11
```

```
502.gcc_r: icc -m32 -std=c11 -L/opt/intel/lib/ia32
```

C++ benchmarks (except as noted below):

```
icpc -m64
```

```
523.xalancbmk_r: icpc -m32 -L/opt/intel/lib/ia32
```

Fortran benchmarks:

```
ifort -m64
```

## Peak Portability Flags

```
500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
```

```
502.gcc_r: -D_FILE_OFFSET_BITS=64
```

```
505.mcf_r: -DSPEC_LP64
```

```
520.omnetpp_r: -DSPEC_LP64
```

```
523.xalancbmk_r: -D_FILE_OFFSET_BITS=64 -DSPEC_LINUX
```

```
525.x264_r: -DSPEC_LP64
```

```
531.deepsjeng_r: -DSPEC_LP64
```

```
541.leela_r: -DSPEC_LP64
```

```
548.exchange2_r: -DSPEC_LP64
```

```
557.xz_r: -DSPEC_LP64
```



# SPEC CPU®2017 Integer Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS C240 M5 (Intel Xeon Silver 4108  
1.80 GHz)

SPECrate®2017\_int\_base = 67.4

SPECrate®2017\_int\_peak = 71.1

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems

**Test Date:** Dec-2018  
**Hardware Availability:** Aug-2017  
**Software Availability:** Oct-2018

## Peak Optimization Flags

C benchmarks:

500.perlbench\_r: -w1,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo  
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3  
-fno-strict-overflow -L/home/cpu2017/je5.0.1-64/  
-ljemalloc

502.gcc\_r: -w1,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo  
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3  
-L/home/cpu2017/je5.0.1-32/ -ljemalloc

505.mcf\_r: -w1,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div  
-qopt-mem-layout-trans=3 -L/home/cpu2017/je5.0.1-64/  
-ljemalloc

525.x264\_r: -w1,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div  
-qopt-mem-layout-trans=3 -fno-alias  
-L/home/cpu2017/je5.0.1-64/ -ljemalloc

557.xz\_r: Same as 505.mcf\_r

C++ benchmarks:

520.omnetpp\_r: -w1,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo  
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3  
-L/home/cpu2017/je5.0.1-64/ -ljemalloc

523.xalancbmk\_r: -w1,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo  
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3  
-L/home/cpu2017/je5.0.1-32/ -ljemalloc

531.deepsjeng\_r: Same as 520.omnetpp\_r

541.leela\_r: Same as 520.omnetpp\_r

Fortran benchmarks:

-w1,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div  
-qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte  
-L/home/cpu2017/je5.0.1-64/ -ljemalloc

The flags files that were used to format this result can be browsed at

<http://www.spec.org/cpu2017/flags/Intel-ic19.0-official-linux64.html>

<http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revH.html>





# SPEC CPU®2017 Integer Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS C240 M5 (Intel Xeon Silver 4108  
1.80 GHz)

SPECrate®2017\_int\_base = 67.4

SPECrate®2017\_int\_peak = 71.1

**CPU2017 License:** 9019

**Test Sponsor:** Cisco Systems

**Tested by:** Cisco Systems

**Test Date:** Dec-2018

**Hardware Availability:** Aug-2017

**Software Availability:** Oct-2018

You can also download the XML flags sources by saving the following links:

<http://www.spec.org/cpu2017/flags/Intel-ic19.0-official-linux64.xml>

<http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revH.xml>

SPEC CPU and SPECrate are registered trademarks of the Standard Performance Evaluation Corporation. All other brand and product names appearing in this result are trademarks or registered trademarks of their respective holders.

For questions about this result, please contact the tester. For other inquiries, please contact [info@spec.org](mailto:info@spec.org).

Tested with SPEC CPU®2017 v1.0.2 on 2018-12-19 11:50:20-0500.

Report generated on 2020-09-04 14:37:14 by CPU2017 PDF formatter v6255.

Originally published on 2019-01-29.