



SPEC CPU®2017 Integer Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS C240 M5 (Intel Xeon Gold 6142M
2.60 GHz)

SPECrate®2017_int_base = 185

SPECrate®2017_int_peak = 194

CPU2017 License: 9019

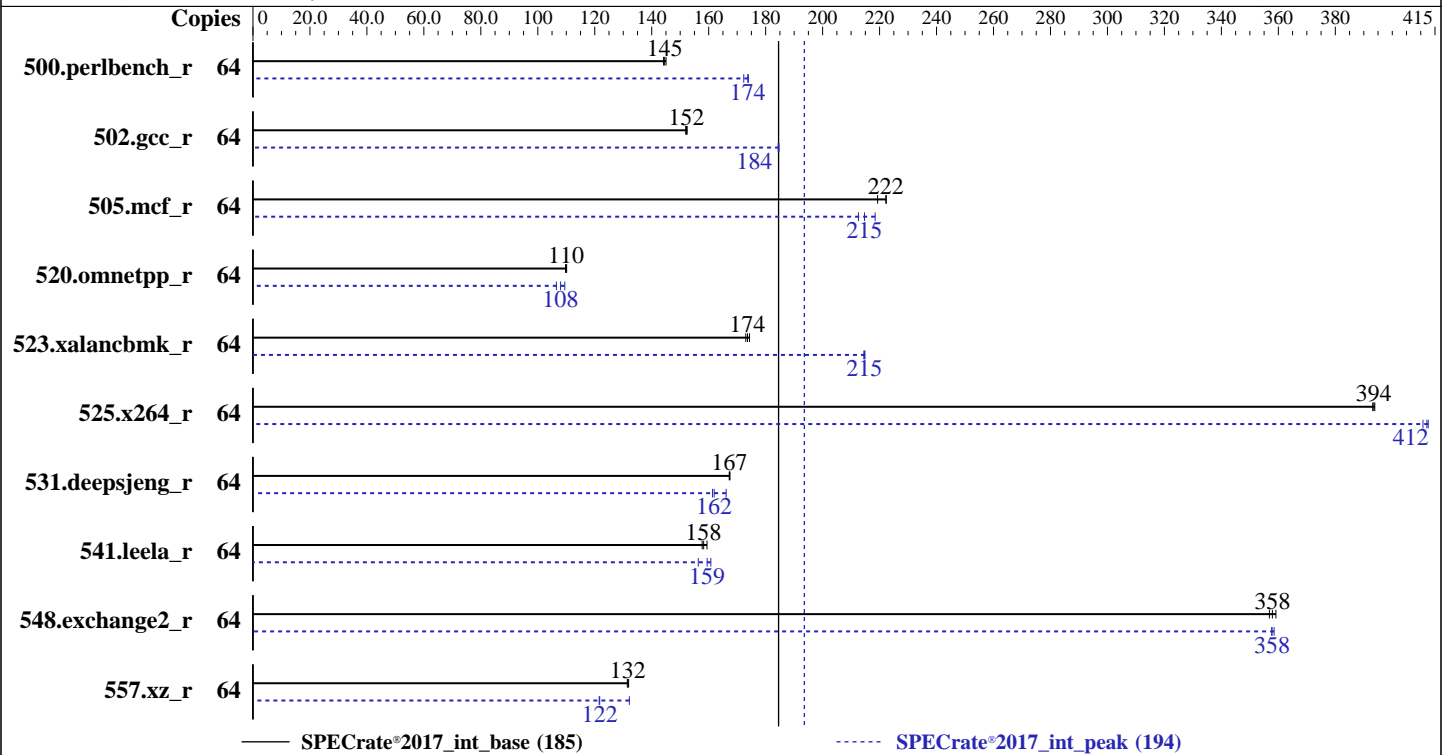
Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Nov-2018

Hardware Availability: Aug-2017

Software Availability: Oct-2018



Hardware

CPU Name: Intel Xeon Gold 6142M
 Max MHz: 3700
 Nominal: 2600
 Enabled: 32 cores, 2 chips, 2 threads/core
 Orderable: 1,2 Chips
 Cache L1: 32 KB I + 32 KB D on chip per core
 L2: 1 MB I+D on chip per core
 L3: 22 MB I+D on chip per chip
 Other: None
 Memory: 768 GB (24 x 32 GB 2Rx4 PC4-2666V-R)
 Storage: 1 x 600G SAS 10K RPM
 Other: None

Software

OS: SUSE Linux Enterprise Server 12 SP2 (x86_64)
 4.4.120-92.70-default
 Compiler: C/C++: Version 19.0.1.144 of Intel C/C++
 Compiler for Linux;
 Fortran: Version 19.0.1.144 of Intel Fortran
 Compiler for Linux
 Parallel: No
 Firmware: Version 4.0.1 released Oct-2018
 File System: xfs
 System State: Run level 3 (multi-user)
 Base Pointers: 64-bit
 Peak Pointers: 32/64-bit
 Other: jemalloc memory allocator V5.0.1
 Power Management: --



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Results Table

Benchmark	Base							Peak						
	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
500.perlbench_r	64	703	145	<u>705</u>	<u>145</u>	707	144	64	586	174	<u>587</u>	<u>174</u>	591	172
502.gcc_r	64	594	152	<u>595</u>	<u>152</u>	597	152	64	<u>491</u>	<u>184</u>	491	185	491	184
505.mcf_r	64	<u>465</u>	<u>222</u>	465	222	472	219	64	473	218	<u>482</u>	<u>215</u>	487	213
520.omnetpp_r	64	765	110	762	110	<u>764</u>	<u>110</u>	64	767	109	<u>777</u>	<u>108</u>	788	107
523.xalancbmk_r	64	391	173	388	174	<u>389</u>	<u>174</u>	64	<u>315</u>	<u>215</u>	315	215	315	214
525.x264_r	64	285	393	<u>285</u>	<u>394</u>	285	394	64	272	413	273	411	<u>272</u>	<u>412</u>
531.deepsjeng_r	64	438	167	439	167	<u>438</u>	<u>167</u>	64	442	166	455	161	<u>453</u>	<u>162</u>
541.leela_r	64	665	159	672	158	<u>670</u>	<u>158</u>	64	<u>665</u>	<u>159</u>	659	161	678	156
548.exchange2_r	64	467	359	470	357	<u>468</u>	<u>358</u>	64	468	359	469	358	<u>469</u>	<u>358</u>
557.xz_r	64	<u>525</u>	<u>132</u>	524	132	526	131	64	523	132	<u>568</u>	<u>122</u>	569	122

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Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

General Notes

Environment variables set by runcpu before the start of the run:

LD_LIBRARY_PATH = "/home/cpu2017/lib/ia32:/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-32:/home/cpu2017/je5.0.1-64"

Binaries compiled on a system with 1x Intel Core i7-4790 CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.4
Transparent Huge Pages enabled by default
Prior to runcpu invocation

Filesystem page cache synced and cleared with:
sync; echo 3> /proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:
numactl --interleave=all runcpu <etc>

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2)

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General Notes (Continued)

is mitigated in the system as tested and documented.
jemalloc, a general purpose malloc implementation
built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5
sources available from jemalloc.net or <https://github.com/jemalloc/jemalloc/releases>

Platform Notes

BIOS Settings:

Intel HyperThreading Technology set to Enabled
CPU performance set to Enterprise
Power Performance Tuning set to OS Controls
SNC set to Enabled
IMC Interleaving set to 1-way Interleave
Patrol Scrub set to Disabled
Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r5797 of 2017-06-14 96c45e4568ad54c135fd618bcc091c0f
running on linux-dkz7 Fri Dec 7 18:20:03 2018

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
<https://www.spec.org/cpu2017/Docs/config.html#sysinfo>

From /proc/cpuinfo

```
model name : Intel(R) Xeon(R) Gold 6142M CPU @ 2.60GHz
 2 "physical id"s (chips)
 64 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following
excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 16
siblings  : 32
physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
physical 1: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
```

From lscpu:

```
Architecture:          x86_64
CPU op-mode(s):        32-bit, 64-bit
Byte Order:             Little Endian
CPU(s):                 64
On-line CPU(s) list:   0-63
Thread(s) per core:    2
Core(s) per socket:    16
Socket(s):              2
NUMA node(s):          4
Vendor ID:              GenuineIntel
CPU family:             6
Model:                  85
```

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Platform Notes (Continued)

```

Model name: Intel(R) Xeon(R) Gold 6142M CPU @ 2.60GHz
Stepping: 4
CPU MHz: 1613.565
CPU max MHz: 3700.0000
CPU min MHz: 1000.0000
BogoMIPS: 5187.83
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 22528K
NUMA node0 CPU(s): 0-3,8-11,32-35,40-43
NUMA node1 CPU(s): 4-7,12-15,36-39,44-47
NUMA node2 CPU(s): 16-19,24-27,48-51,56-59
NUMA node3 CPU(s): 20-23,28-31,52-55,60-63
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc
aperfmpperf eagerfpu pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg
fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes
xsave avx f16c rdrand lahf_lm abm 3dnowprefetch ida arat epb invpcid_single pln pts
dtherm hwp hwp_act_window hwp_epp hwp_pkg_req intel_pt rsb_ctxsw spec_ctrl stibp
retpoline kaiser tpr_shadow vnmi flexpriority ept vpid fsgsbase tsc_adjust bmi1 hle
avx2 smep bmi2 erms invpcid rtm cqm mpx avx512f avx512dq rdseed adx smap clflushopt
clwb avx512cd avx512bw avx512vl xsaveopt xsavec xgetbv1 cqm_llc cqm_occup_llc

```

```

/proc/cpuinfo cache data
cache size : 22528 KB

```

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.

```

available: 4 nodes (0-3)
node 0 cpus: 0 1 2 3 8 9 10 11 32 33 34 35 40 41 42 43
node 0 size: 192097 MB
node 0 free: 189963 MB
node 1 cpus: 4 5 6 7 12 13 14 15 36 37 38 39 44 45 46 47
node 1 size: 193528 MB
node 1 free: 191507 MB
node 2 cpus: 16 17 18 19 24 25 26 27 48 49 50 51 56 57 58 59
node 2 size: 193528 MB
node 2 free: 191541 MB
node 3 cpus: 20 21 22 23 28 29 30 31 52 53 54 55 60 61 62 63
node 3 size: 193525 MB
node 3 free: 191425 MB
node distances:
node 0 1 2 3
0: 10 11 21 21

```

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Platform Notes (Continued)

```
1: 11 10 21 21
2: 21 21 10 11
3: 21 21 11 10
```

From /proc/meminfo

```
MemTotal:      791224900 kB
HugePages_Total:      0
Hugepagesize:    2048 kB
```

From /etc/*release* /etc/*version*

SuSE-release:

```
SUSE Linux Enterprise Server 12 (x86_64)
VERSION = 12
PATCHLEVEL = 2
```

```
# This file is deprecated and will be removed in a future service pack or release.
# Please check /etc/os-release for details about this release.
```

os-release:

```
NAME="SLES"
VERSION="12-SP2"
VERSION_ID="12.2"
PRETTY_NAME="SUSE Linux Enterprise Server 12 SP2"
ID="sles"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:12:sp2"
```

uname -a:

```
Linux linux-dkz7 4.4.120-92.70-default #1 SMP Wed Mar 14 15:59:43 UTC 2018 (52a83de)
x86_64 x86_64 x86_64 GNU/Linux
```

run-level 3 Dec 7 09:08

SPEC is set to: /home/cpu2017

```
Filesystem      Type      Size      Used Avail Use% Mounted on
/dev/sda2        xfs       500G      124G   377G   25% /
```

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

BIOS Cisco Systems, Inc. C240M5.4.0.1.139.1003182220 10/03/2018

Memory:

```
12x 0xCE00 M393A4K40BB2-CTD 32 GB 2 rank 2666
12x 0xCE00 M393A4K40CB2-CTD 32 GB 2 rank 2666
```

(End of data from sysinfo program)



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Compiler Version Notes

=====
C | 500.perlbench_r(base, peak) 502.gcc_r(base, peak) 505.mcf_r(base,
| peak) 525.x264_r(base, peak) 557.xz_r(base, peak)
=====

icc (ICC) 19.0.1.144 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

=====
C++ | 520.omnetpp_r(base, peak) 523.xalancbmk_r(base, peak)
| 531.deepsjeng_r(base, peak) 541.leela_r(base, peak)
=====

icpc (ICC) 19.0.1.144 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

=====
Fortran | 548.exchange2_r(base, peak)
=====

ifort (IFORT) 19.0.1.144 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64

Base Portability Flags

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -DSPEC_LP64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64

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Base Portability Flags (Continued)

541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64

Base Optimization Flags

C benchmarks:

-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -L/home/cpu2017/je5.0.1-64/ -ljemalloc

C++ benchmarks:

-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -L/home/cpu2017/je5.0.1-64/ -ljemalloc

Fortran benchmarks:

-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte
-L/home/cpu2017/je5.0.1-64/ -ljemalloc

Peak Compiler Invocation

C benchmarks (except as noted below):

icc -m64 -std=c11

502.gcc_r: icc -m32 -std=c11 -L/opt/intel/lib/ia32

C++ benchmarks (except as noted below):

icpc -m64

523.xalancbmk_r: icpc -m32 -L/opt/intel/lib/ia32

Fortran benchmarks:

ifort -m64

Peak Portability Flags

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -D_FILE_OFFSET_BITS=64
505.mcf_r: -DSPEC_LP64

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Peak Portability Flags (Continued)

520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -D_FILE_OFFSET_BITS=64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64

Peak Optimization Flags

C benchmarks:

500.perlbench_r: -w1, -z, muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3
-fno-strict-overflow -L/home/cpu2017/je5.0.1-64/
-ljemalloc

502.gcc_r: -w1, -z, muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3
-L/home/cpu2017/je5.0.1-32/ -ljemalloc

505.mcf_r: -w1, -z, muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -L/home/cpu2017/je5.0.1-64/
-ljemalloc

525.x264_r: -w1, -z, muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -fno-alias
-L/home/cpu2017/je5.0.1-64/ -ljemalloc

557.xz_r: Same as 505.mcf_r

C++ benchmarks:

520.omnetpp_r: -w1, -z, muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3
-L/home/cpu2017/je5.0.1-64/ -ljemalloc

523.xalancbmk_r: -w1, -z, muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3
-L/home/cpu2017/je5.0.1-32/ -ljemalloc

531.deepsjeng_r: Same as 520.omnetpp_r

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Peak Optimization Flags (Continued)

541.leela_r: Same as 520.omnetpp_r

Fortran benchmarks:

```
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div  
-qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte  
-L/home/cpu2017/je5.0.1-64/ -ljemalloc
```

The flags files that were used to format this result can be browsed at

<http://www.spec.org/cpu2017/flags/Intel-ic19.0-official-linux64.html>

<http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revH.html>

You can also download the XML flags sources by saving the following links:

<http://www.spec.org/cpu2017/flags/Intel-ic19.0-official-linux64.xml>

<http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revH.xml>

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.0.2 on 2018-12-07 21:20:02-0500.

Report generated on 2020-09-04 14:37:14 by CPU2017 PDF formatter v6255.

Originally published on 2019-01-29.