



# SPEC CPU®2017 Integer Rate Result

Copyright 2017-2023 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS B200 M5 (Intel Xeon Bronze 3104, 1.70 GHz)

SPECrate®2017\_int\_base = 33.4

SPECrate®2017\_int\_peak = 34.8

CPU2017 License: 9019

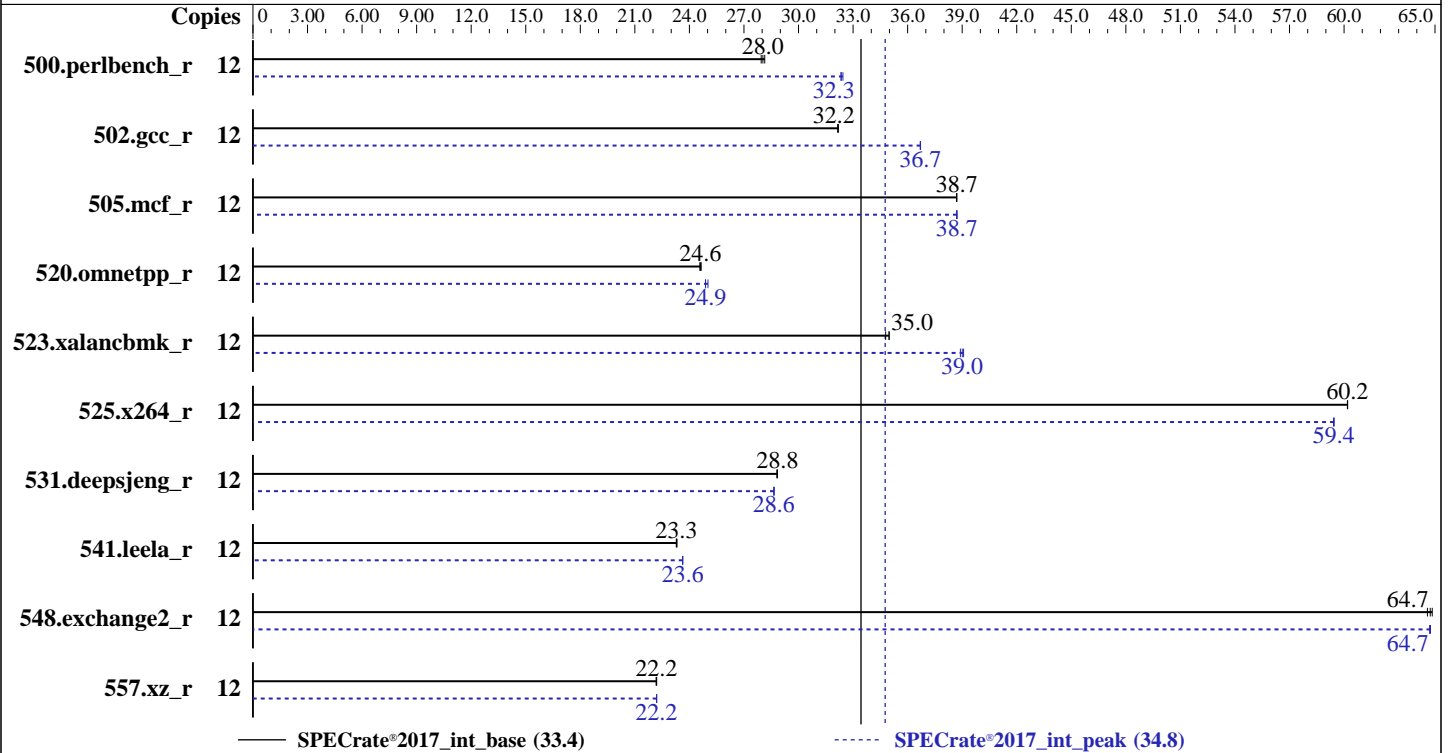
Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Jun-2018

Hardware Availability: Aug-2017

Software Availability: Mar-2018



### Hardware

CPU Name: Intel Xeon Bronze 3104  
 Max MHz: 1700  
 Nominal: 1700  
 Enabled: 12 cores, 2 chips  
 Orderable: 1,2 Chips  
 Cache L1: 32 KB I + 32 KB D on chip per core  
 L2: 1 MB I+D on chip per core  
 L3: 8.25 MB I+D on chip per chip  
 Other: None  
 Memory: 384 GB (24 x 16 GB 2Rx4 PC4-2666V-R, running at 2133)  
 Storage: 1 x 1 TB SAS HDD, 7.2K RPM  
 Other: None

### Software

OS: SUSE Linux Enterprise Server 12 SP2 (x86\_64) 4.4.103-92.56-default  
 Compiler: C/C++: Version 18.0.2.199 of Intel C/C++ Compiler for Linux;  
 Fortran: Version 18.0.2.199 of Intel Fortran Compiler for Linux  
 Parallel: No  
 Firmware: Version 3.2.3c released Mar-2018  
 File System: xfs  
 System State: Run level 3 (multi-user)  
 Base Pointers: 64-bit  
 Peak Pointers: 32/64-bit  
 Other: jemalloc: jemalloc memory allocator library V5.0.1;  
 Power Management: --



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## Results Table

Benchmark	Base							Peak						
	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
500.perlbench_r	12	<b>681</b>	<b>28.0</b>	684	27.9	679	28.1	12	589	32.4	<b>591</b>	<b>32.3</b>	591	32.3
502.gcc_r	12	528	32.2	<b>528</b>	<b>32.2</b>	528	32.2	12	463	36.7	463	36.7	<b>463</b>	<b>36.7</b>
505.mcf_r	12	501	38.7	501	38.7	<b>501</b>	<b>38.7</b>	12	501	38.7	<b>501</b>	<b>38.7</b>	501	38.7
520.omnetpp_r	12	641	24.6	<b>640</b>	<b>24.6</b>	639	24.6	12	629	25.0	633	24.9	<b>633</b>	<b>24.9</b>
523.xalancbmk_r	12	<b>362</b>	<b>35.0</b>	362	35.0	364	34.8	12	<b>325</b>	<b>39.0</b>	326	38.9	324	39.1
525.x264_r	12	349	60.2	349	60.2	<b>349</b>	<b>60.2</b>	12	<b>353</b>	<b>59.4</b>	354	59.4	353	59.4
531.deepsjeng_r	12	477	28.8	<b>477</b>	<b>28.8</b>	477	28.8	12	480	28.6	<b>480</b>	<b>28.6</b>	480	28.7
541.leela_r	12	852	23.3	<b>853</b>	<b>23.3</b>	854	23.3	12	<b>841</b>	<b>23.6</b>	841	23.6	841	23.6
548.exchange2_r	12	<b>486</b>	<b>64.7</b>	485	64.8	487	64.6	12	486	64.8	486	64.7	<b>486</b>	<b>64.7</b>
557.xz_r	12	<b>584</b>	<b>22.2</b>	584	22.2	585	22.2	12	584	22.2	<b>584</b>	<b>22.2</b>	584	22.2

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Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

## Submit Notes

The taskset mechanism was used to bind copies to processors. The config file option 'submit' was used to generate taskset commands to bind each copy to a specific processor. For details, please see the config file.

## Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

## General Notes

Environment variables set by runcpu before the start of the run:

LD\_LIBRARY\_PATH = "/home/cpu2017/lib/ia32:/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-32:/home/cpu2017/je5.0.1-64"

Binaries compiled on a system with 1x Intel Core i7-4790 CPU + 32GB RAM  
memory using Redhat Enterprise Linux 7.4  
Transparent Huge Pages enabled by default  
Prior to runcpu invocation

Filesystem page cache synced and cleared with:

```
sync; echo 3> /proc/sys/vm/drop_caches
```

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

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### General Notes (Continued)

jemalloc: configured and built at default for 32bit (i686) and 64bit (x86\_64) targets;  
jemalloc: built with the RedHat Enterprise 7.4, and the system compiler gcc 4.8.5;  
jemalloc: sources available from jemalloc.net or <https://github.com/jemalloc/jemalloc/releases>

### Platform Notes

BIOS Settings:

CPU performance set to Enterprise  
Power Performance Tuning set to OS Controls  
SNC set to Disabled  
IMC Interleaving set to 1-way Interleave  
Patrol Scrub set to Disabled  
Sysinfo program /home/cpu2017/bin/sysinfo  
Rev: r5797 of 2017-06-14 96c45e4568ad54c135fd618bcc091c0f  
running on linux-uezu Wed Jun 6 07:59:13 2018

SUT (System Under Test) info as seen by some common utilities.  
For more information on this section, see <https://www.spec.org/cpu2017/Docs/config.html#sysinfo>

From /proc/cpuinfo  
model name : Intel(R) Xeon(R) Bronze 3104 CPU @ 1.70GHz  
2 "physical id"s (chips)  
12 "processors"  
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)  
cpu cores : 6  
siblings : 6  
physical 0: cores 0 1 2 3 4 5  
physical 1: cores 0 1 2 3 4 5

From lscpu:  
Architecture: x86\_64  
CPU op-mode(s): 32-bit, 64-bit  
Byte Order: Little Endian  
CPU(s): 12  
On-line CPU(s) list: 0-11  
Thread(s) per core: 1  
Core(s) per socket: 6  
Socket(s): 2  
NUMA node(s): 2  
Vendor ID: GenuineIntel

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### Platform Notes (Continued)

```

CPU family:           6
Model:               85
Model name:         Intel(R) Xeon(R) Bronze 3104 CPU @ 1.70GHz
Stepping:           4
CPU MHz:             1700.000
CPU max MHz:        1700.0000
CPU min MHz:        800.0000
BogoMIPS:           3400.01
Virtualization:     VT-x
L1d cache:          32K
L1i cache:          32K
L2 cache:           1024K
L3 cache:           8448K
NUMA node0 CPU(s): 0-5
NUMA node1 CPU(s): 6-11
Flags:              fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc
aperfmpperf eagerfpu pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg
fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes
xsave avx f16c rdrand lahf_lm abm 3dnowprefetch arat epb invpcid_single pln pts
dtherm hwp hwp_act_window hwp_epp hwp_pkg_req intel_pt spec_ctrl kaiser tpr_shadow
vnm flexpriority ept vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid
rtm cqm mpx avx512f avx512dq rdseed adx smap clflushopt clwb avx512cd avx512bw
avx512vl xsaveopt xsavec xgetbv1 cqm_llc cqm_occup_llc

```

```

/proc/cpuinfo cache data
cache size : 8448 KB

```

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.

```

available: 2 nodes (0-1)
node 0 cpus: 0 1 2 3 4 5
node 0 size: 193018 MB
node 0 free: 192666 MB
node 1 cpus: 6 7 8 9 10 11
node 1 size: 193504 MB
node 1 free: 193164 MB
node distances:
node  0  1
  0:  10  21
  1:  21  10

```

```

From /proc/meminfo
MemTotal:      395799220 kB
HugePages_Total:      0
Hugepagesize:    2048 kB

```

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### Platform Notes (Continued)

```

From /etc/*release* /etc/*version*
SuSE-release:
  SUSE Linux Enterprise Server 12 (x86_64)
  VERSION = 12
  PATCHLEVEL = 2
  # This file is deprecated and will be removed in a future service pack or release.
  # Please check /etc/os-release for details about this release.
os-release:
  NAME="SLES"
  VERSION="12-SP2"
  VERSION_ID="12.2"
  PRETTY_NAME="SUSE Linux Enterprise Server 12 SP2"
  ID="sles"
  ANSI_COLOR="0;32"
  CPE_NAME="cpe:/o:suse:sles:12:sp2"

uname -a:
  Linux linux-uezu 4.4.103-92.56-default #1 SMP Wed Dec 27 16:24:31 UTC 2017 (2fd2155)
  x86_64 x86_64 x86_64 GNU/Linux

run-level 3 Jan 1 10:42

SPEC is set to: /home/cpu2017
Filesystem      Type  Size  Used Avail Use% Mounted on
/dev/sdal        xfs   894G  105G  790G  12% /

Additional information from dmidecode follows.  WARNING: Use caution when you interpret
this section. The 'dmidecode' program reads system data which is "intended to allow
hardware to be accurately determined", but the intent may not be met, as there are
frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
  BIOS Cisco Systems, Inc. B200M5.3.2.3c.0.0307181316 03/07/2018
  Memory:
    24x 0xCE00 M393A2G40EB2-CTD 16 GB 2 rank 2666, configured at 2133

(End of data from sysinfo program)

```

### Compiler Version Notes

```

=====
C      | 500.perlbench_r(base, peak) 502.gcc_r(base, peak) 505.mcf_r(base,
      | peak) 525.x264_r(base, peak) 557.xz_r(base, peak)
-----
icc (ICC) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
-----

```

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## Compiler Version Notes (Continued)

```

=====
C++      | 520.omnetpp_r(base, peak) 523.xalanbmk_r(base, peak)
         | 531.deepsjeng_r(base, peak) 541.leela_r(base, peak)
=====

```

```

icpc (ICC) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
=====

```

```

=====
Fortran | 548.exchange2_r(base, peak)
=====

```

```

ifort (IFORT) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
=====

```

## Base Compiler Invocation

C benchmarks:

icc -m64 -std=c11

C++ benchmarks:

icpc -m64

Fortran benchmarks:

ifort -m64

## Base Portability Flags

```

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -DSPEC_LP64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalanbmk_r: -DSPEC_LP64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64

```



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## Base Optimization Flags

C benchmarks:

```
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div  
-qopt-mem-layout-trans=3 -L/home/cpu2017/je5.0.1-64/ -ljemalloc
```

C++ benchmarks:

```
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div  
-qopt-mem-layout-trans=3 -L/home/cpu2017/je5.0.1-64/ -ljemalloc
```

Fortran benchmarks:

```
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div  
-qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte  
-L/home/cpu2017/je5.0.1-64/ -ljemalloc
```

## Peak Compiler Invocation

C benchmarks (except as noted below):

```
icc -m64 -std=c11
```

```
502.gcc_r: icc -m32 -std=c11 -L/opt/intel/compilers_and_libraries_2018/linux/lib/ia32
```

C++ benchmarks (except as noted below):

```
icpc -m64
```

```
523.xalancbmk_r: icpc -m32 -L/opt/intel/compilers_and_libraries_2018/linux/lib/ia32
```

Fortran benchmarks:

```
ifort -m64
```

## Peak Portability Flags

```
500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
```

```
502.gcc_r: -D_FILE_OFFSET_BITS=64
```

```
505.mcf_r: -DSPEC_LP64
```

```
520.omnetpp_r: -DSPEC_LP64
```

```
523.xalancbmk_r: -D_FILE_OFFSET_BITS=64 -DSPEC_LINUX
```

```
525.x264_r: -DSPEC_LP64
```

```
531.deepsjeng_r: -DSPEC_LP64
```

```
541.leela_r: -DSPEC_LP64
```

```
548.exchange2_r: -DSPEC_LP64
```

```
557.xz_r: -DSPEC_LP64
```



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## Peak Optimization Flags

C benchmarks:

```
500.perlbench_r: -w1,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo  
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3  
-fno-strict-overflow -L/home/cpu2017/je5.0.1-64/  
-ljemalloc
```

```
502.gcc_r: -w1,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo  
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3  
-L/home/cpu2017/je5.0.1-32/ -ljemalloc
```

```
505.mcf_r: -w1,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div  
-qopt-mem-layout-trans=3 -L/home/cpu2017/je5.0.1-64/  
-ljemalloc
```

```
525.x264_r: -w1,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div  
-qopt-mem-layout-trans=3 -fno-alias  
-L/home/cpu2017/je5.0.1-64/ -ljemalloc
```

557.xz\_r: Same as 505.mcf\_r

C++ benchmarks:

```
520.omnetpp_r: -w1,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo  
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3  
-L/home/cpu2017/je5.0.1-64/ -ljemalloc
```

```
523.xalancbmk_r: -w1,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo  
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3  
-L/home/cpu2017/je5.0.1-32/ -ljemalloc
```

531.deepsjeng\_r: Same as 520.omnetpp\_r

541.leela\_r: Same as 520.omnetpp\_r

Fortran benchmarks:

```
-w1,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div  
-qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte  
-L/home/cpu2017/je5.0.1-64/ -ljemalloc
```

The flags files that were used to format this result can be browsed at

<http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.2018-06-13.html>

<http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revH.html>





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You can also download the XML flags sources by saving the following links:

<http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.2018-06-13.xml>

<http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revH.xml>

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