



# SPEC CPU®2017 Floating Point Speed Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS B480 M5 (Intel Xeon Gold 6136, 3.00 GHz)

SPECspeed®2017\_fp\_base = 149

SPECspeed®2017\_fp\_peak = 151

CPU2017 License: 9019

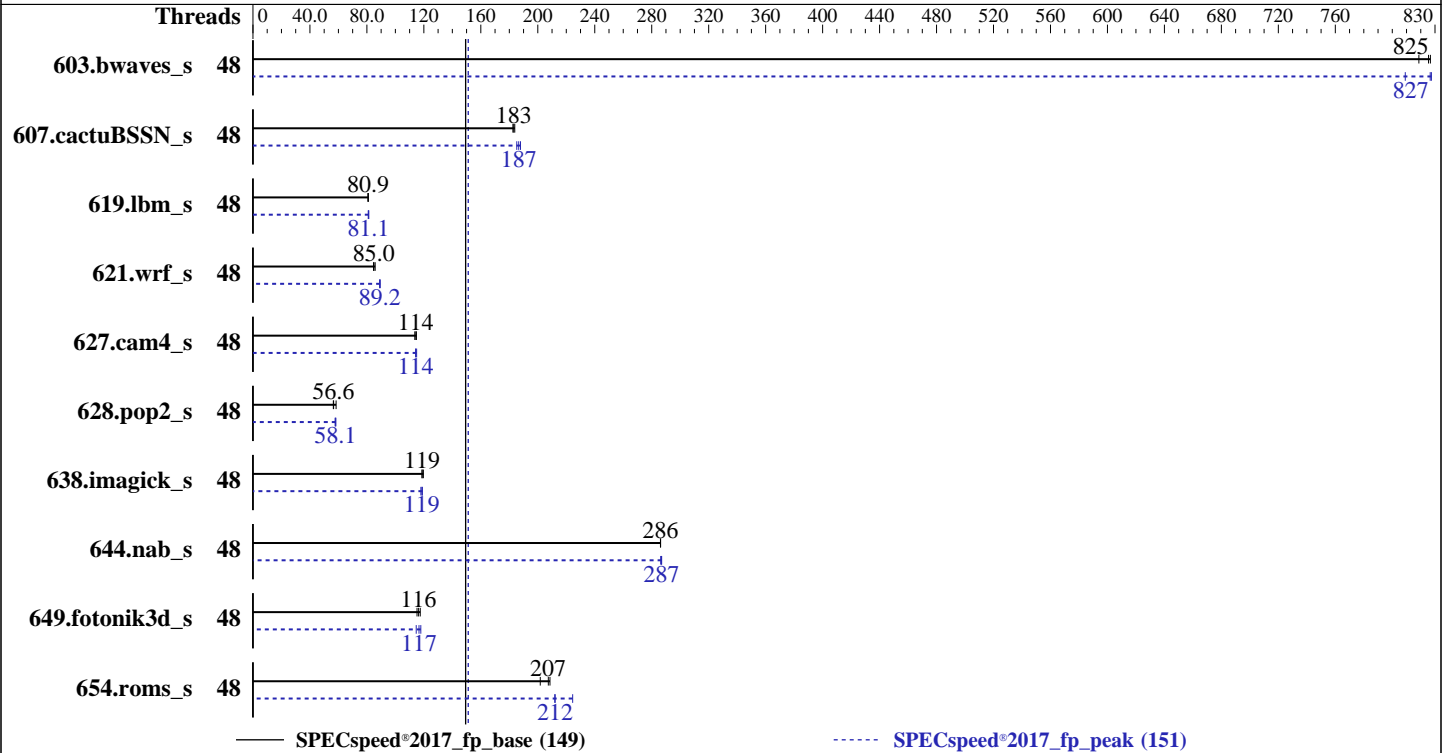
Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Nov-2017

Hardware Availability: Aug-2017

Software Availability: Sep-2017



### Hardware

CPU Name: Intel Xeon Gold 6136  
 Max MHz: 3700  
 Nominal: 3000  
 Enabled: 48 cores, 4 chips  
 Orderable: 2,4 Chips  
 Cache L1: 32 KB I + 32 KB D on chip per core  
 L2: 1 MB I+D on chip per core  
 L3: 24.75 MB I+D on chip per chip  
 Other: None  
 Memory: 768 GB (48 x 16 GB 2Rx4 PC4-2666V-R)  
 Storage: 1 x 1 TB SAS HDD, 7.2K RPM  
 Other: None

### Software

OS: SUSE Linux Enterprise Server 12 SP2 (x86\_64) 4.4.21-69-default  
 Compiler: C/C++: Version 18.0.0.128 of Intel C/C++ Compiler for Linux;  
 Fortran: Version 18.0.0.128 of Intel Fortran Compiler for Linux  
 Parallel: Yes  
 Firmware: Version 3.2.0 released Apr-2017  
 File System: xfs  
 System State: Run level 3 (multi-user)  
 Base Pointers: 64-bit  
 Peak Pointers: 64-bit  
 Other: None  
 Power Management: --



# SPEC CPU®2017 Floating Point Speed Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS B480 M5 (Intel Xeon Gold 6136, 3.00 GHz)

SPECSpeed®2017\_fp\_base = 149

SPECSpeed®2017\_fp\_peak = 151

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems

**Test Date:** Nov-2017  
**Hardware Availability:** Aug-2017  
**Software Availability:** Sep-2017

## Results Table

Benchmark	Base							Peak						
	Threads	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Threads	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
603.bwaves_s	48	71.4	827	72.1	819	<u>71.5</u>	<u>825</u>	48	72.9	809	71.3	827	<u>71.4</u>	<u>827</u>
607.cactuBSSN_s	48	90.7	184	<u>91.0</u>	<u>183</u>	91.3	183	48	90.0	185	<u>89.3</u>	<u>187</u>	88.7	188
619.lbm_s	48	64.8	80.8	<u>64.8</u>	<u>80.9</u>	64.7	81.0	48	64.7	80.9	<u>64.5</u>	<u>81.1</u>	64.4	81.3
621.wrf_s	48	156	84.6	<u>156</u>	<u>85.0</u>	154	85.8	48	149	88.9	<u>148</u>	<u>89.2</u>	148	89.3
627.cam4_s	48	<u>77.5</u>	<u>114</u>	78.0	114	77.2	115	48	77.6	114	77.1	115	<u>77.5</u>	<u>114</u>
628.pop2_s	48	203	58.4	210	56.4	<u>210</u>	<u>56.6</u>	48	204	58.2	206	57.7	<u>205</u>	<u>58.1</u>
638.imagick_s	48	<u>121</u>	<u>119</u>	121	119	121	120	48	<u>122</u>	<u>119</u>	121	119	122	118
644.nab_s	48	<u>61.0</u>	<u>286</u>	61.0	286	61.1	286	48	60.9	287	<u>60.9</u>	<u>287</u>	61.0	286
649.fotonik3d_s	48	79.1	115	<u>78.4</u>	<u>116</u>	77.6	117	48	<u>78.2</u>	<u>117</u>	77.3	118	79.5	115
654.roms_s	48	75.5	209	78.0	202	<u>75.9</u>	<u>207</u>	48	<u>74.2</u>	<u>212</u>	70.1	224	74.3	212

SPECSpeed®2017\_fp\_base = **149**

SPECSpeed®2017\_fp\_peak = **151**

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

## Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

## General Notes

Environment variables set by runcpu before the start of the run:

KMP\_AFFINITY = "granularity=fine,compact"

LD\_LIBRARY\_PATH = "/home/cpu2017/lib/ia32:/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-32:/home/cpu2017/je5.0.1-64"

OMP\_STACKSIZE = "192M"

Binaries compiled on a system with 1x Intel Core i7-4790 CPU + 32GB RAM

memory using Redhat Enterprise Linux 7.4

Transparent Huge Pages enabled by default

Prior to runcpu invocation

Filesystem page cache synced and cleared with:

```
sync; echo 3> /proc/sys/vm/drop_caches
```

## Platform Notes

BIOS Settings:

Intel HyperThreading Technology set to Disabled

CPU performance set to Enterprise

Power Performance Tuning set to OS

SNC set to Disabled

IMC Interleaving set to Auto

Patrol Scrub set to Disabled

Sysinfo program /home/cpu2017/bin/sysinfo

Rev: r5797 of 2017-06-14 96c45e4568ad54c135fd618bcc091c0f

(Continued on next page)



# SPEC CPU®2017 Floating Point Speed Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS B480 M5 (Intel Xeon Gold 6136, 3.00 GHz)

SPECspeed®2017\_fp\_base = 149

SPECspeed®2017\_fp\_peak = 151

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems

**Test Date:** Nov-2017  
**Hardware Availability:** Aug-2017  
**Software Availability:** Sep-2017

### Platform Notes (Continued)

running on linux-0vth Mon Nov 27 09:31:54 2017

SUT (System Under Test) info as seen by some common utilities.  
For more information on this section, see  
<https://www.spec.org/cpu2017/Docs/config.html#sysinfo>

From /proc/cpuinfo

```
model name : Intel(R) Xeon(R) Gold 6136 CPU @ 3.00GHz
 4 "physical id"s (chips)
 48 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following
excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 12
siblings : 12
physical 0: cores 0 3 4 5 6 7 16 18 19 20 21 22
physical 1: cores 0 1 2 3 4 8 9 11 17 18 19 20
physical 2: cores 0 1 2 3 4 8 9 11 17 18 19 20
physical 3: cores 0 1 2 3 4 9 10 16 18 19 25 26
```

From lscpu:

```
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 48
On-line CPU(s) list: 0-47
Thread(s) per core: 1
Core(s) per socket: 12
Socket(s): 4
NUMA node(s): 4
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Gold 6136 CPU @ 3.00GHz
Stepping: 4
CPU MHz: 3700.499
CPU max MHz: 3700.0000
CPU min MHz: 1200.0000
BogoMIPS: 5985.89
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 25344K
NUMA node0 CPU(s): 0-11
NUMA node1 CPU(s): 12-23
NUMA node2 CPU(s): 24-35
NUMA node3 CPU(s): 36-47
```

(Continued on next page)



# SPEC CPU®2017 Floating Point Speed Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS B480 M5 (Intel Xeon Gold 6136, 3.00 GHz)

SPECspeed®2017\_fp\_base = 149

SPECspeed®2017\_fp\_peak = 151

CPU2017 License: 9019

Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Nov-2017

Hardware Availability: Aug-2017

Software Availability: Sep-2017

### Platform Notes (Continued)

Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant\_tsc art arch\_perfmon pebs bts rep\_good nopl xtopology nonstop\_tsc aperfmperf eagerfpu pni pclmulqdq dtes64 monitor ds\_cpl vmx smx est tm2 sse3 sdbg fma cx16 xtpr pdcm pcid dca sse4\_1 sse4\_2 x2apic movbe popcnt tsc\_deadline\_timer aes xsave avx f16c rdrand lahf\_lm abm 3dnowprefetch ida arat epb pln pts dtherm hwp hwp\_act\_window hwp\_epp hwp\_pkg\_req intel\_pt tpr\_shadow vnmi flexpriority ept vpid fsgsbase tsc\_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm cqm mpx avx512f avx512dq rdseed adx smap clflushopt clwb avx512cd avx512bw avx512vl xsaveopt xsavec xgetbv1 cqm\_llc cqm\_occup\_llc

```
/proc/cpuinfo cache data
cache size : 25344 KB
```

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.

```
available: 4 nodes (0-3)
node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11
node 0 size: 191928 MB
node 0 free: 190709 MB
node 1 cpus: 12 13 14 15 16 17 18 19 20 21 22 23
node 1 size: 193521 MB
node 1 free: 188814 MB
node 2 cpus: 24 25 26 27 28 29 30 31 32 33 34 35
node 2 size: 193521 MB
node 2 free: 191879 MB
node 3 cpus: 36 37 38 39 40 41 42 43 44 45 46 47
node 3 size: 193518 MB
node 3 free: 191835 MB
node distances:
node 0 1 2 3
0: 10 21 21 21
1: 21 10 21 21
2: 21 21 10 21
3: 21 21 21 10
```

```
From /proc/meminfo
MemTotal: 791029516 kB
HugePages_Total: 0
Hugepagesize: 2048 kB
```

From /etc/\*release\* /etc/\*version\*

```
SuSE-release:
SUSE Linux Enterprise Server 12 (x86_64)
VERSION = 12
PATCHLEVEL = 2
# This file is deprecated and will be removed in a future service pack or release.
```

(Continued on next page)



# SPEC CPU®2017 Floating Point Speed Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS B480 M5 (Intel Xeon Gold 6136, 3.00 GHz)

SPECspeed®2017\_fp\_base = 149

SPECspeed®2017\_fp\_peak = 151

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems

**Test Date:** Nov-2017  
**Hardware Availability:** Aug-2017  
**Software Availability:** Sep-2017

### Platform Notes (Continued)

# Please check /etc/os-release for details about this release.

os-release:

```
NAME="SLES"
VERSION="12-SP2"
VERSION_ID="12.2"
PRETTY_NAME="SUSE Linux Enterprise Server 12 SP2"
ID="sles"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:12:sp2"
```

uname -a:

```
Linux linux-0vth 4.4.21-69-default #1 SMP Tue Oct 25 10:58:20 UTC 2016 (9464f67)
x86_64 x86_64 x86_64 GNU/Linux
```

run-level 3 Jan 4 06:46

SPEC is set to: /home/cpu2017

```
Filesystem      Type  Size  Used Avail Use% Mounted on
/dev/sda1       xfs   280G   94G  186G  34% /
```

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

BIOS Cisco Systems, Inc. B480M5.3.2.0.176.0425171408 04/25/2017

Memory:

48x 0xCE00 M393A2G40EB2-CTD 16 GB 2 rank 2666

(End of data from sysinfo program)

### Compiler Version Notes

```
=====  
C          | 619.lbm_s(base, peak) 638.imagick_s(base, peak)  
          | 644.nab_s(base, peak)  
-----
```

icc (ICC) 18.0.0 20170811

Copyright (C) 1985-2017 Intel Corporation. All rights reserved.

```
=====  
C++, C, Fortran | 607.cactuBSSN_s(base, peak)  
-----
```

icpc (ICC) 18.0.0 20170811

Copyright (C) 1985-2017 Intel Corporation. All rights reserved.

icc (ICC) 18.0.0 20170811

(Continued on next page)



# SPEC CPU®2017 Floating Point Speed Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS B480 M5 (Intel Xeon Gold 6136, 3.00 GHz)

SPECspeed®2017\_fp\_base = 149

SPECspeed®2017\_fp\_peak = 151

**CPU2017 License:** 9019

**Test Sponsor:** Cisco Systems

**Tested by:** Cisco Systems

**Test Date:** Nov-2017

**Hardware Availability:** Aug-2017

**Software Availability:** Sep-2017

## Compiler Version Notes (Continued)

Copyright (C) 1985-2017 Intel Corporation. All rights reserved.

ifort (IFORT) 18.0.0 20170811

Copyright (C) 1985-2017 Intel Corporation. All rights reserved.

-----  
Fortran | 603.bwaves\_s(base, peak) 649.fotonik3d\_s(base, peak)  
654.roms\_s(base, peak)

ifort (IFORT) 18.0.0 20170811

Copyright (C) 1985-2017 Intel Corporation. All rights reserved.

-----  
Fortran, C | 621.wrf\_s(base, peak) 627.cam4\_s(base, peak)  
628.pop2\_s(base, peak)

ifort (IFORT) 18.0.0 20170811

Copyright (C) 1985-2017 Intel Corporation. All rights reserved.

icc (ICC) 18.0.0 20170811

Copyright (C) 1985-2017 Intel Corporation. All rights reserved.

## Base Compiler Invocation

C benchmarks:

icc

Fortran benchmarks:

ifort

Benchmarks using both Fortran and C:

ifort icc

Benchmarks using Fortran, C, and C++:

icpc icc ifort

## Base Portability Flags

603.bwaves\_s: -DSPEC\_LP64

607.cactuBSSN\_s: -DSPEC\_LP64

619.lbm\_s: -DSPEC\_LP64

621.wrf\_s: -DSPEC\_LP64 -DSPEC\_CASE\_FLAG -convert big\_endian

(Continued on next page)



# SPEC CPU®2017 Floating Point Speed Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

**Cisco Systems**

Cisco UCS B480 M5 (Intel Xeon Gold 6136,  
3.00 GHz)

SPECspeed®2017\_fp\_base = 149

SPECspeed®2017\_fp\_peak = 151

**CPU2017 License:** 9019

**Test Sponsor:** Cisco Systems

**Tested by:** Cisco Systems

**Test Date:** Nov-2017

**Hardware Availability:** Aug-2017

**Software Availability:** Sep-2017

## Base Portability Flags (Continued)

```
627.cam4_s: -DSPEC_LP64 -DSPEC_CASE_FLAG
628.pop2_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
-assume byterecl
638.imagick_s: -DSPEC_LP64
644.nab_s: -DSPEC_LP64
649.fotonik3d_s: -DSPEC_LP64
654.roms_s: -DSPEC_LP64
```

## Base Optimization Flags

C benchmarks:

```
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp -DSPEC_OPENMP
```

Fortran benchmarks:

```
-DSPEC_OPENMP -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp
-nostandard-realloc-lhs -align array32byte
```

Benchmarks using both Fortran and C:

```
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp -DSPEC_OPENMP
-nostandard-realloc-lhs -align array32byte
```

Benchmarks using Fortran, C, and C++:

```
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp -DSPEC_OPENMP
-nostandard-realloc-lhs -align array32byte
```

## Base Other Flags

C benchmarks:

```
-m64 -std=c11
```

Fortran benchmarks:

```
-m64
```

Benchmarks using both Fortran and C:

```
-m64 -std=c11
```

Benchmarks using Fortran, C, and C++:

```
-m64 -std=c11
```



# SPEC CPU®2017 Floating Point Speed Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS B480 M5 (Intel Xeon Gold 6136, 3.00 GHz)

SPECspeed®2017\_fp\_base = 149

SPECspeed®2017\_fp\_peak = 151

**CPU2017 License:** 9019

**Test Sponsor:** Cisco Systems

**Tested by:** Cisco Systems

**Test Date:** Nov-2017

**Hardware Availability:** Aug-2017

**Software Availability:** Sep-2017

## Peak Compiler Invocation

C benchmarks:

icc

Fortran benchmarks:

ifort

Benchmarks using both Fortran and C:

ifort icc

Benchmarks using Fortran, C, and C++:

icpc icc ifort

## Peak Portability Flags

Same as Base Portability Flags

## Peak Optimization Flags

C benchmarks:

```
619.lbm_s: -prof-gen(pass 1) -prof-use(pass 2) -O2 -xCORE-AVX512
-qopt-prefetch -ipo -O3 -ffinite-math-only -no-prec-div
-qopt-mem-layout-trans=3 -DSPEC_SUPPRESS_OPENMP -qopenmp
-DSPEC_OPENMP
```

```
638.imagick_s: -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp
-DSPEC_OPENMP
```

644.nab\_s: Same as 638.imagick\_s

Fortran benchmarks:

```
-prof-gen(pass 1) -prof-use(pass 2) -DSPEC_SUPPRESS_OPENMP
-DSPEC_OPENMP -O2 -xCORE-AVX512 -qopt-prefetch -ipo -O3
-ffinite-math-only -no-prec-div -qopt-mem-layout-trans=3 -qopenmp
-nostandard-realloc-lhs -align array32byte
```

Benchmarks using both Fortran and C:

```
621.wrf_s: -prof-gen(pass 1) -prof-use(pass 2) -O2 -xCORE-AVX512
-qopt-prefetch -ipo -O3 -ffinite-math-only -no-prec-div
-qopt-mem-layout-trans=3 -DSPEC_SUPPRESS_OPENMP -qopenmp
```

(Continued on next page)





# SPEC CPU®2017 Floating Point Speed Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS B480 M5 (Intel Xeon Gold 6136, 3.00 GHz)

SPECSpeed®2017\_fp\_base = 149

SPECSpeed®2017\_fp\_peak = 151

**CPU2017 License:** 9019

**Test Sponsor:** Cisco Systems

**Tested by:** Cisco Systems

**Test Date:** Nov-2017

**Hardware Availability:** Aug-2017

**Software Availability:** Sep-2017

## Peak Optimization Flags (Continued)

621.wrf\_s (continued):

```
-DSPEC_OPENMP -nostandard-realloc-lhs -align array32byte
```

627.cam4\_s: -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch

```
-ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp
```

```
-DSPEC_OPENMP -nostandard-realloc-lhs -align array32byte
```

628.pop2\_s: Same as 621.wrf\_s

Benchmarks using Fortran, C, and C++:

```
-prof-gen(pass 1) -prof-use(pass 2) -O2 -xCORE-AVX512 -qopt-prefetch
```

```
-ipo -O3 -ffinite-math-only -no-prec-div -qopt-mem-layout-trans=3
```

```
-DSPEC_SUPPRESS_OPENMP -qopenmp -DSPEC_OPENMP -nostandard-realloc-lhs
```

```
-align array32byte
```

## Peak Other Flags

C benchmarks:

```
-m64 -std=c11
```

Fortran benchmarks:

```
-m64
```

Benchmarks using both Fortran and C:

```
-m64 -std=c11
```

Benchmarks using Fortran, C, and C++:

```
-m64 -std=c11
```

The flags files that were used to format this result can be browsed at

<http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.html>

<http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revH.html>

You can also download the XML flags sources by saving the following links:

<http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.xml>

<http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revH.xml>

SPEC CPU and SPECSpeed are registered trademarks of the Standard Performance Evaluation Corporation. All other brand and product names appearing in this result are trademarks or registered trademarks of their respective holders.

For questions about this result, please contact the tester. For other inquiries, please contact [info@spec.org](mailto:info@spec.org).

Tested with SPEC CPU®2017 v1.0.2 on 2017-11-27 09:31:53-0500.

Report generated on 2020-06-25 15:56:54 by CPU2017 PDF formatter v6255.

Originally published on 2017-12-26.