

# Avoiding hot-spots on two-level direct networks



Abhinav Bhatele, Nikhil Jain, William D. Gropp, Laxmikant V. Kale

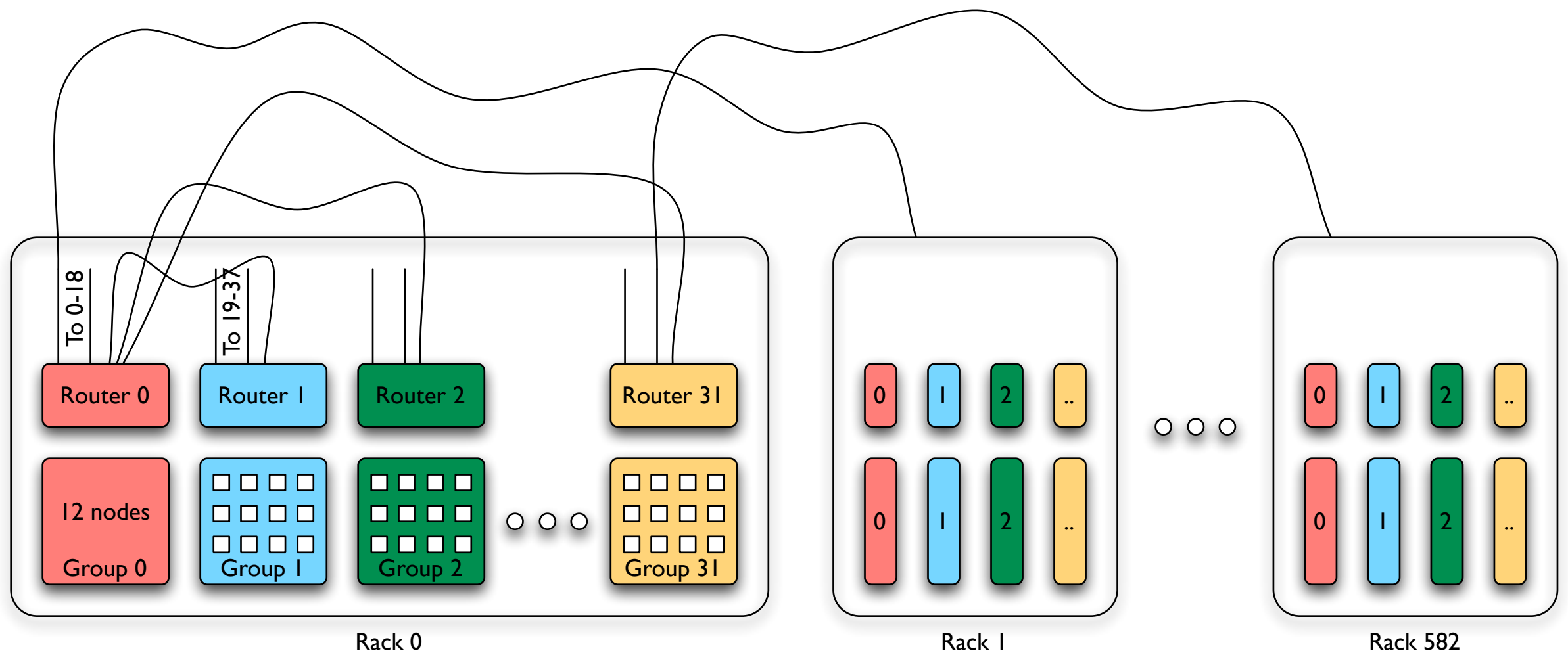


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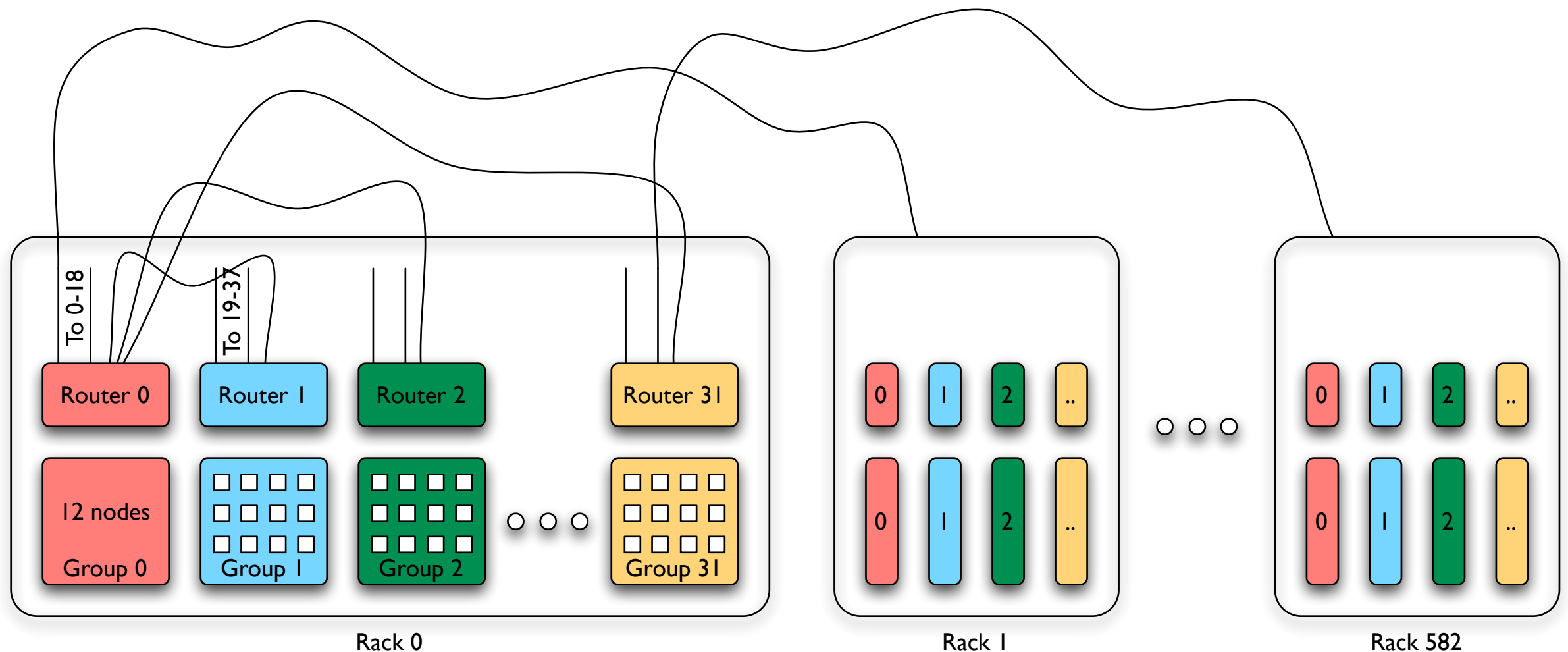


# Interconnects for exascale



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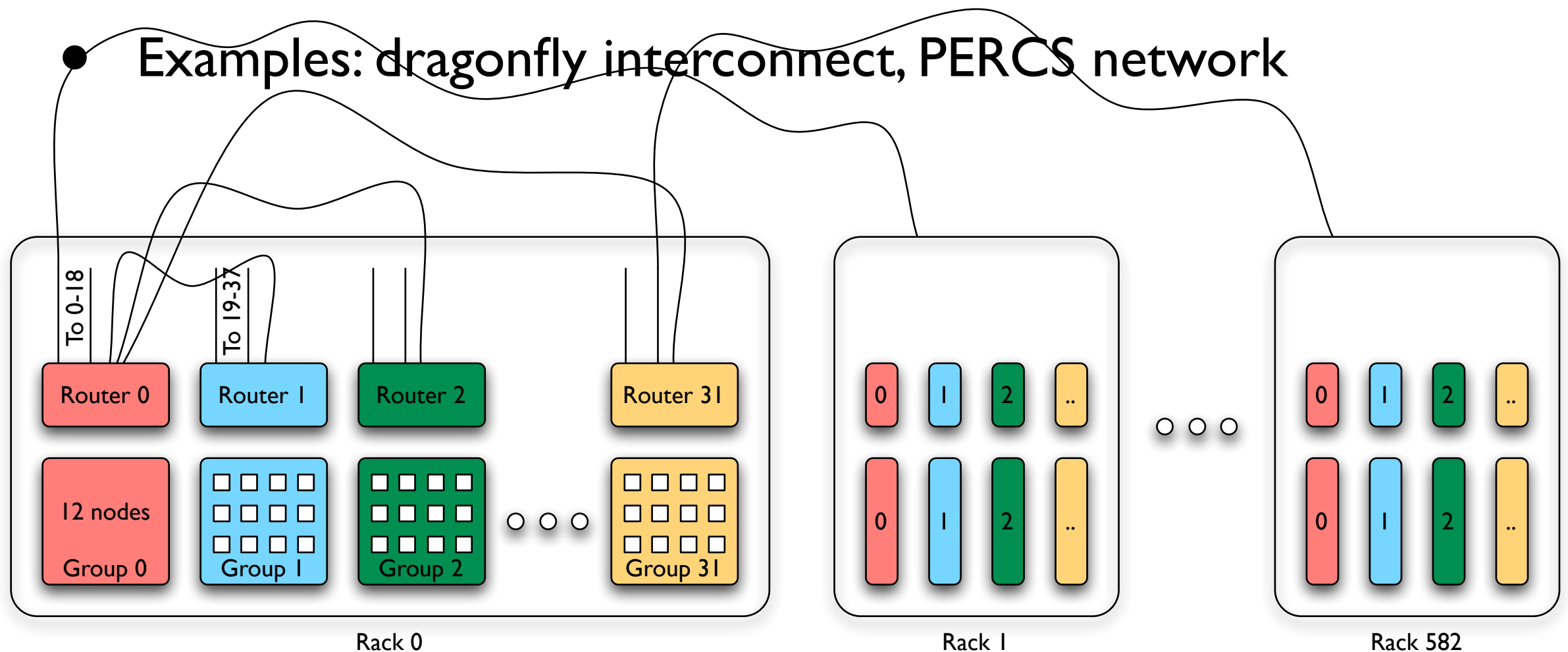
- Multi-level direct (all-to-all connection) networks
  - Higher bandwidth links at lower levels
  - Low diameter: few hops on the average



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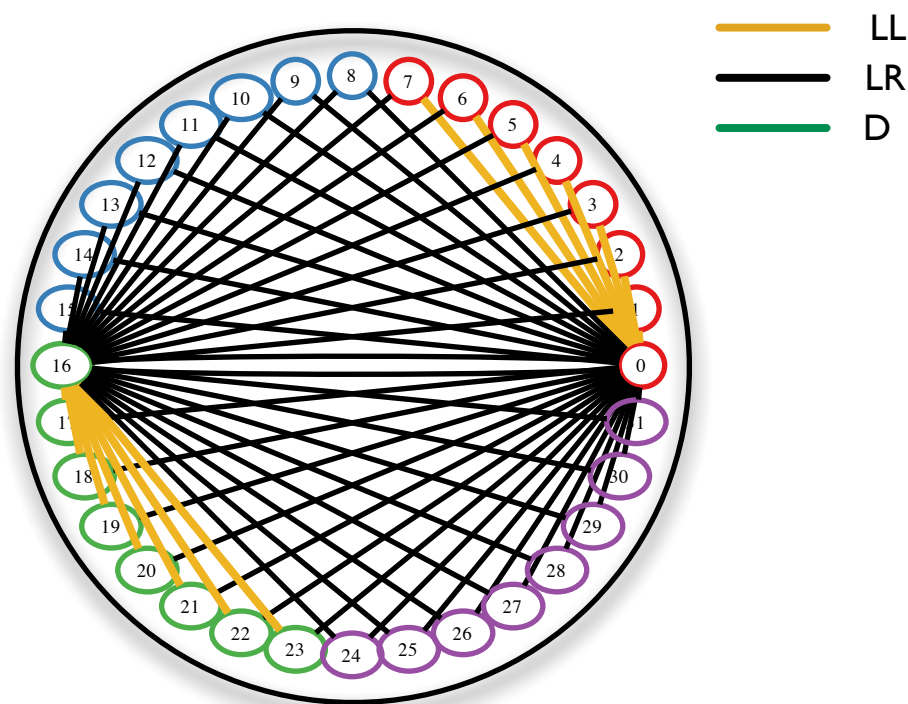
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- Examples: dragonfly interconnect, PERCS network



# IBM's PERCS network

- Each QCM has four 8-core POWER7 chips, 8 such QCMs form a drawer, 4 drawers form a supernode
- Two-level network with 512 supernodes
- Three types of links: LL (24 GB/s), LR (5 GB/s), D (10 GB/s)

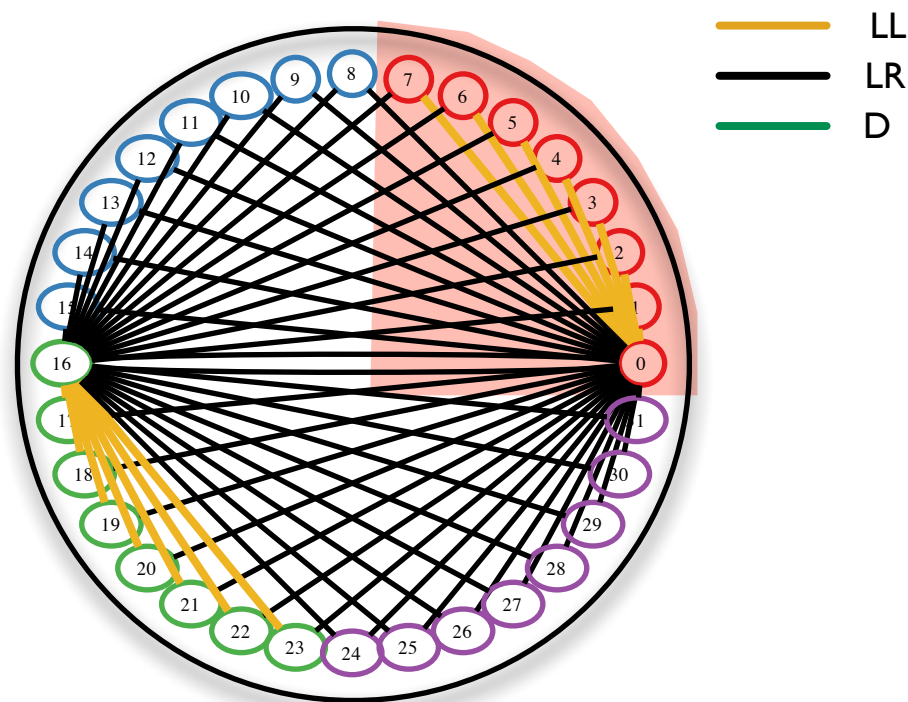


One supernode in the PERCS topology



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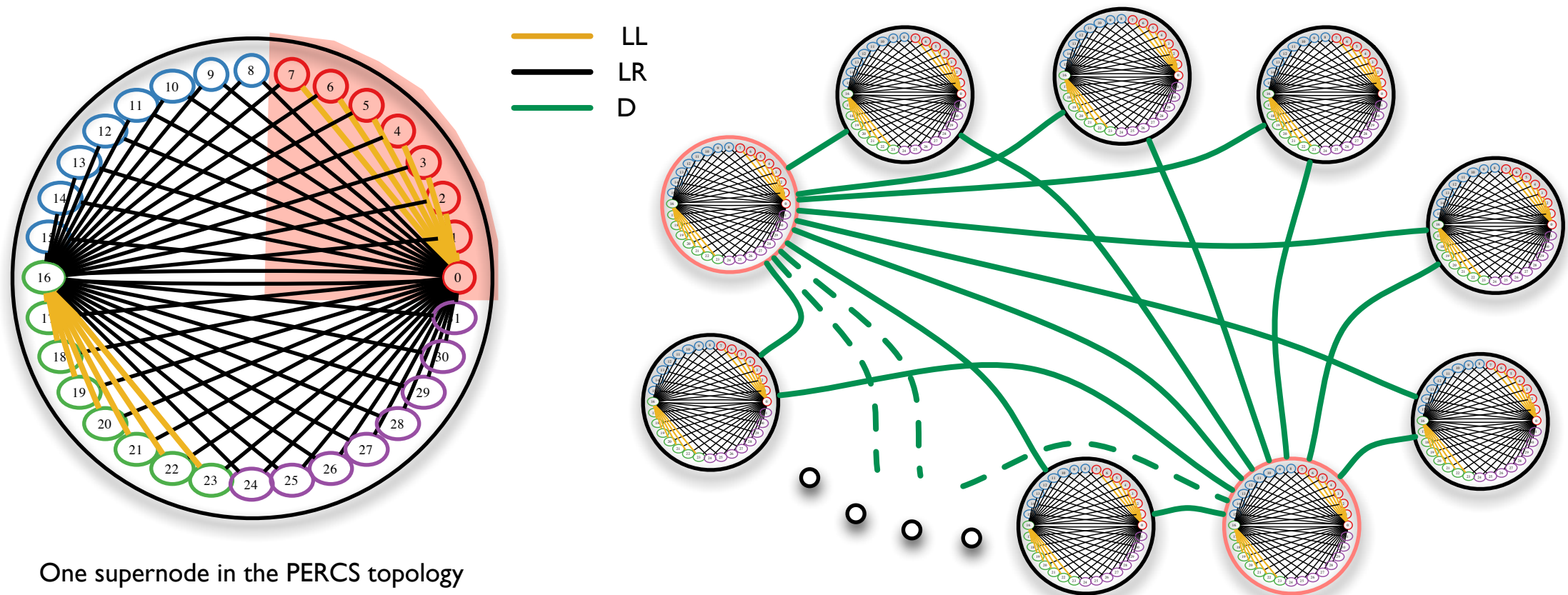
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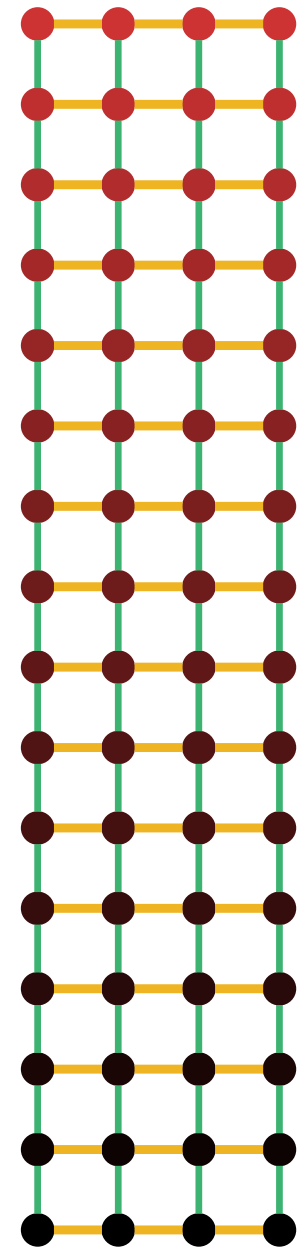
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# The 'D' link bottleneck

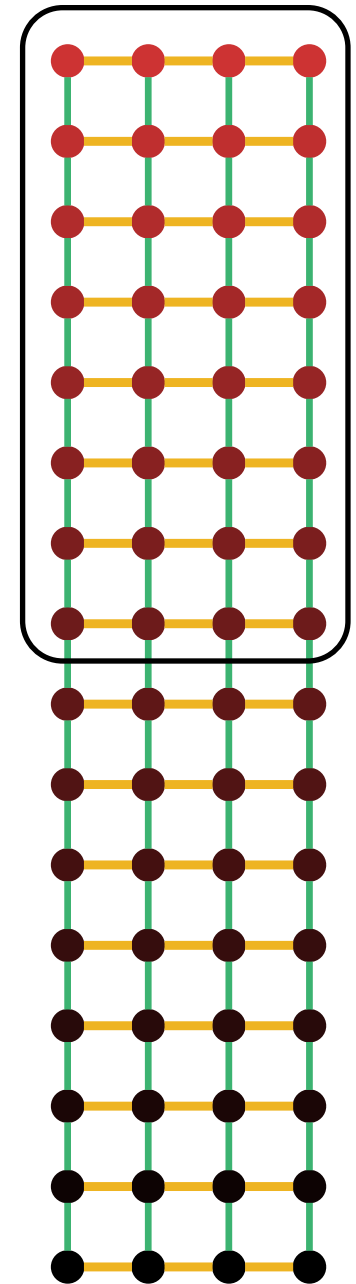
- Lets say we want to run a 2D Stencil on 2 supernodes (64 QCMs)
- Application communication graph: 16 x 4
- MPI-rank ordered mapping leads to significant contention on the **single** D link
- This is true for running any application with  $O(1)$  communicating partners per MPI process





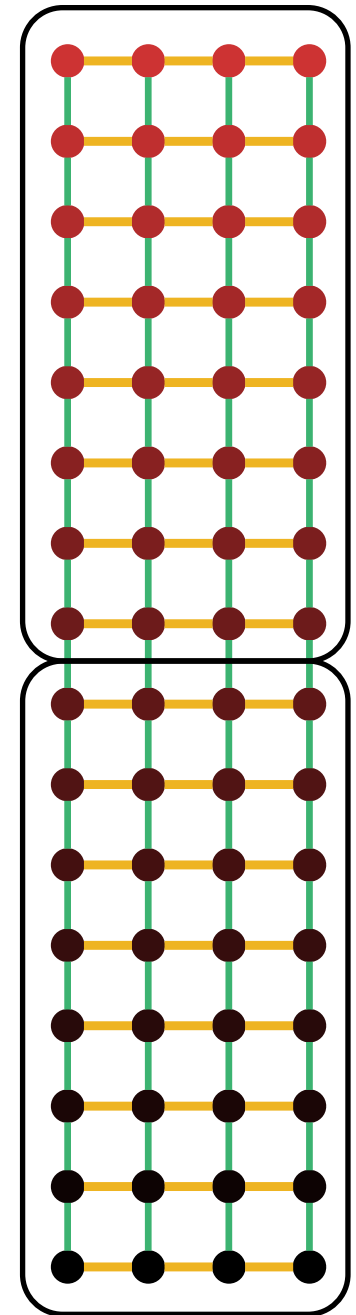
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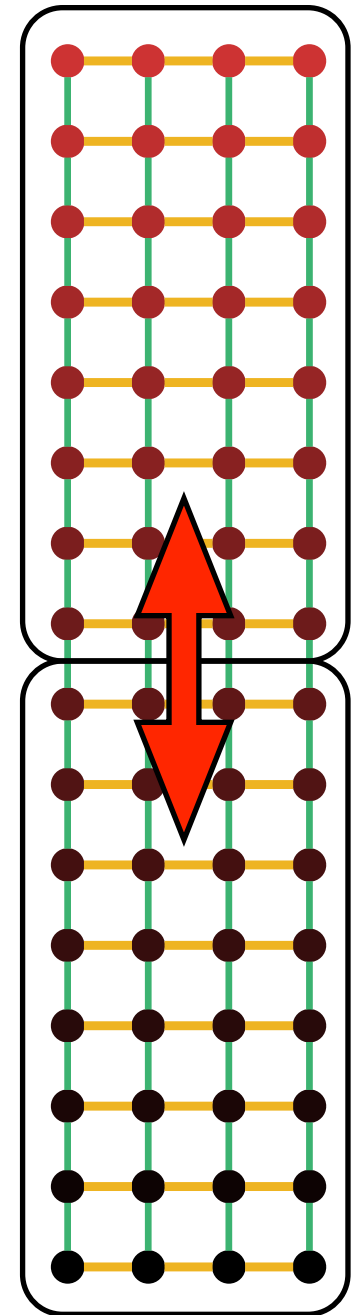
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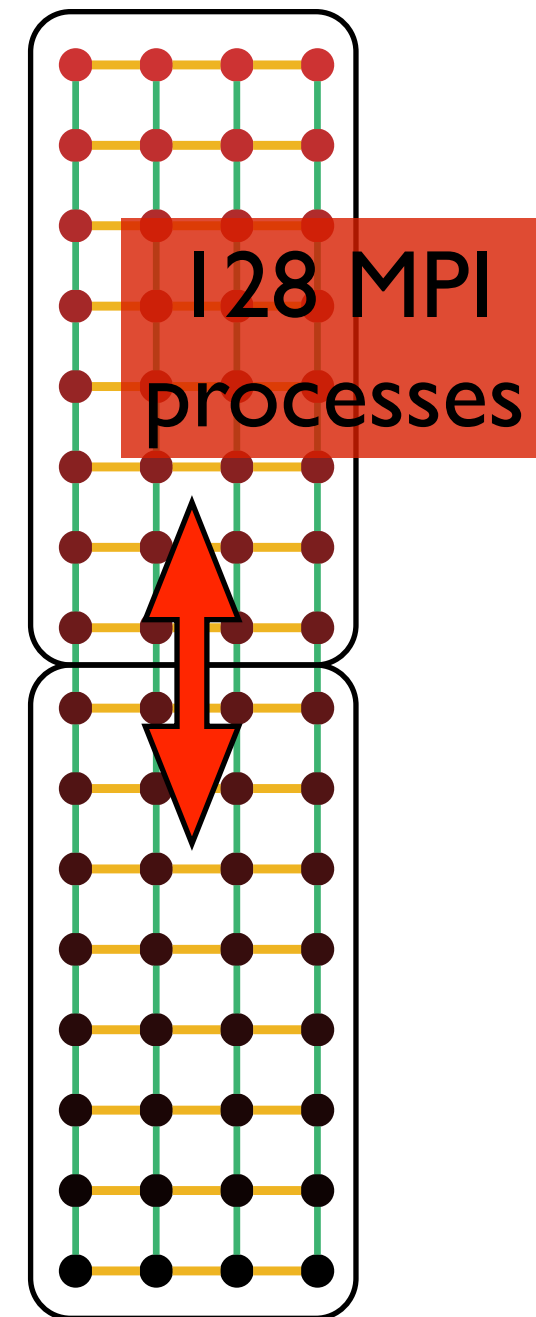
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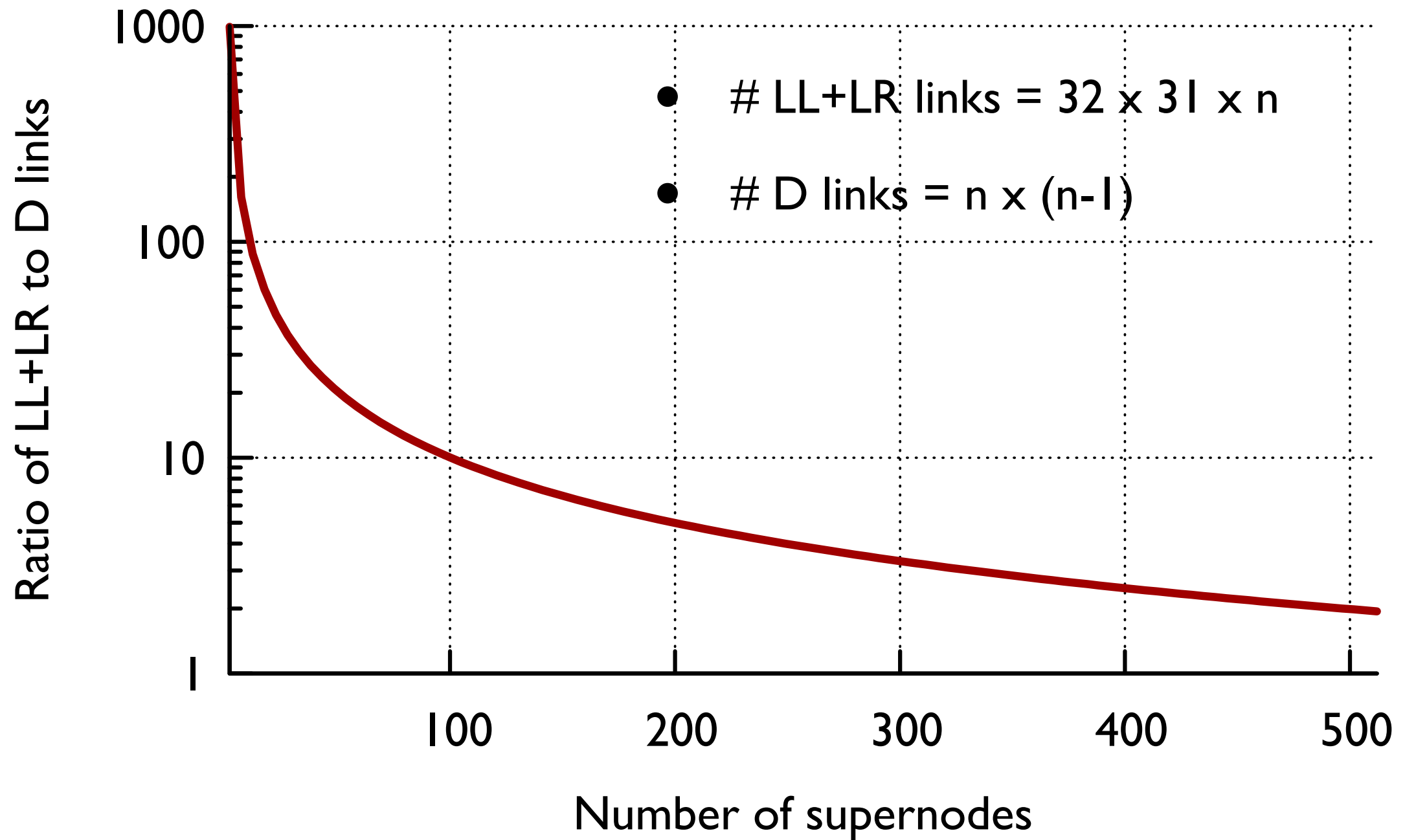


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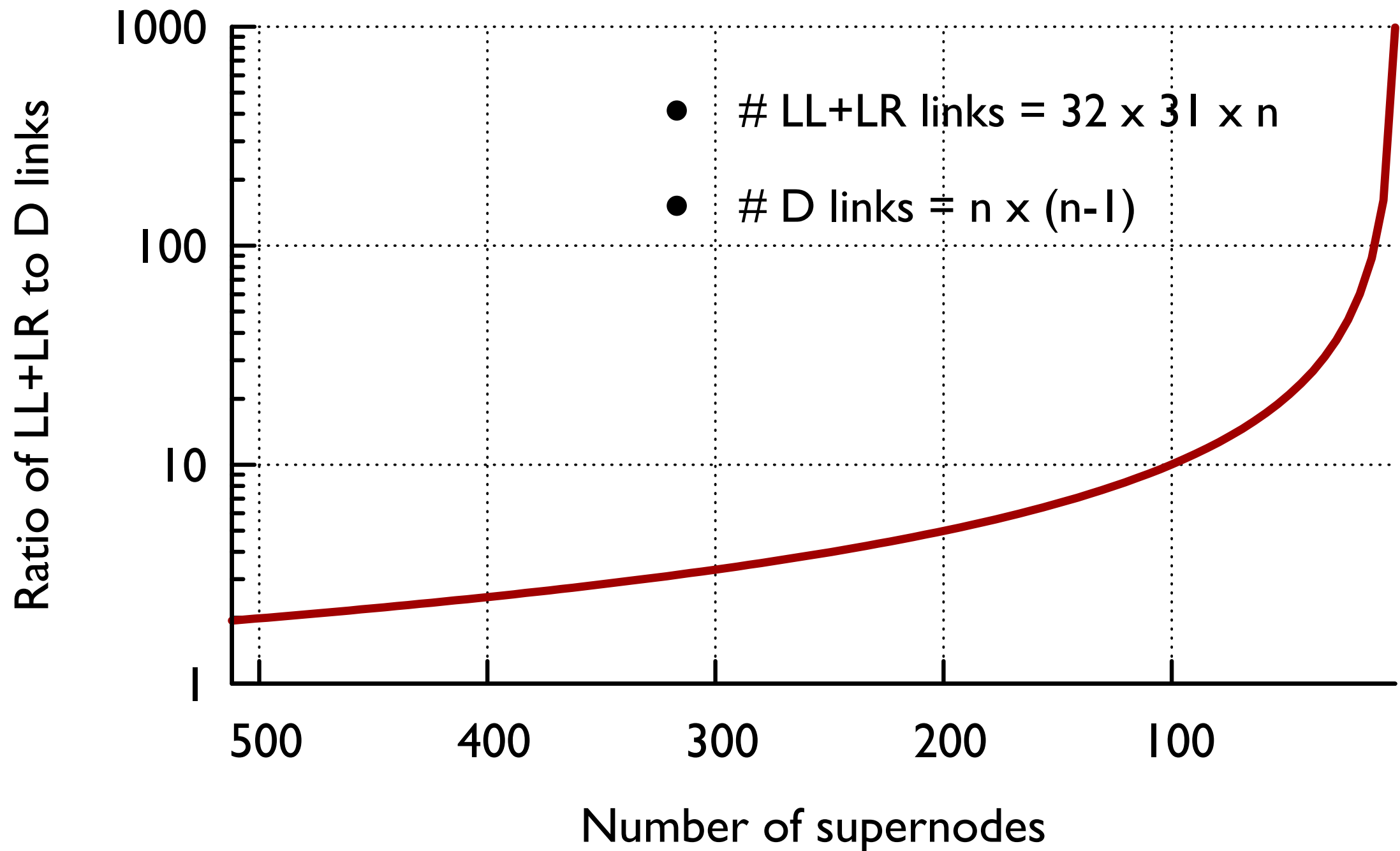


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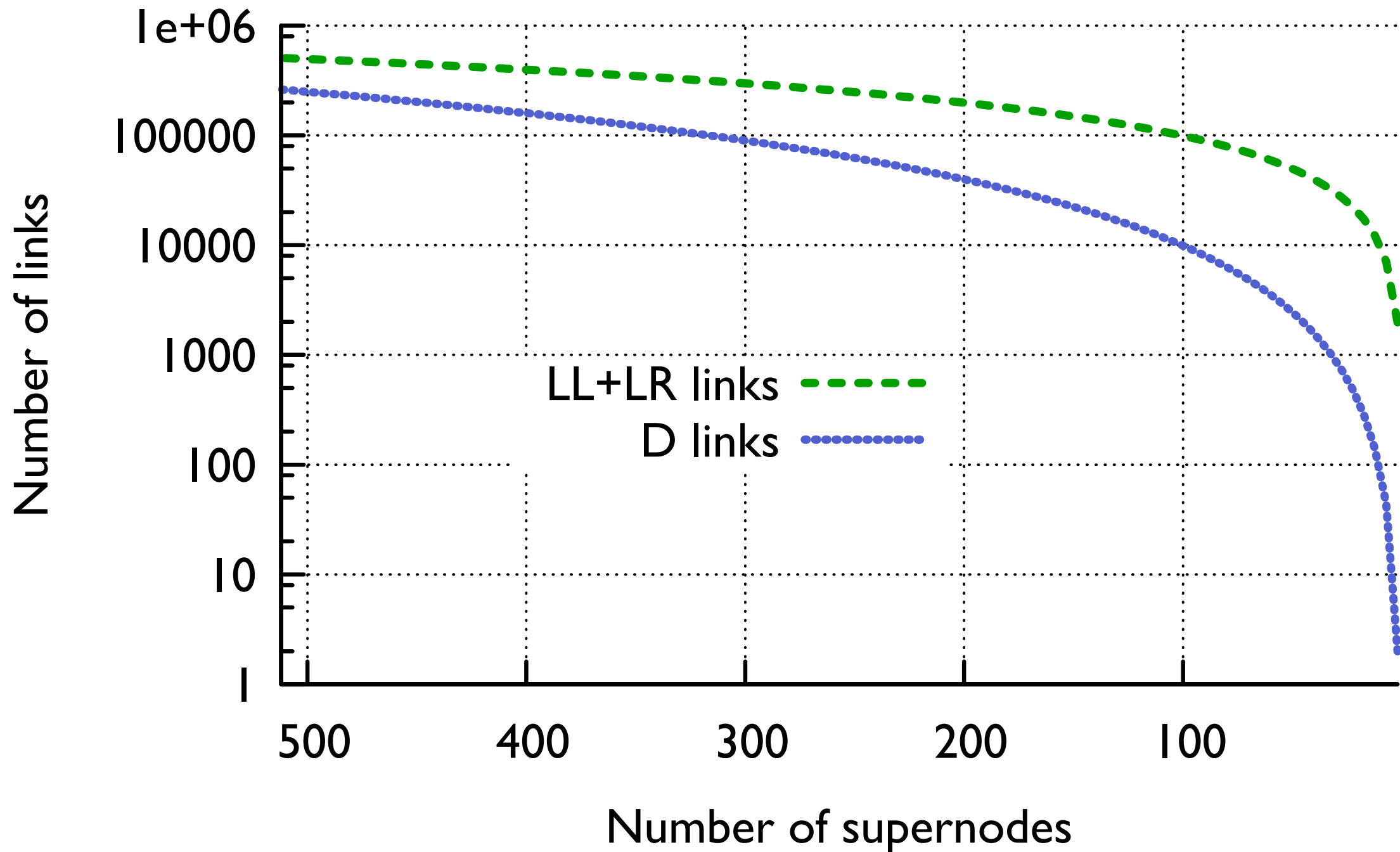




# The 'D' link bottleneck



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# Software stack/runtime choices

- Job scheduler:
  - Granularity of allocation: QCM (node), drawer, supernode
  - Contiguous allocation, random allocation or careful topology-aware allocation
- Routing:
  - Direct versus random indirect
- Mapping
  - Is it important for optimal performance?

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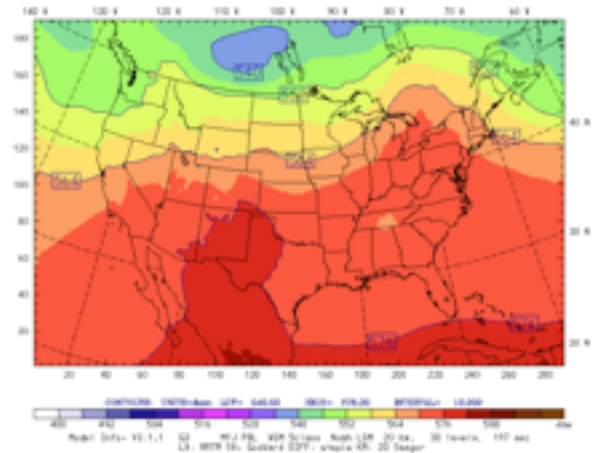
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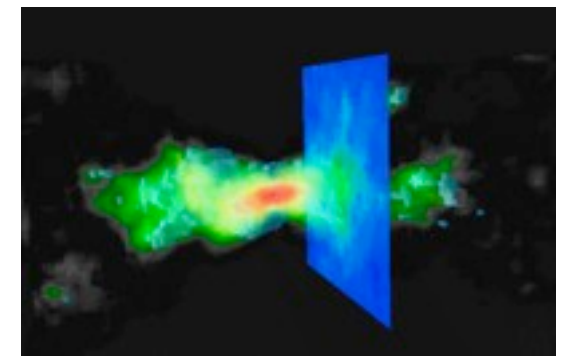
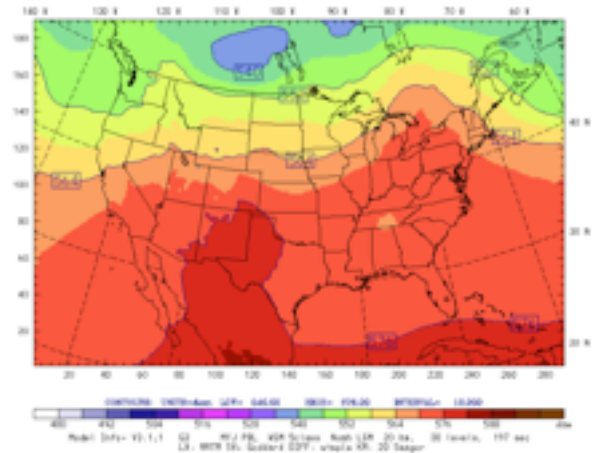
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WRF



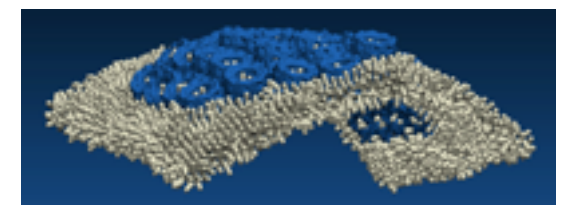
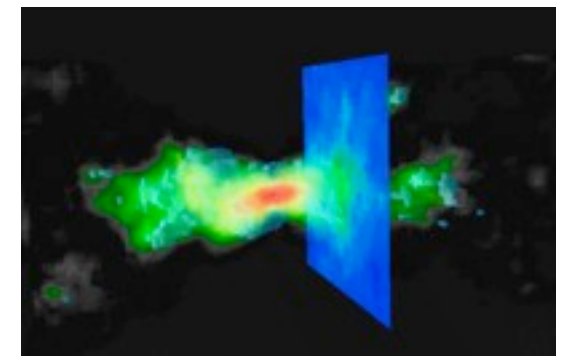
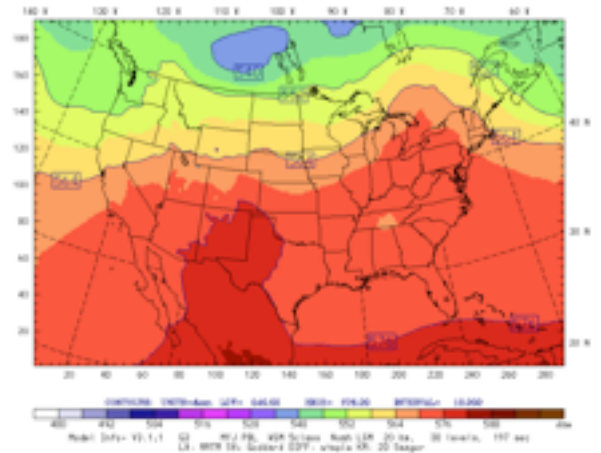
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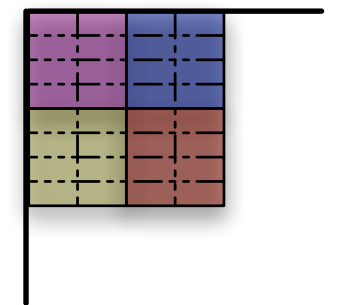
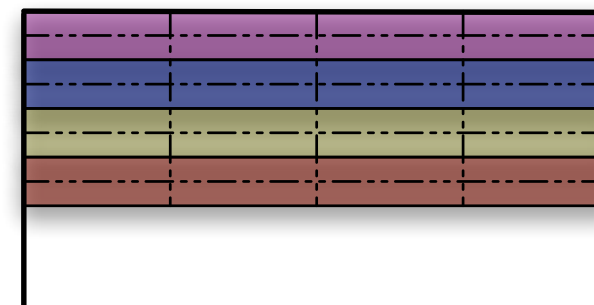
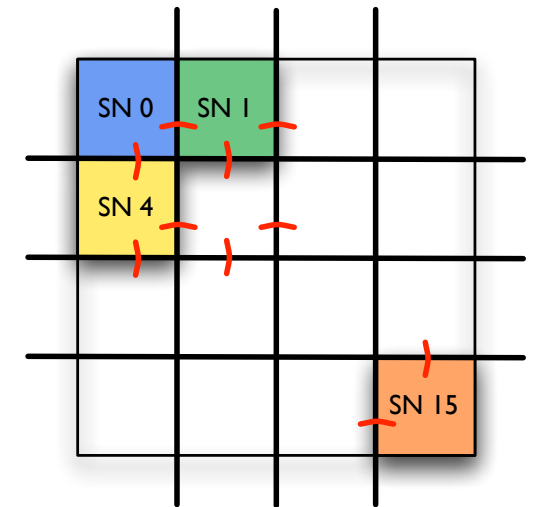
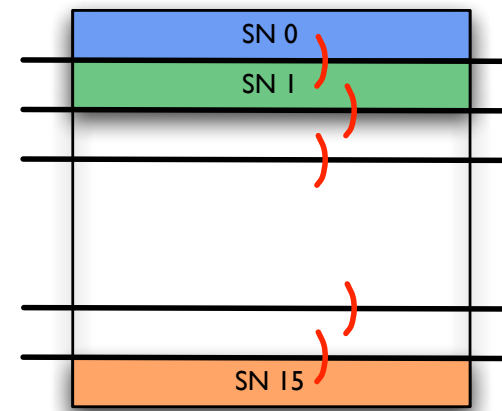


# Prediction Methodology

- Compute time prediction: run on a 3.8 GHz Power7 processor to get timings for sequential computation
- Emulation: obtain traces by running on 512-1360 cores of a 1.9 GHz Power5 cluster
- Simulations on one node of a SGI Altix 1000 shared memory machine

# Mapping and Routing

- Default mapping: MPI rank-ordered mapping
- Blocking: at the level of nodes, then drawers and supernodes
- Random mapping on nodes
- Routing choices:
  - Indirect routing w/ default mapping
  - Indirect routing w/ random drawers mapping



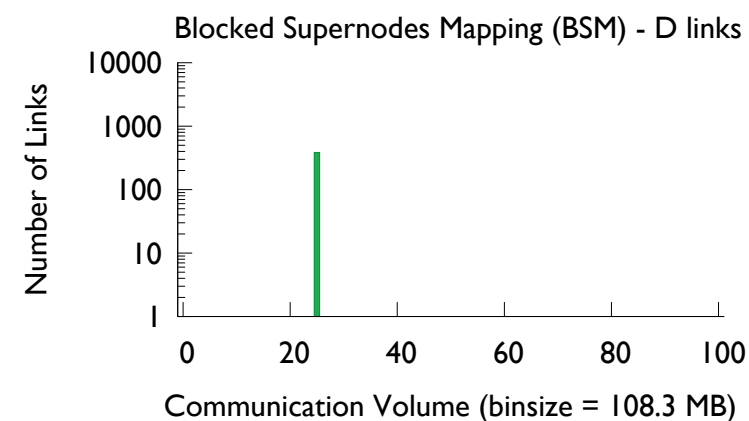
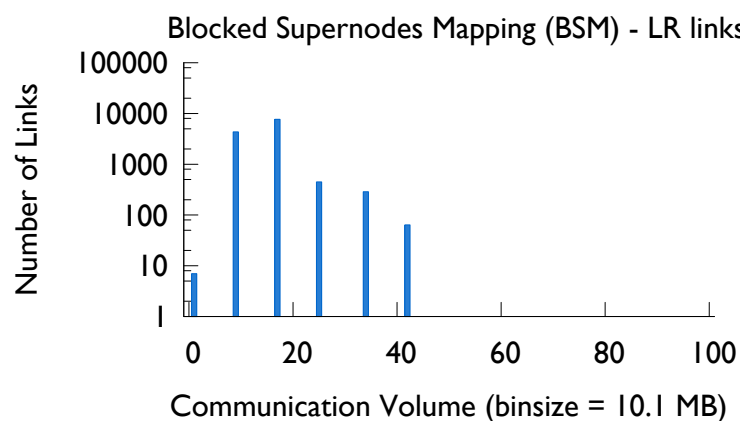
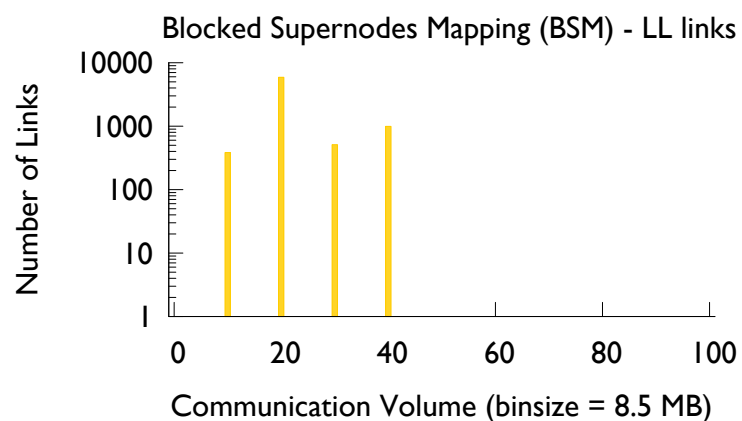
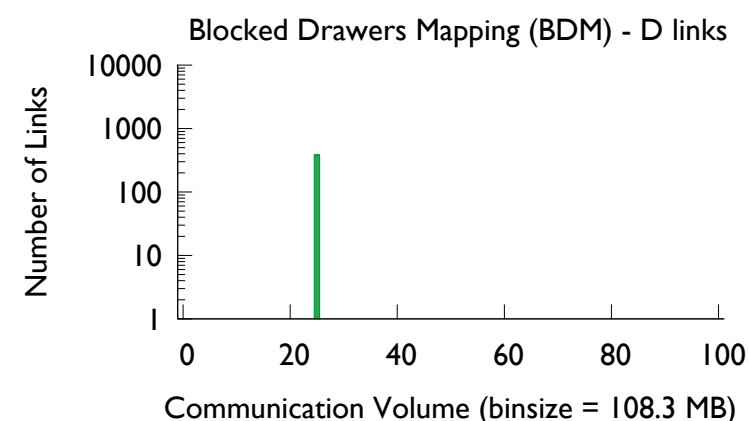
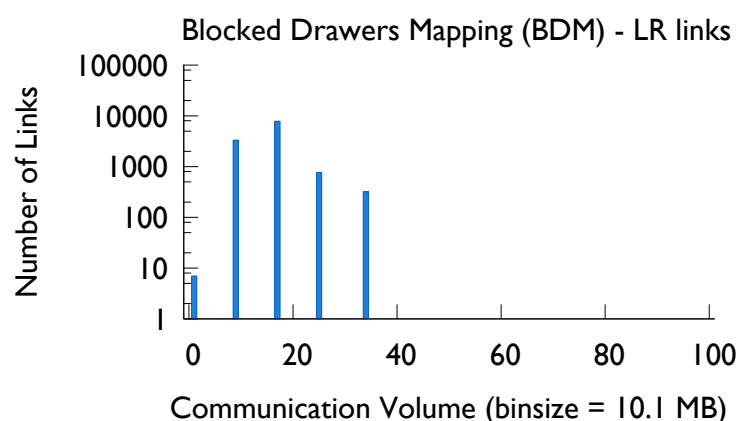
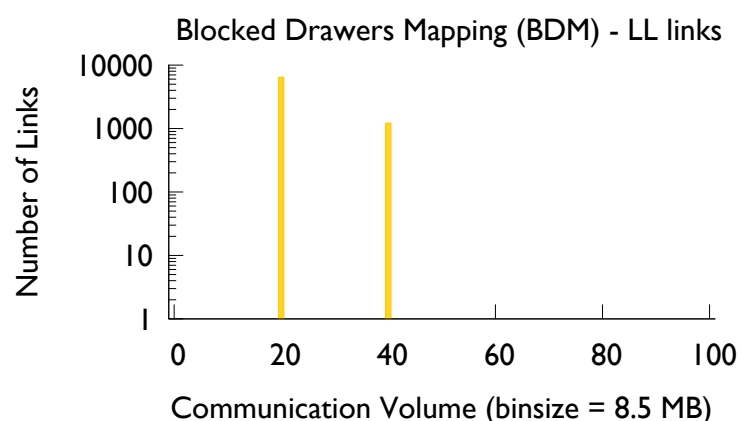
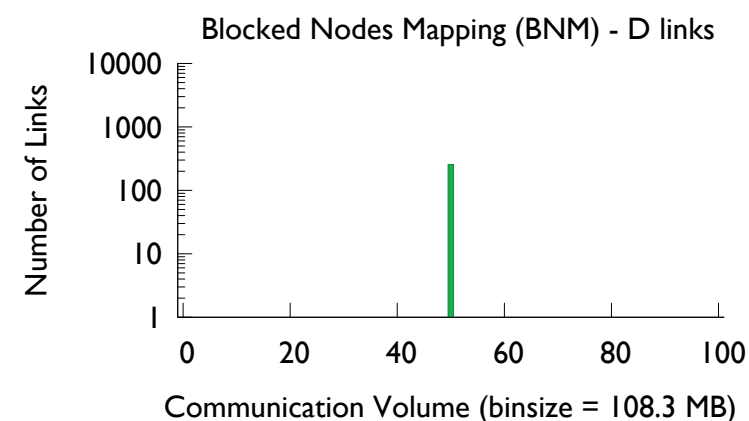
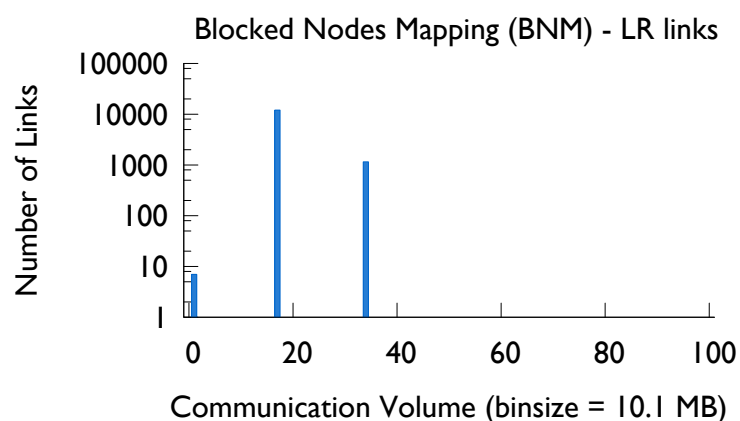
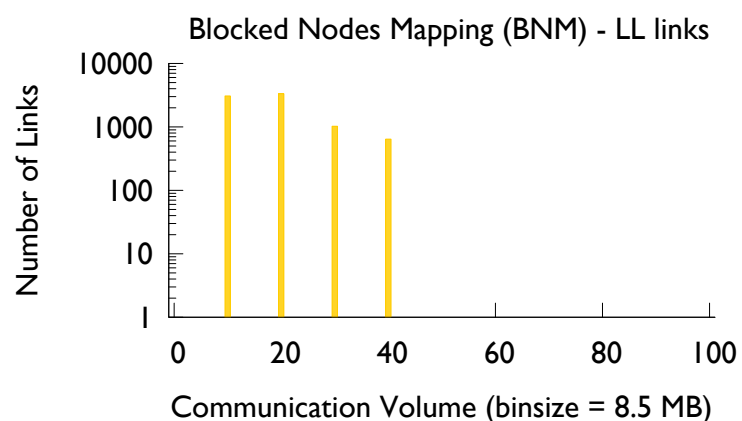
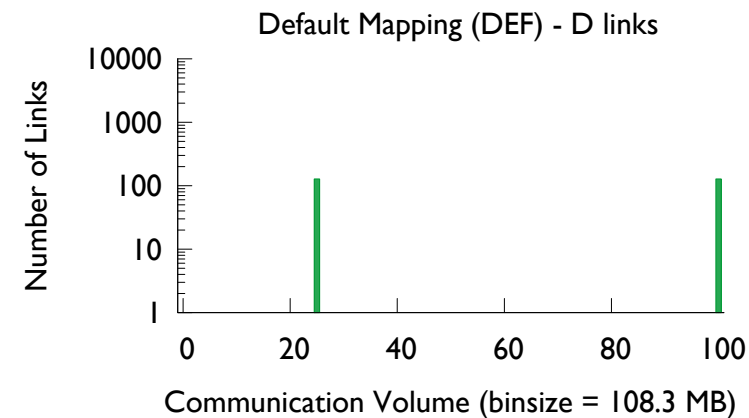
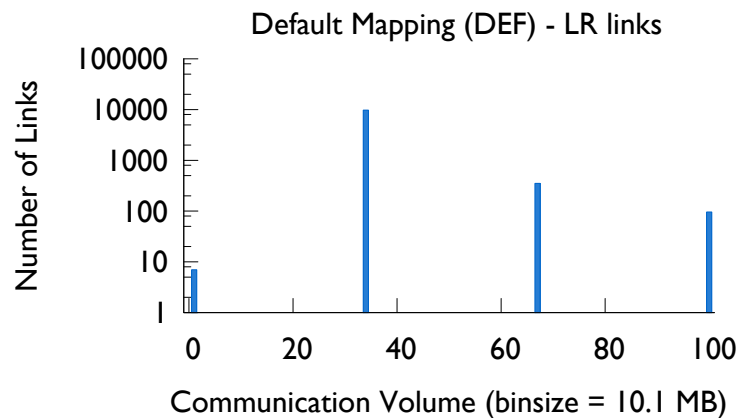
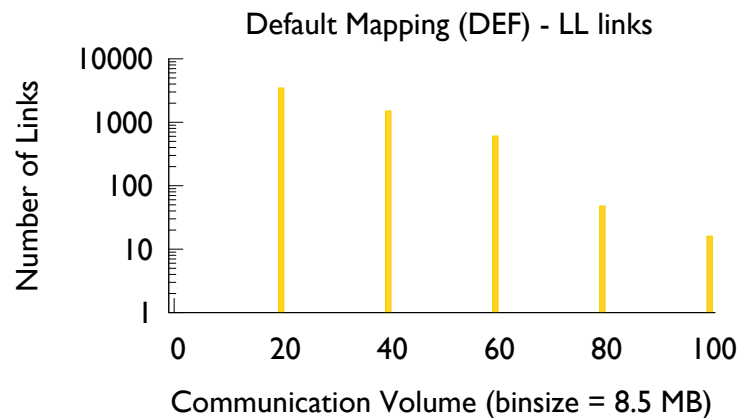
# 4-dimensional stencil

- Representative of MILC, a Lattice QCD code
- Each MPI task has  $64 \times 64 \times 64 \times 64$  elements
- Size of messages exchanged = 2 MB

# Experiments

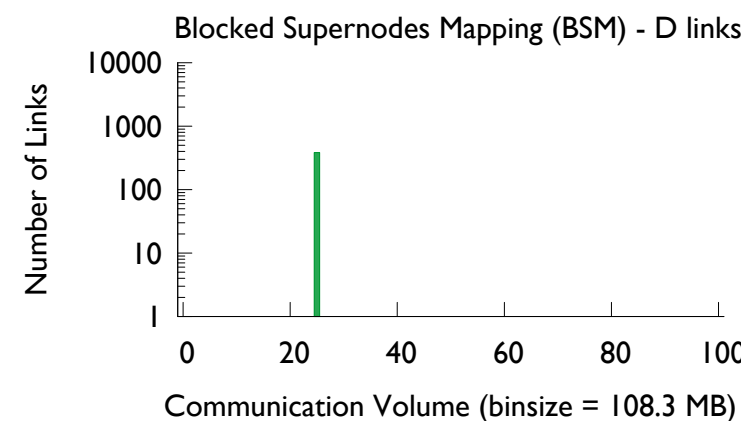
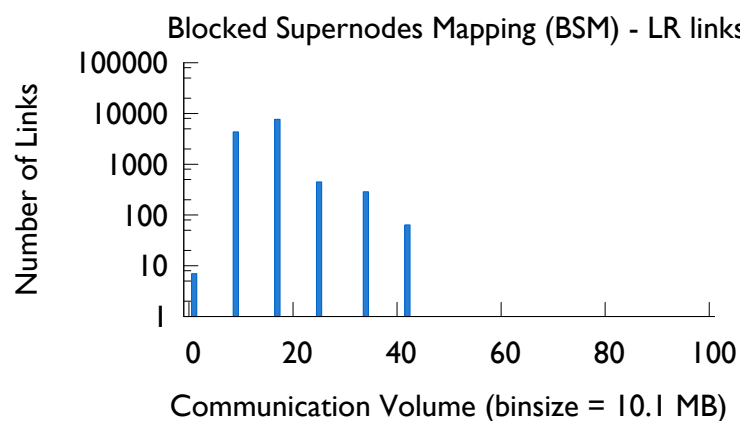
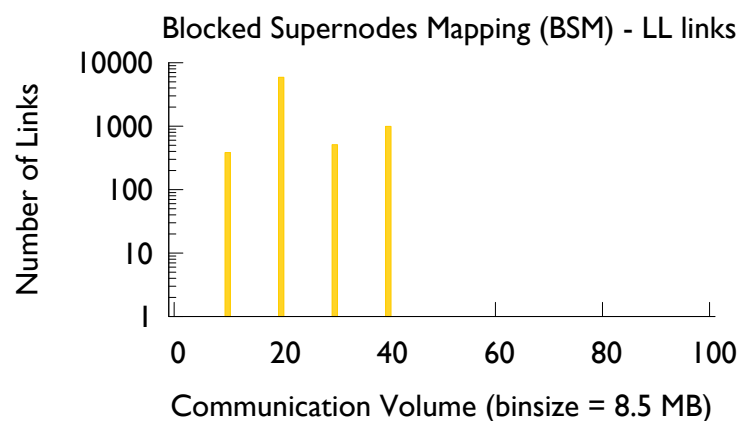
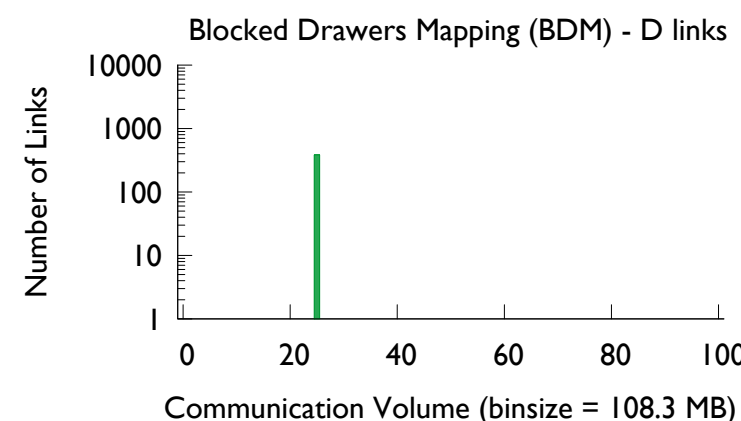
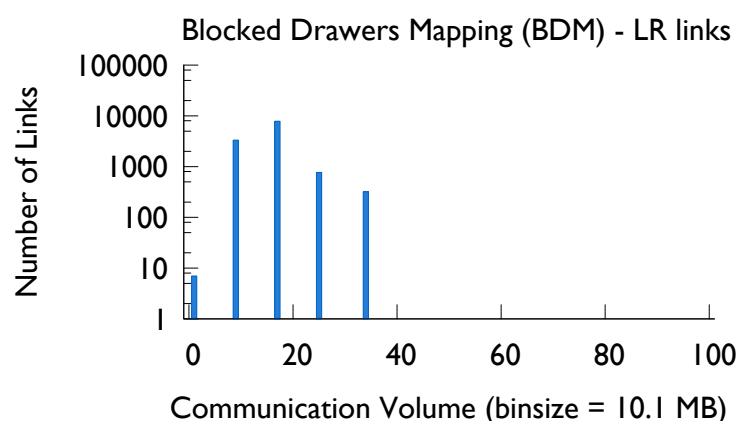
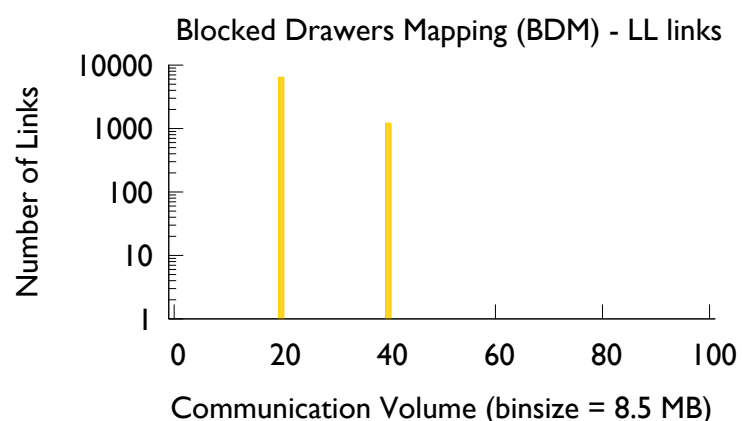
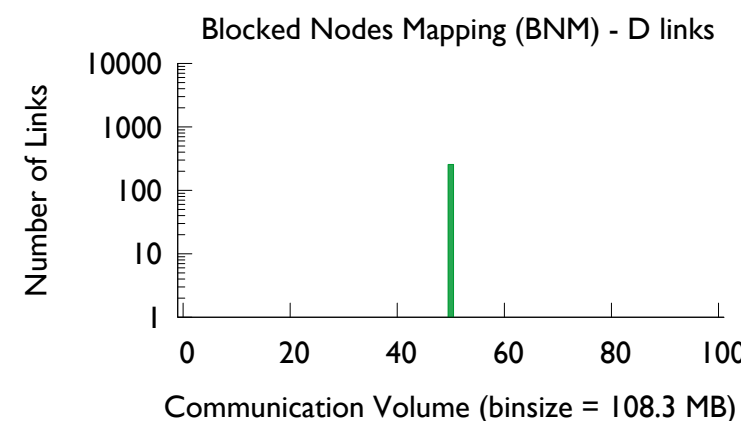
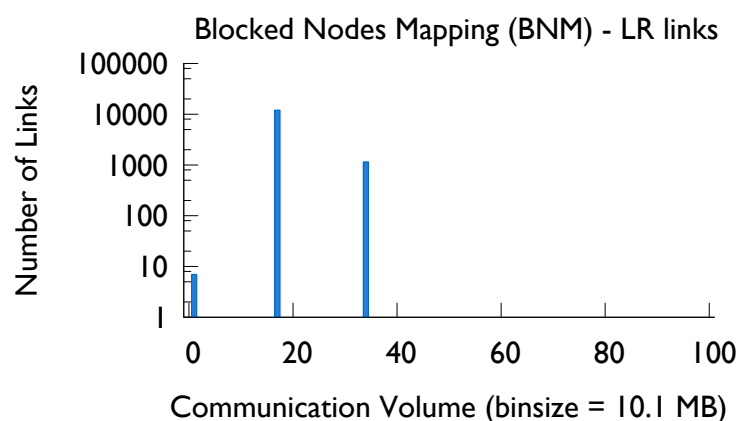
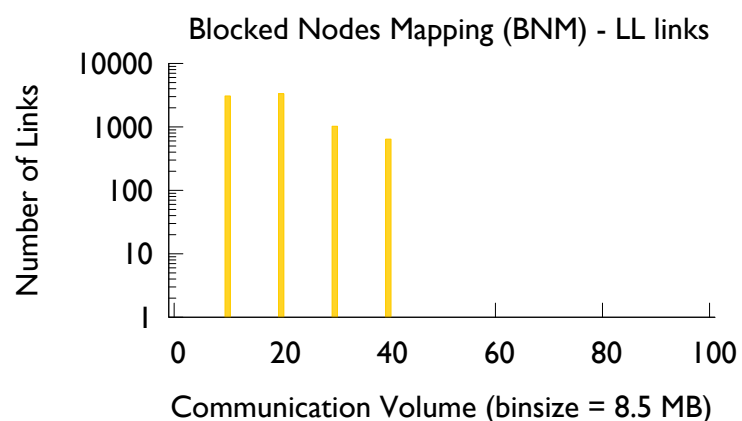
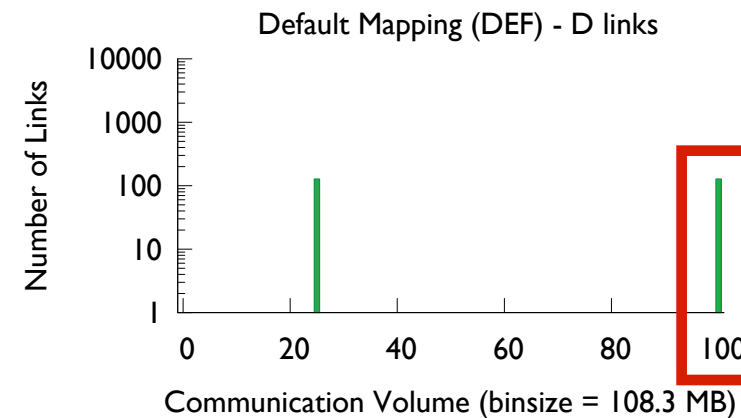
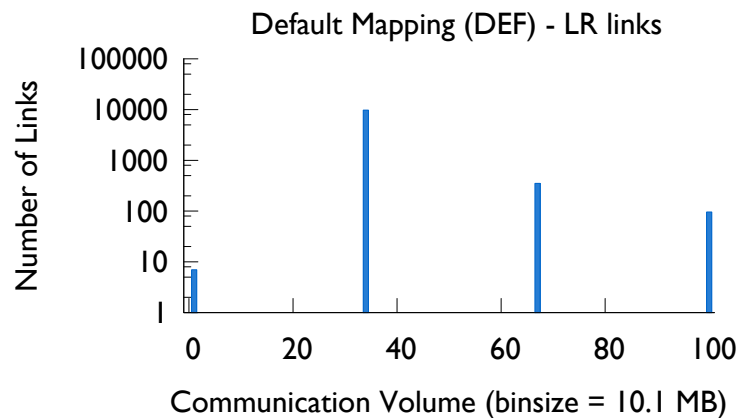
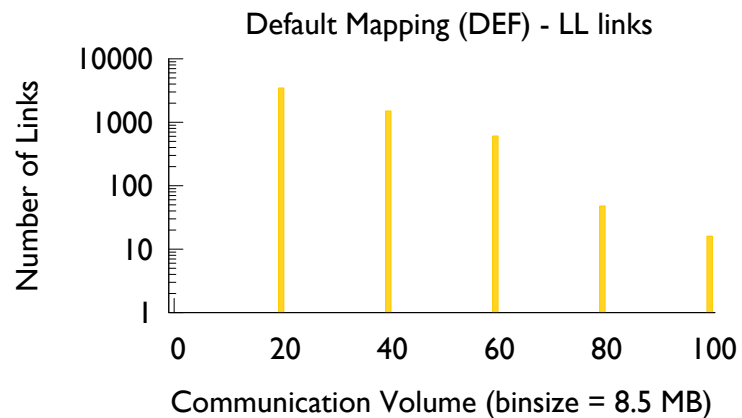
- Direct routing:
  - Default MPI rank-ordered mapping (DEF)
  - Blocking MPI tasks at the level of nodes (BNM)
  - Blocking at the level of drawers (BDM)
  - Blocking at the level of supernodes (BSM)
  - Random mapping at the level of nodes (RNM)
  - Random mapping at the level of drawers (RDM)
- Indirect routing
  - Default MPI rank-ordered mapping (DFI)
  - Random mapping at the level of drawers (RDI)

# 4D Stencil on 64 supernodes

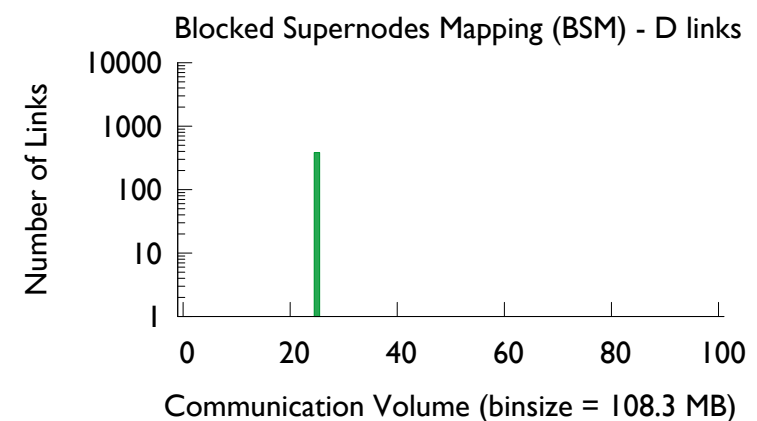
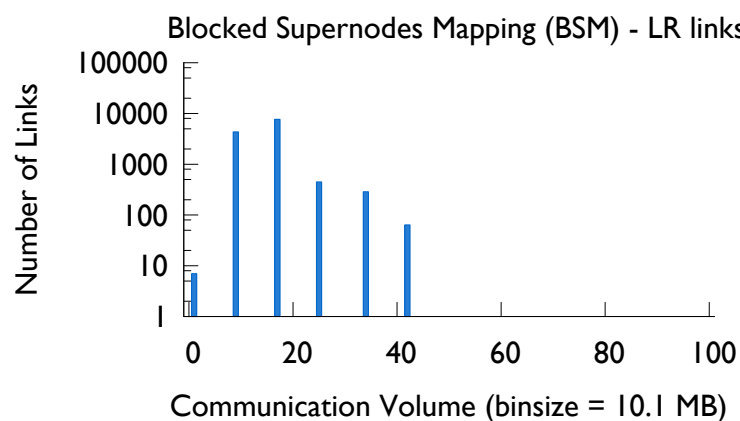
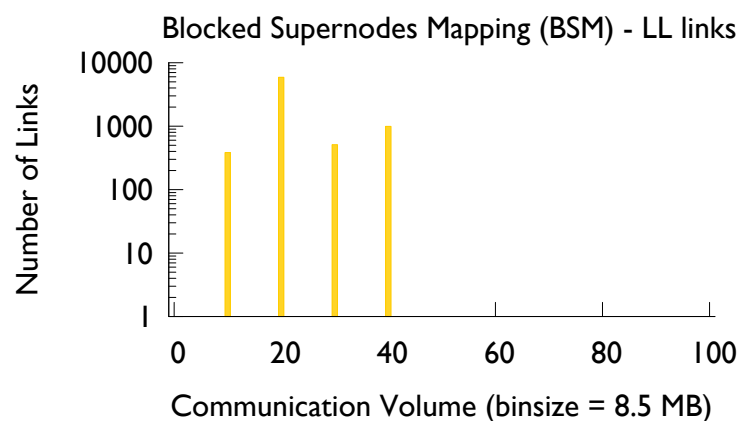
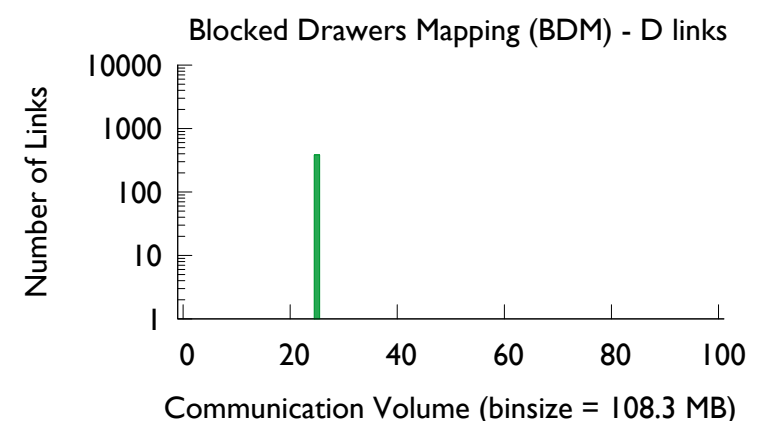
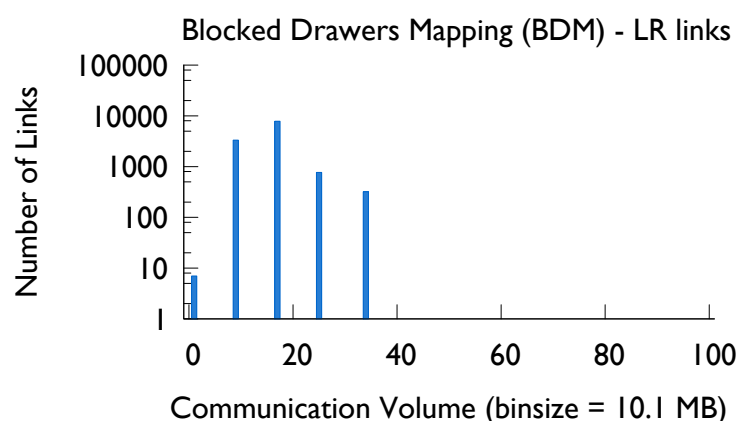
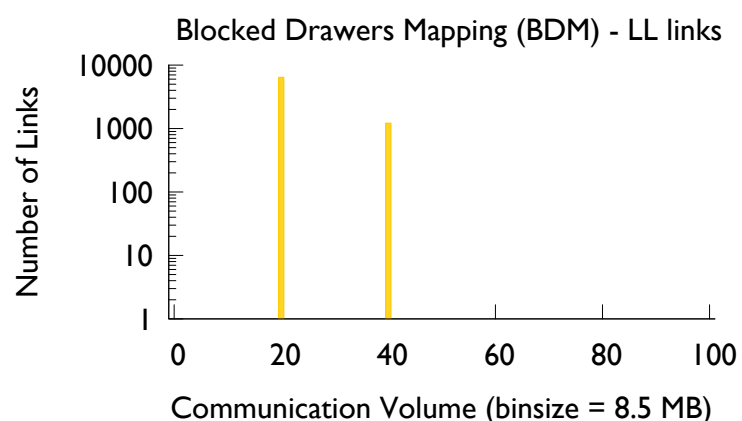
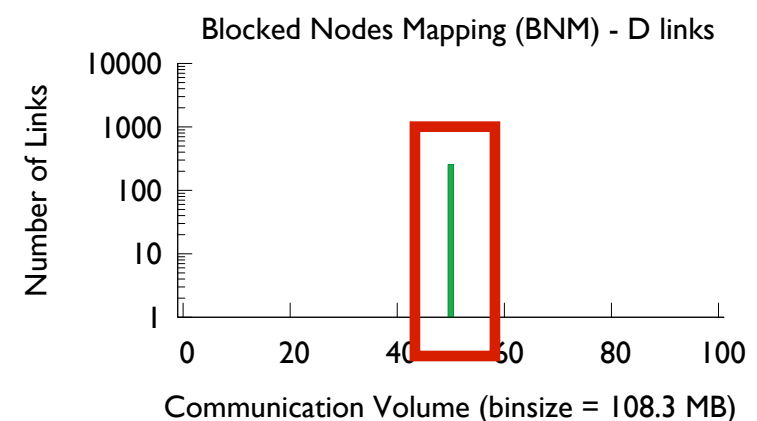
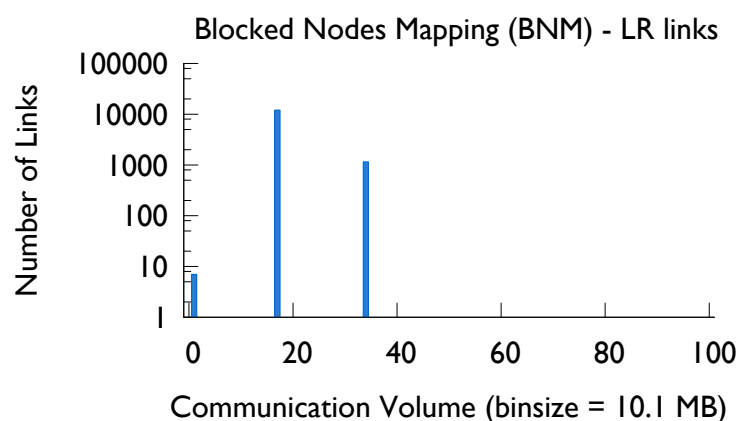
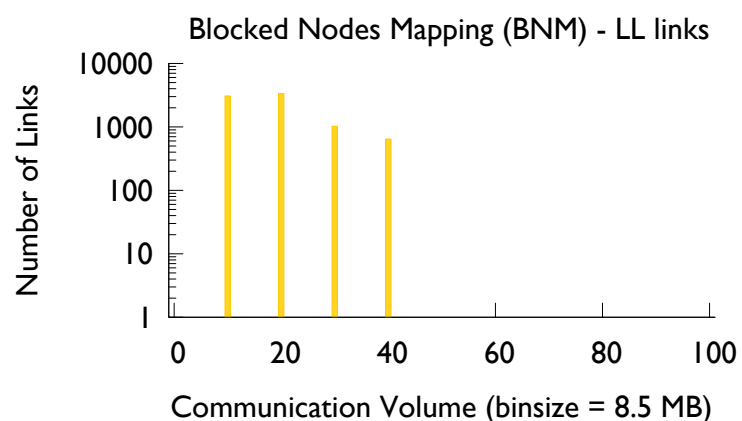
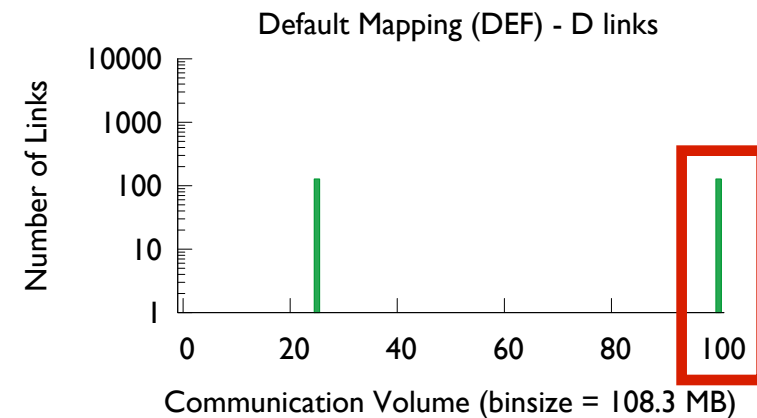
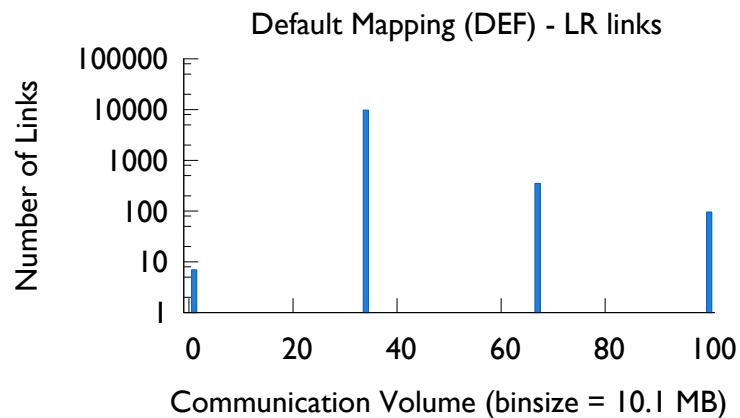
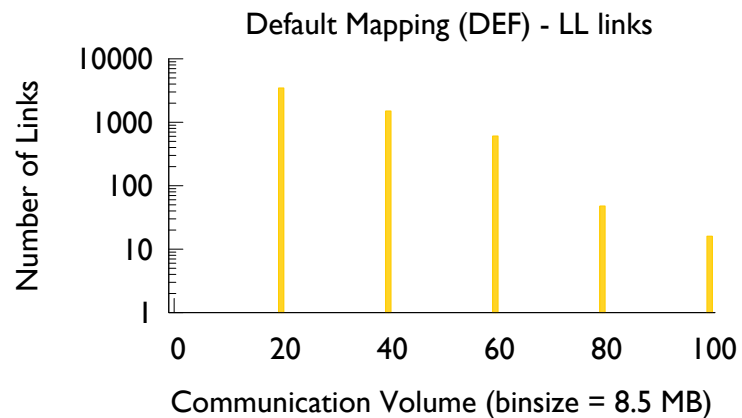




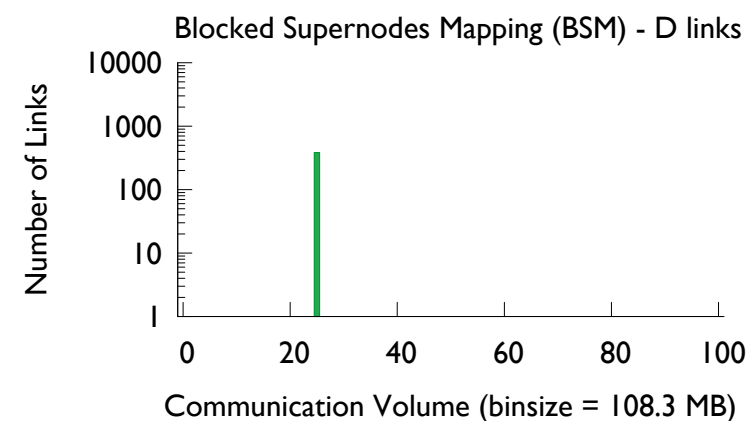
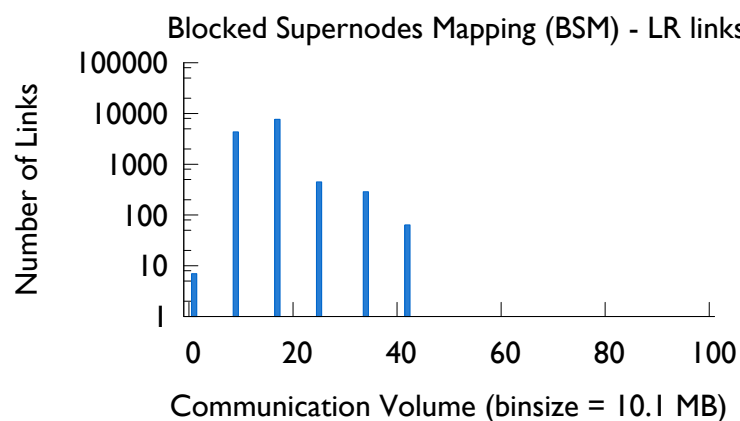
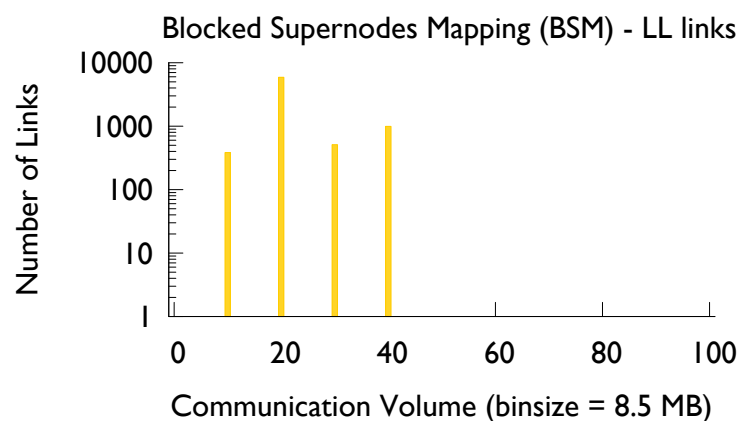
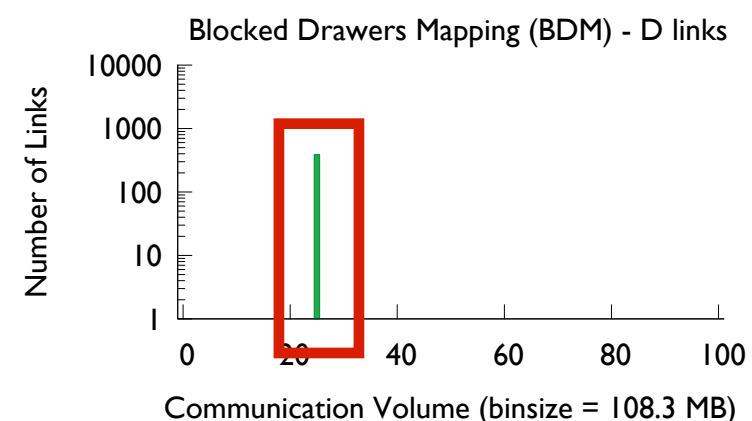
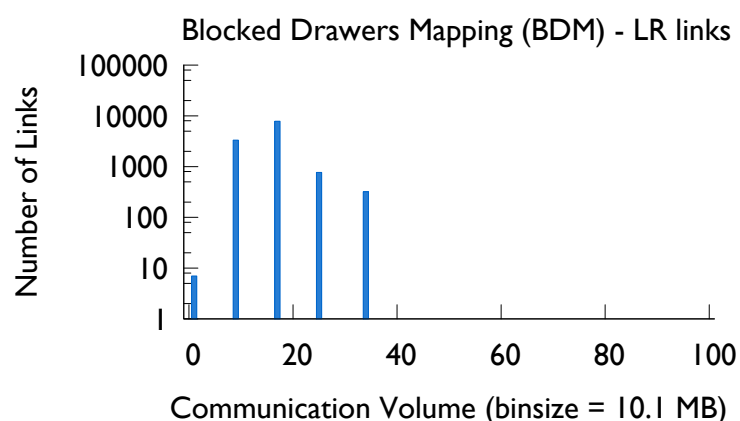
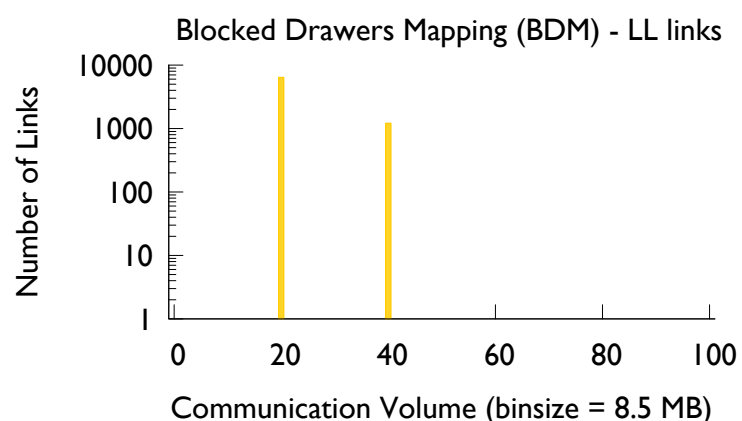
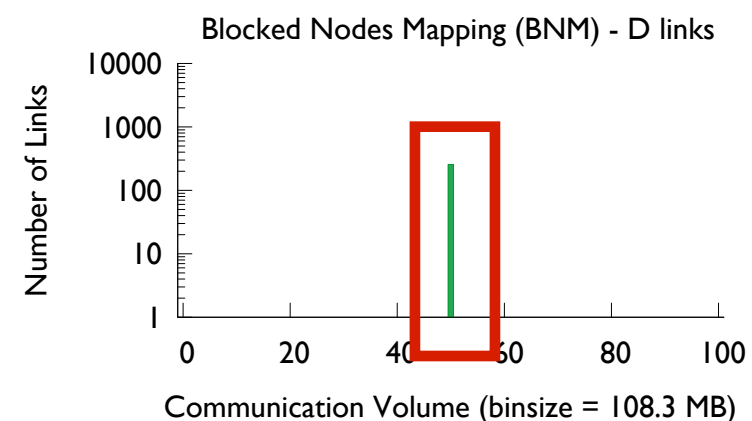
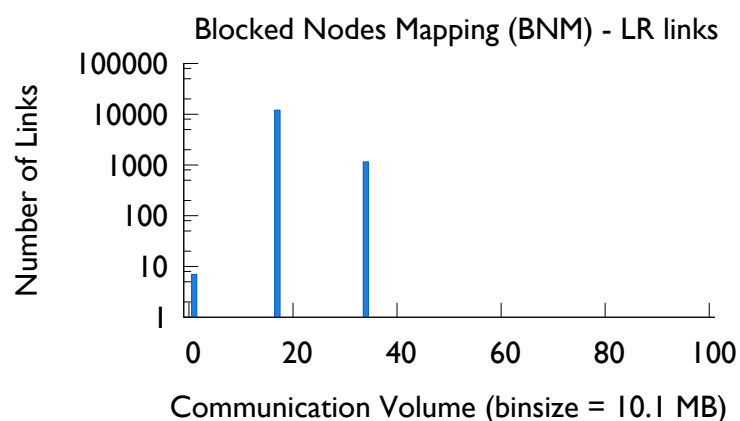
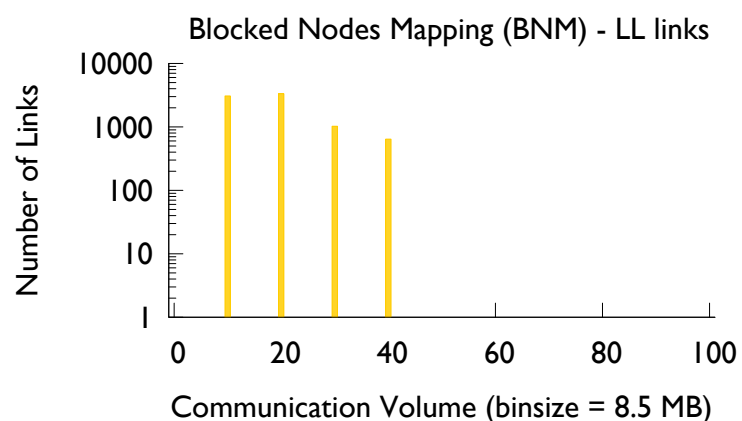
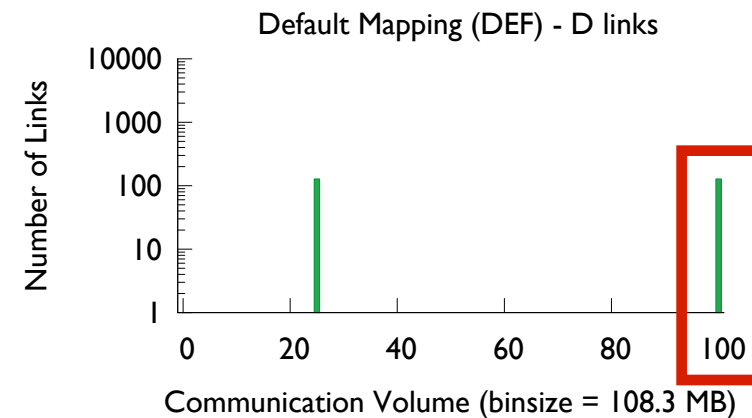
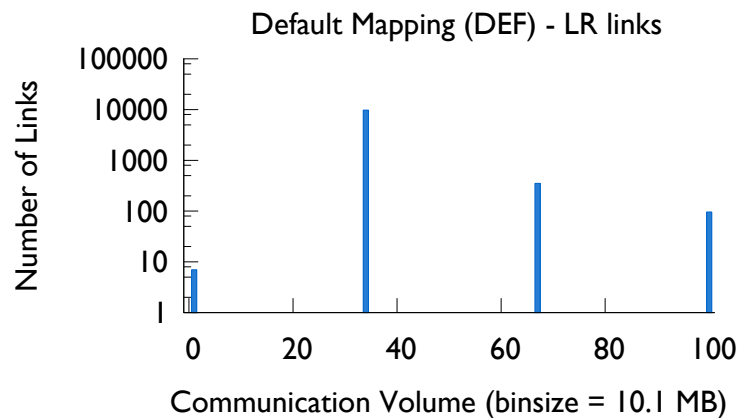
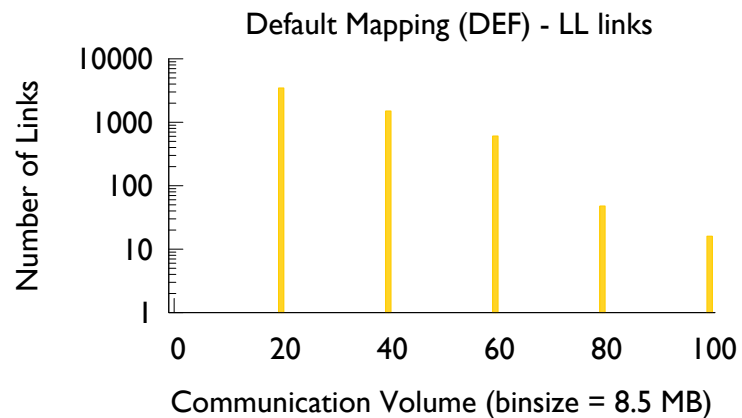
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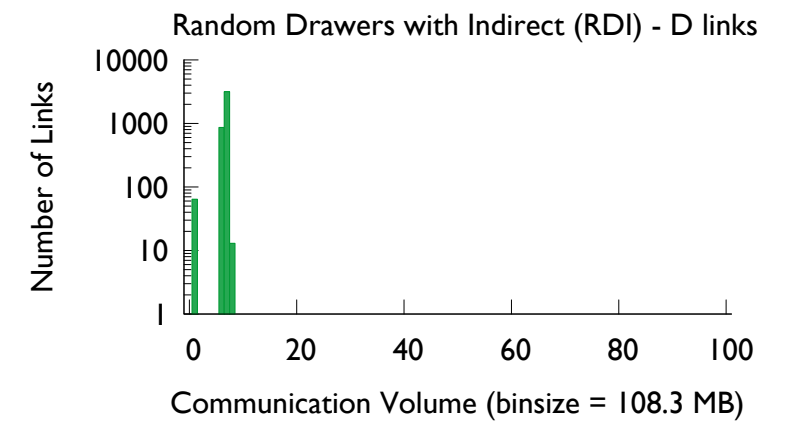
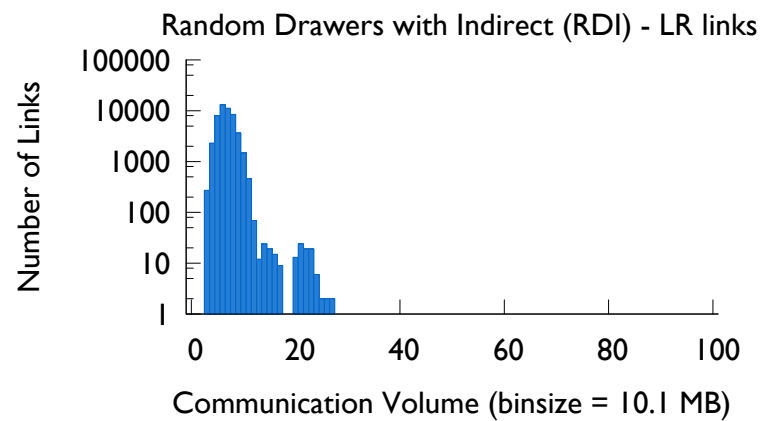
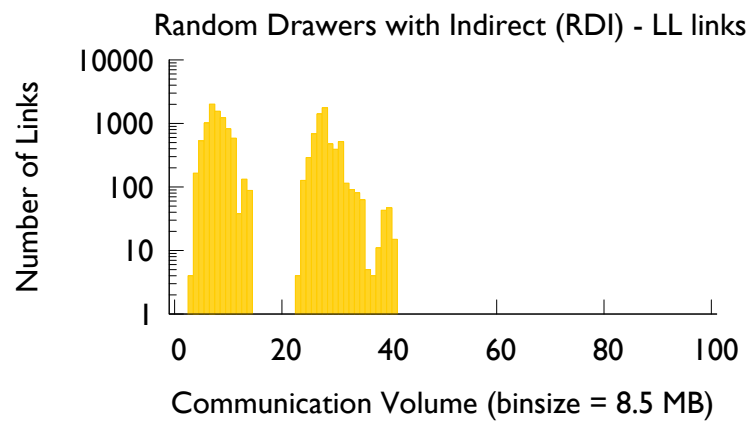
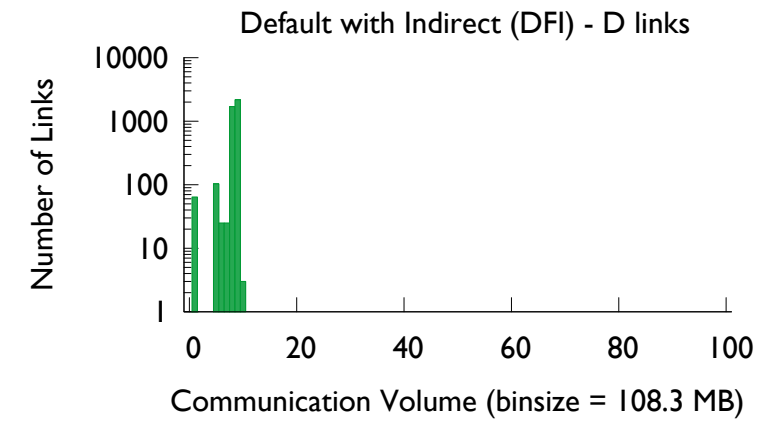
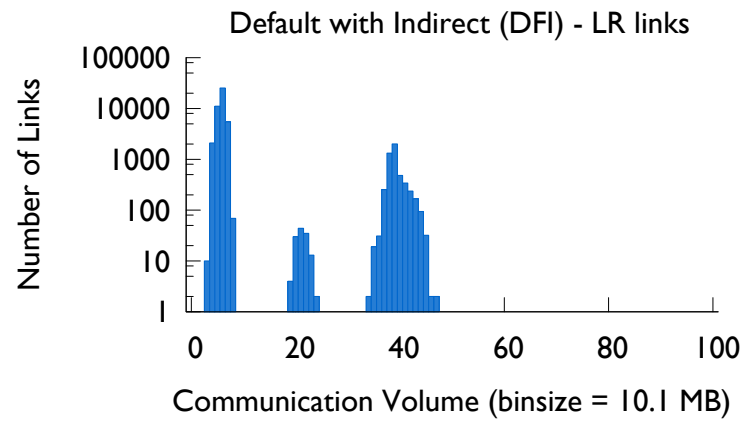
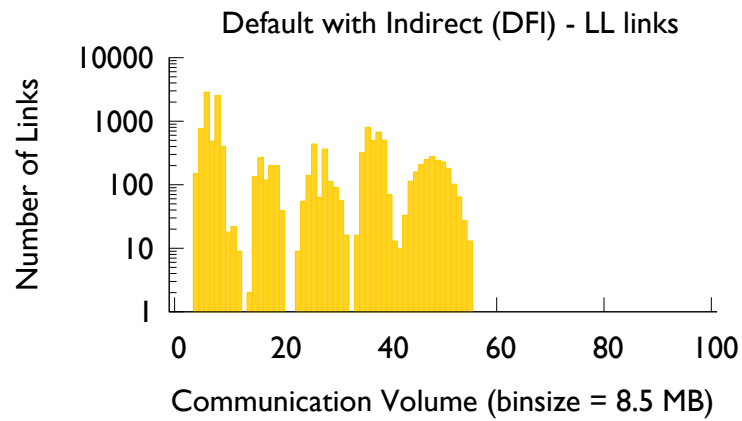
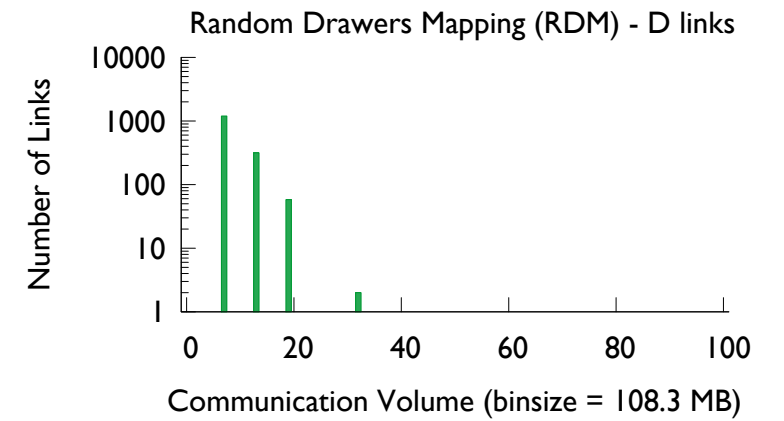
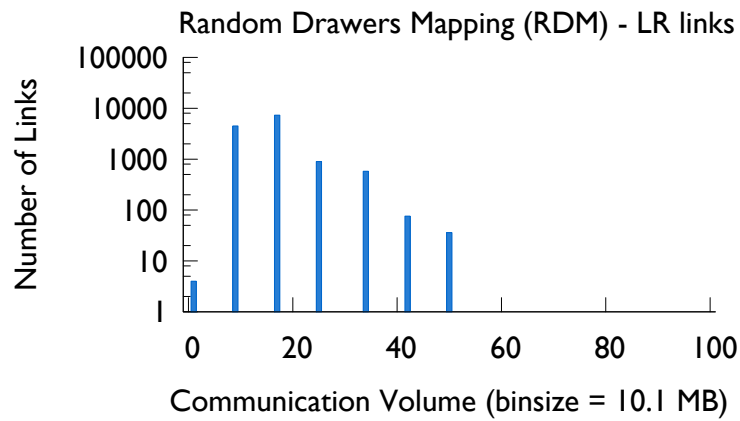
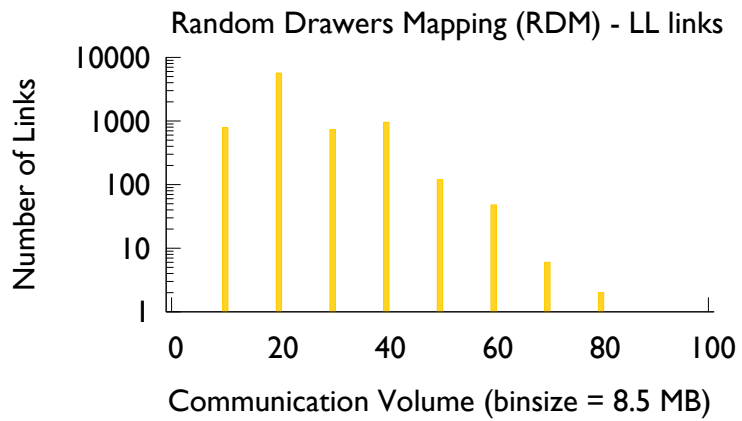
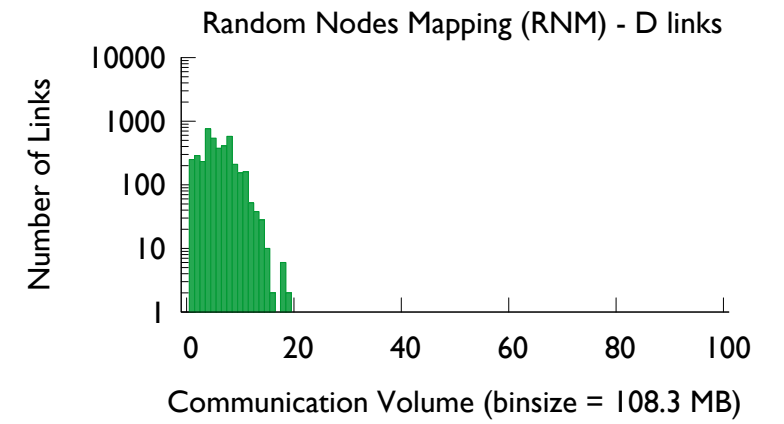
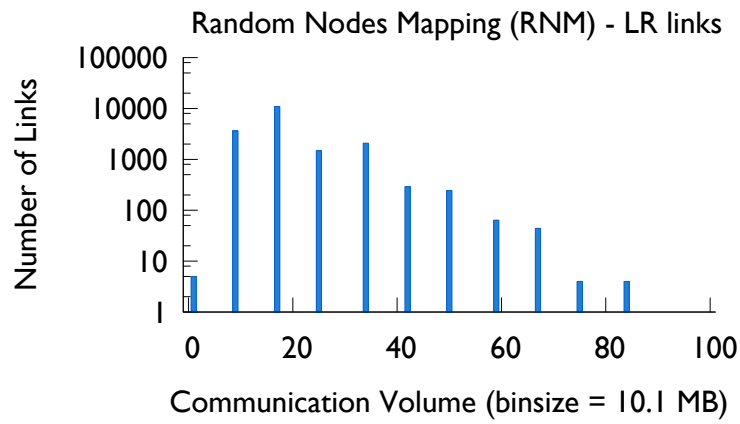
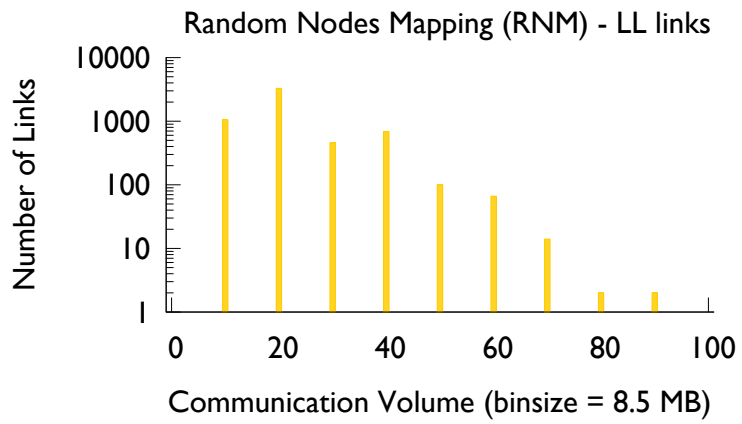
# 4D Stencil on 64 supernodes



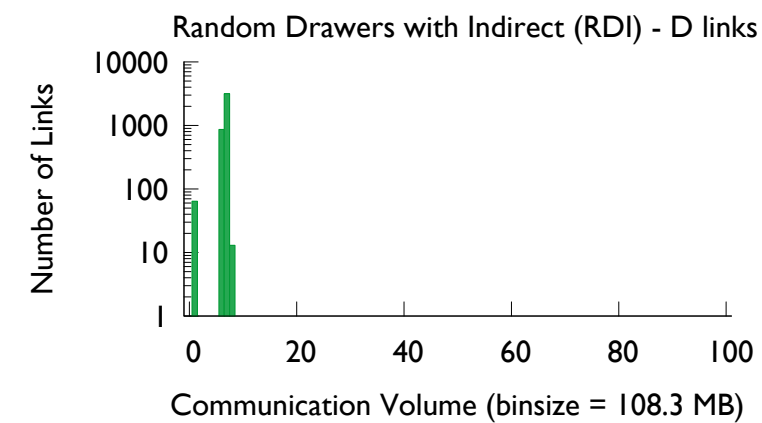
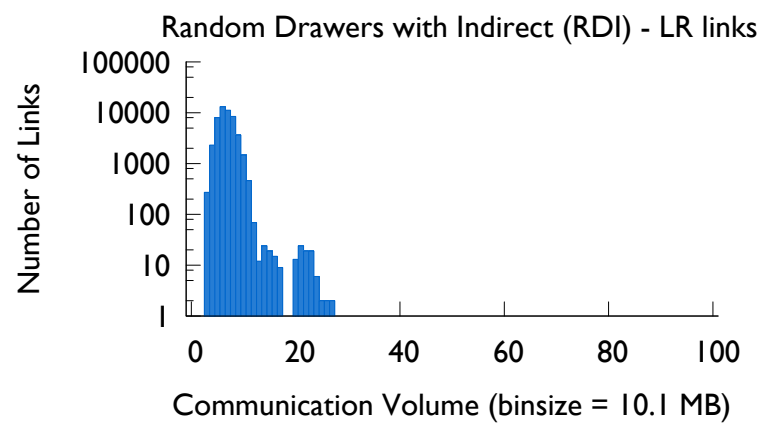
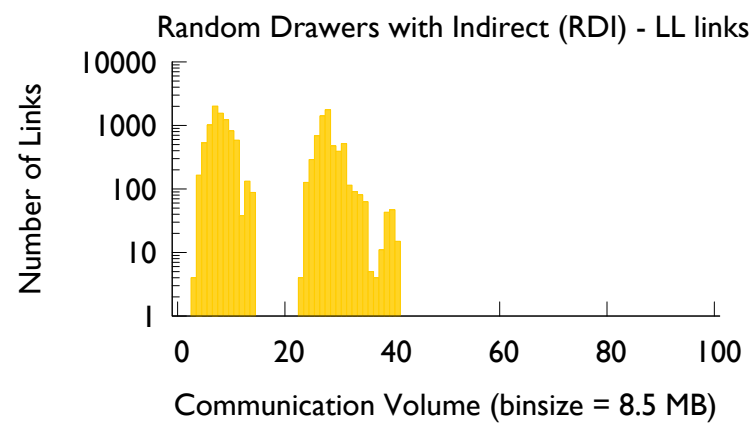
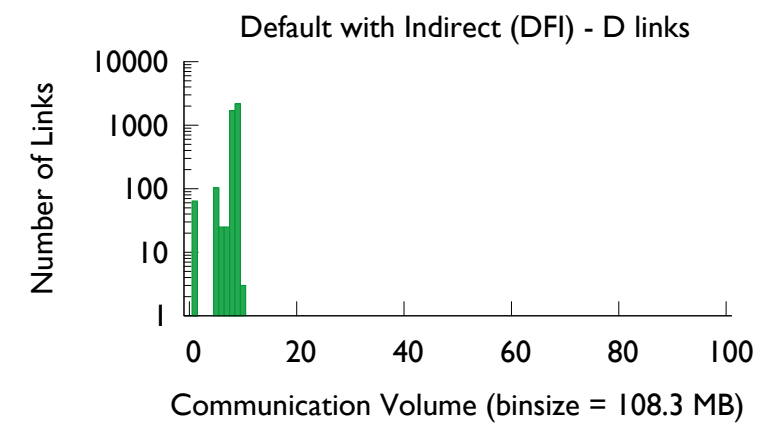
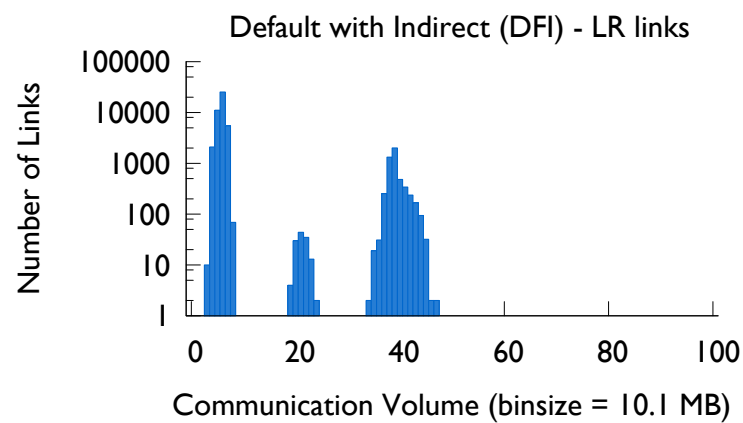
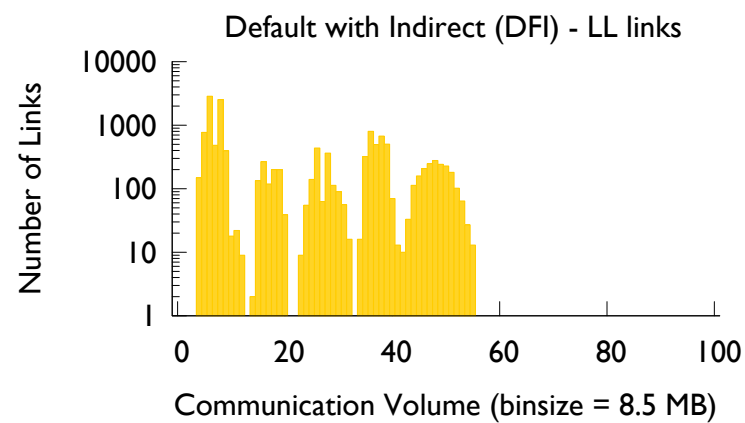
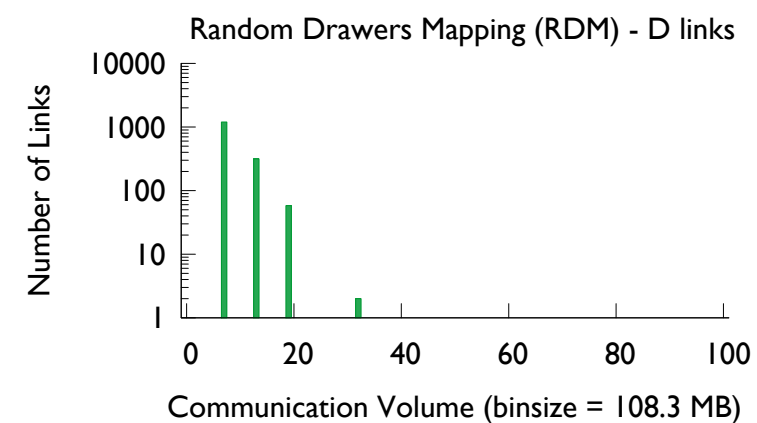
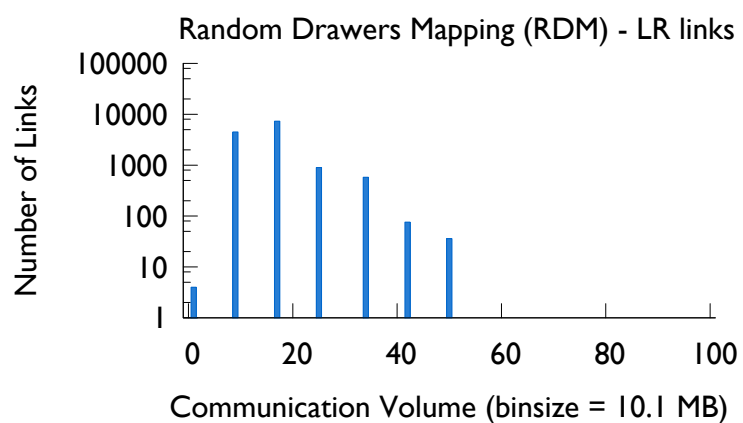
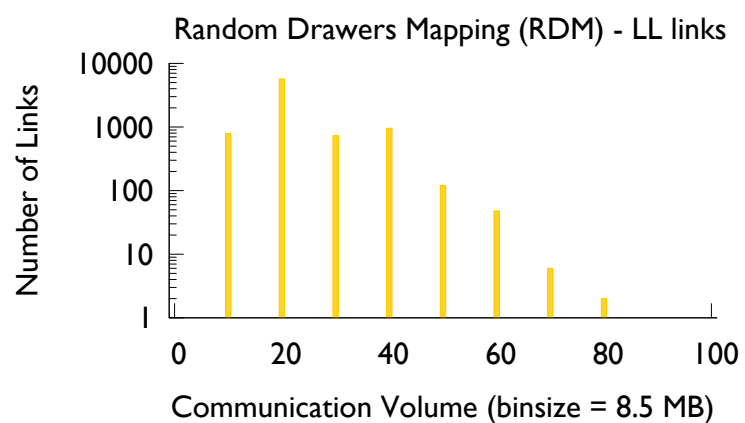
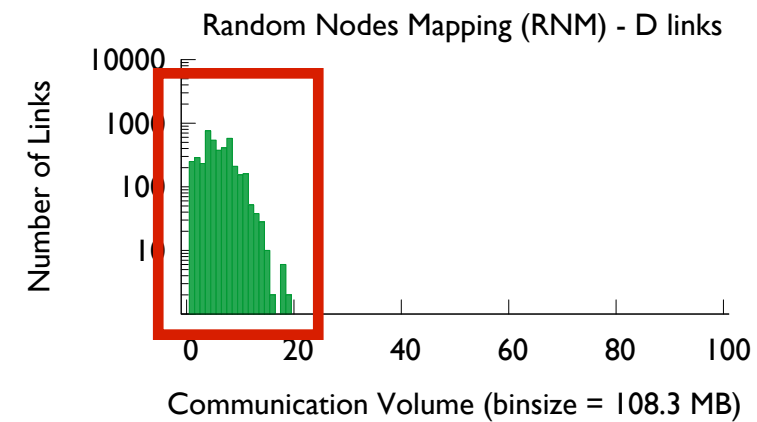
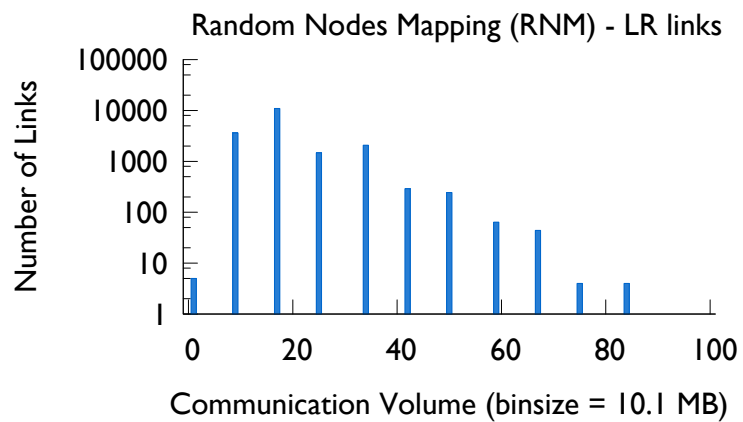
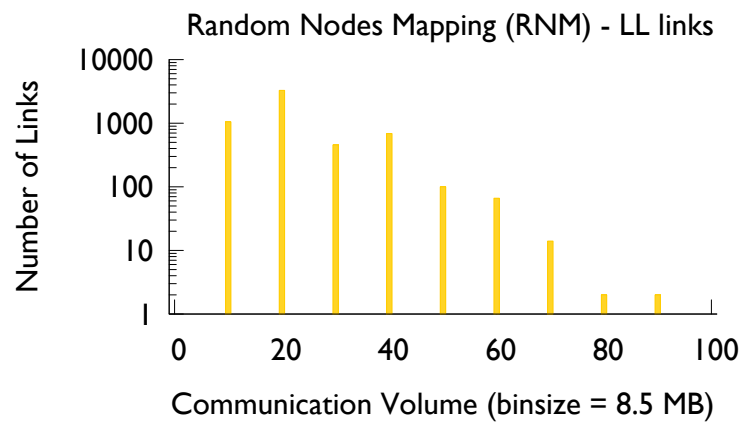
# 4D Stencil on 64 supernodes



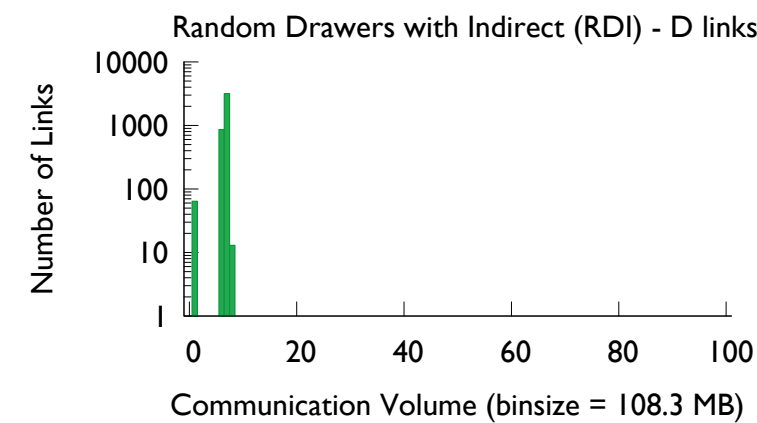
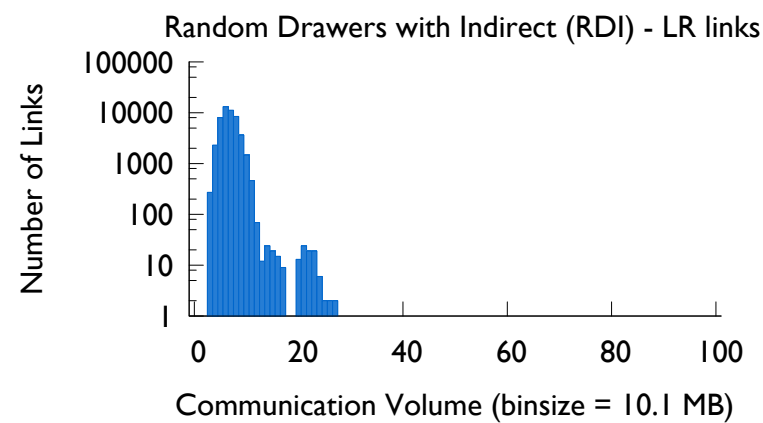
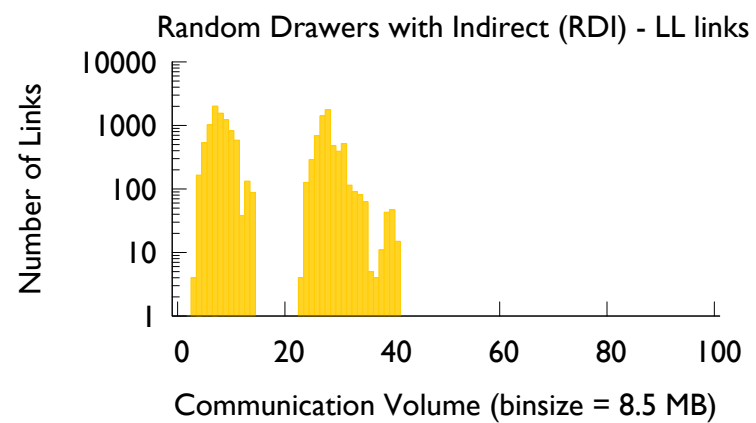
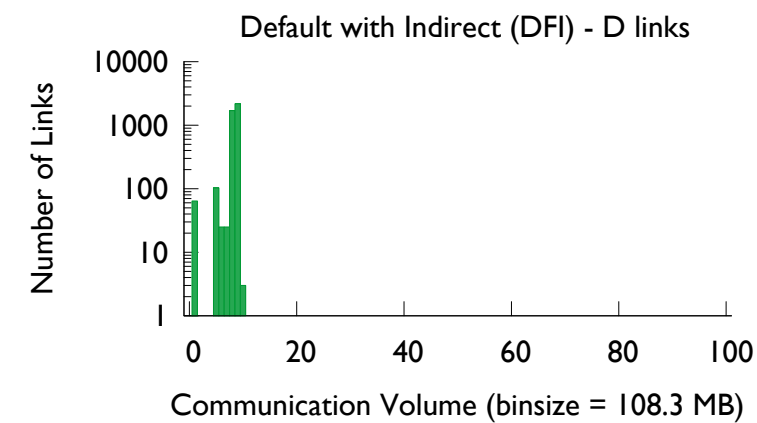
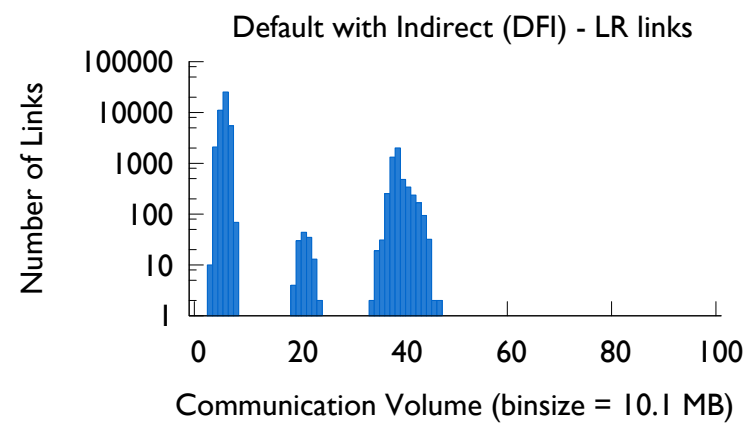
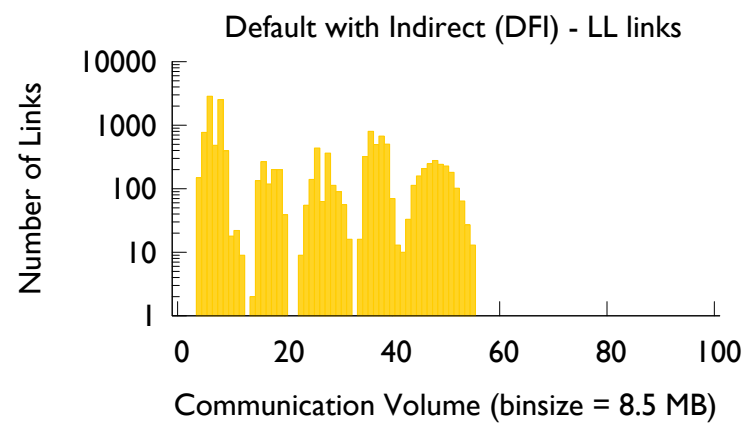
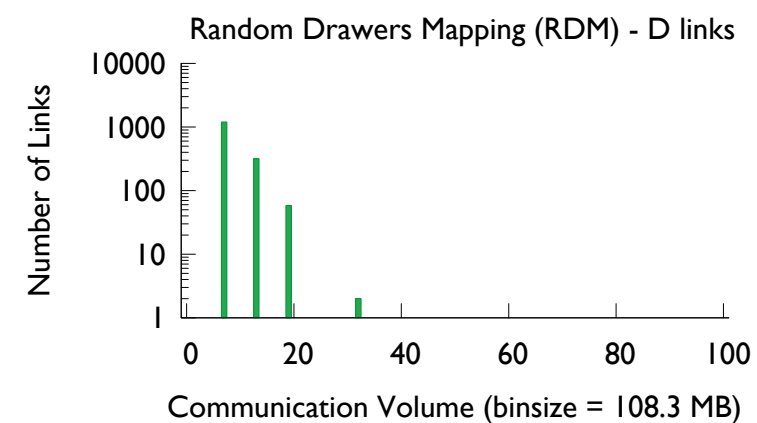
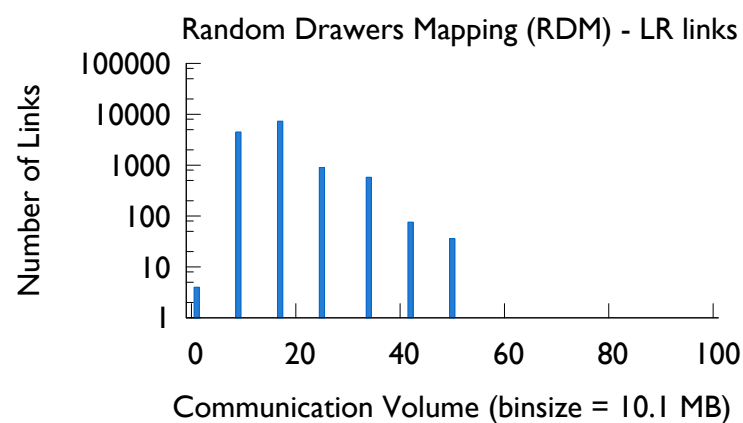
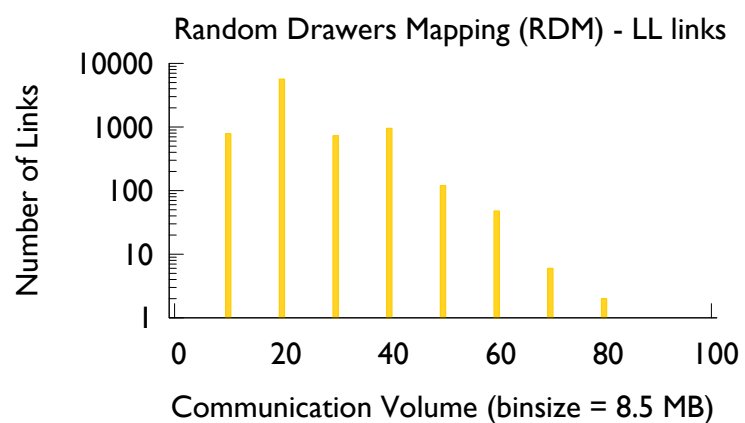
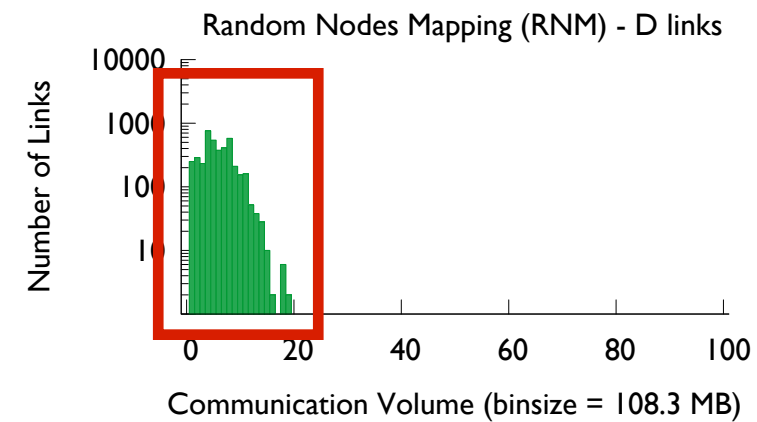
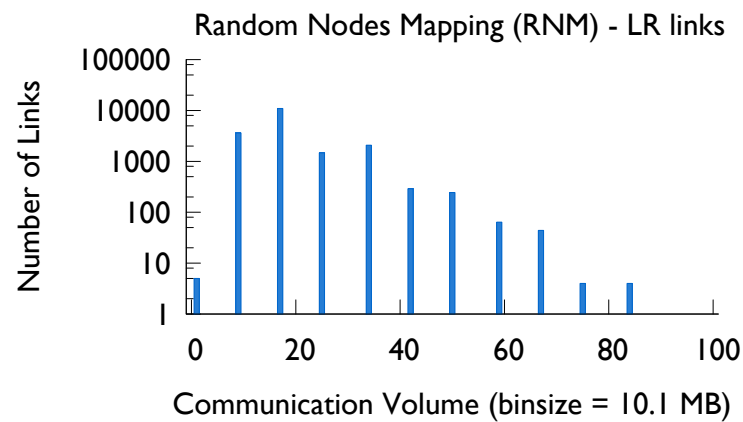
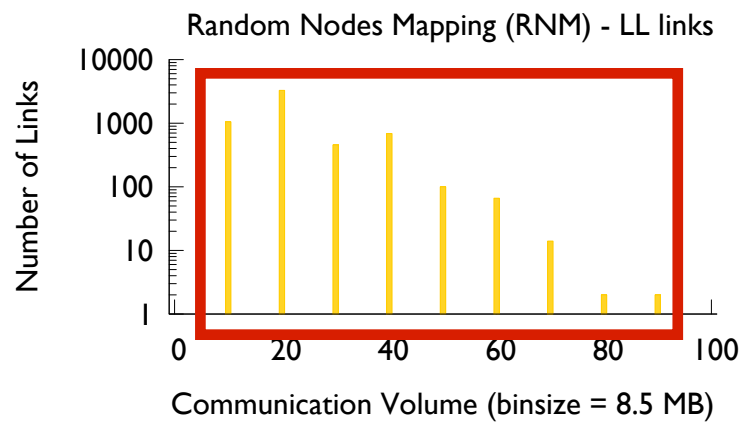
# 4D Stencil on 64 supernodes



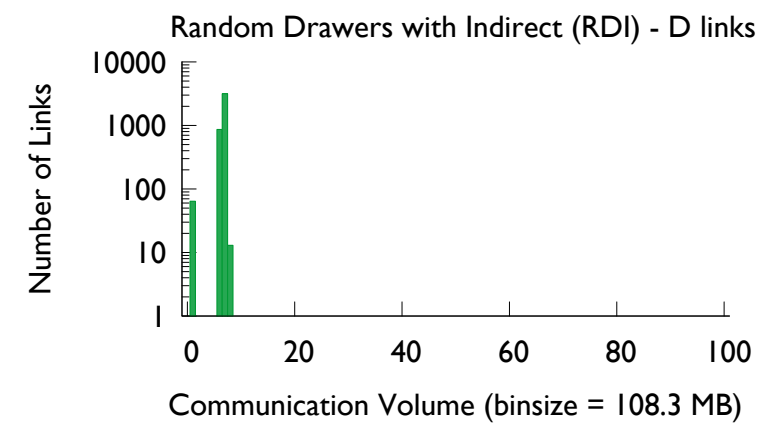
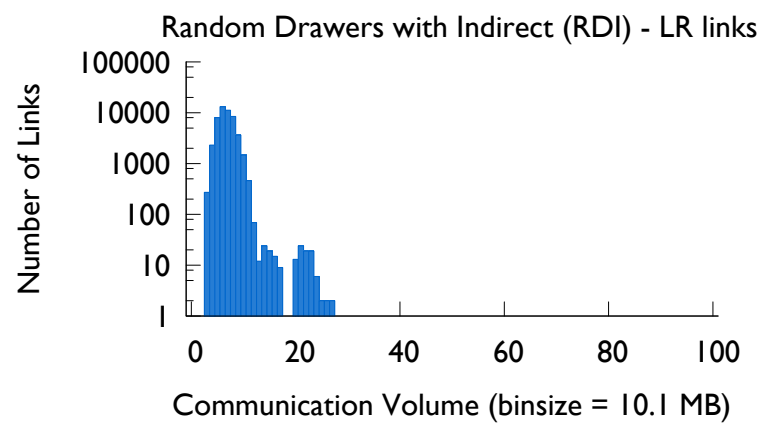
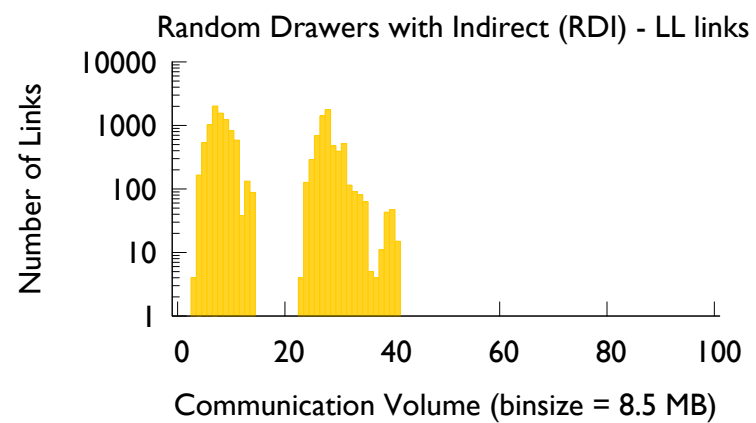
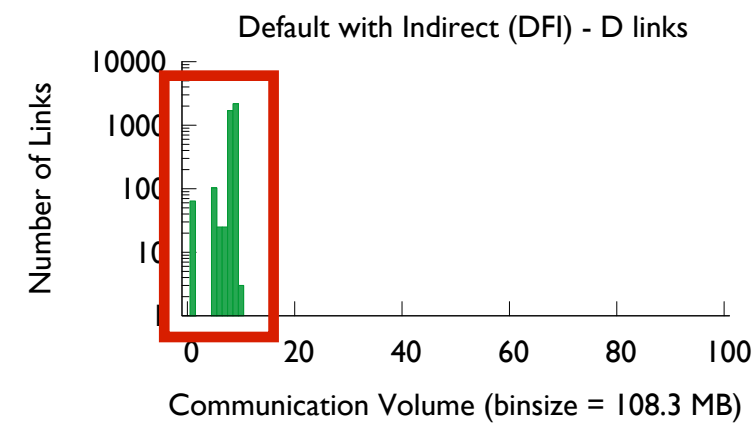
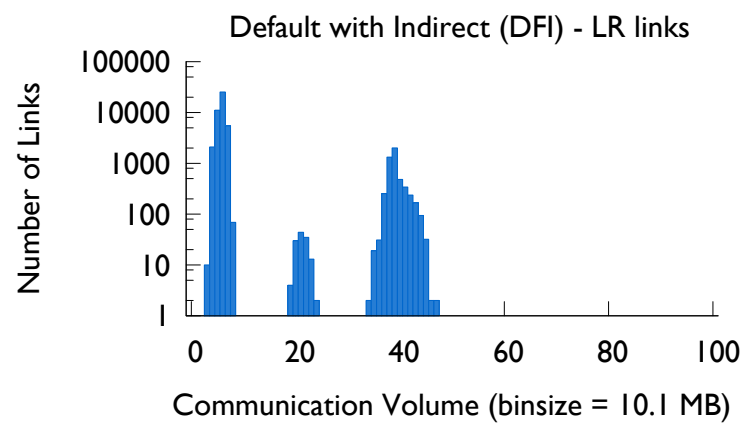
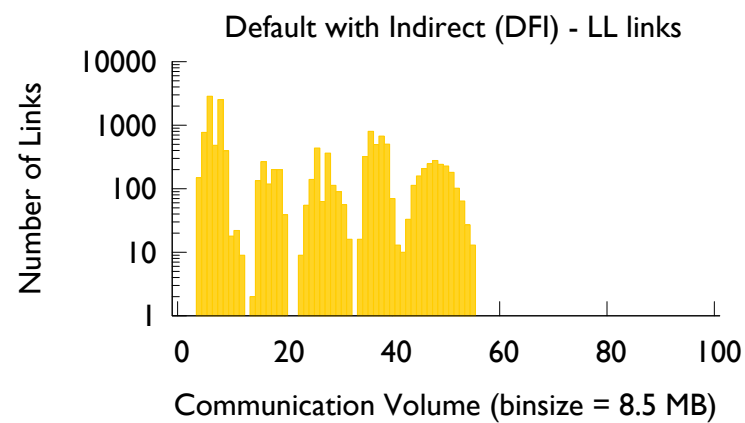
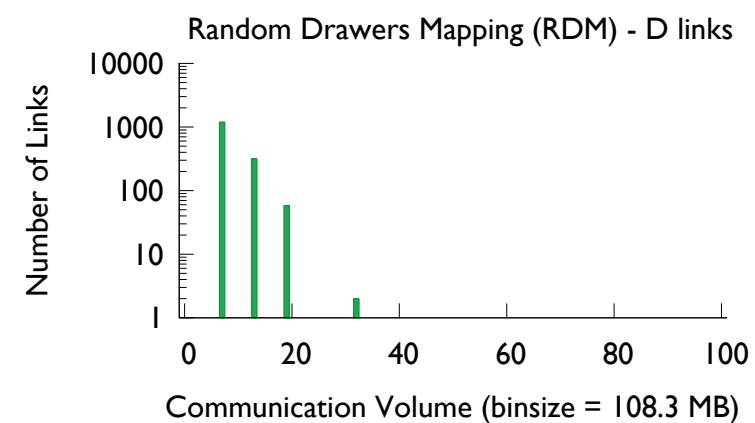
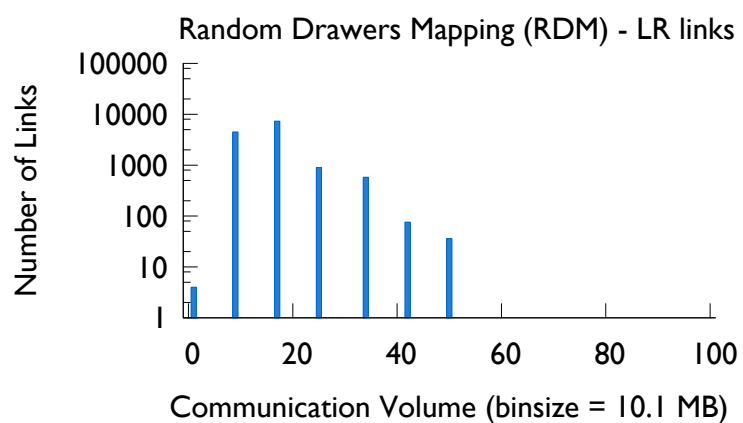
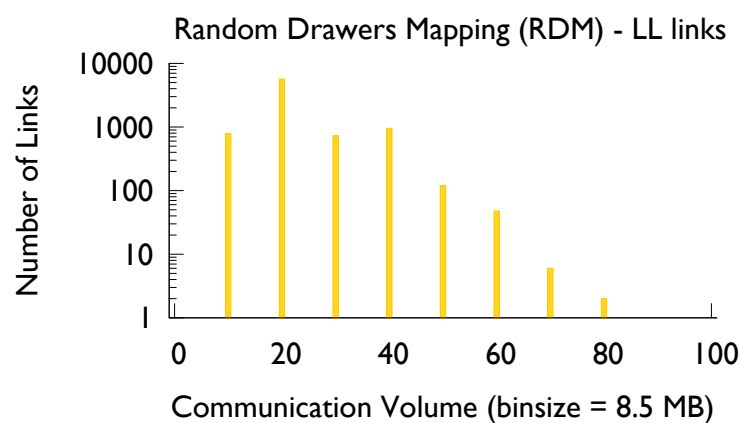
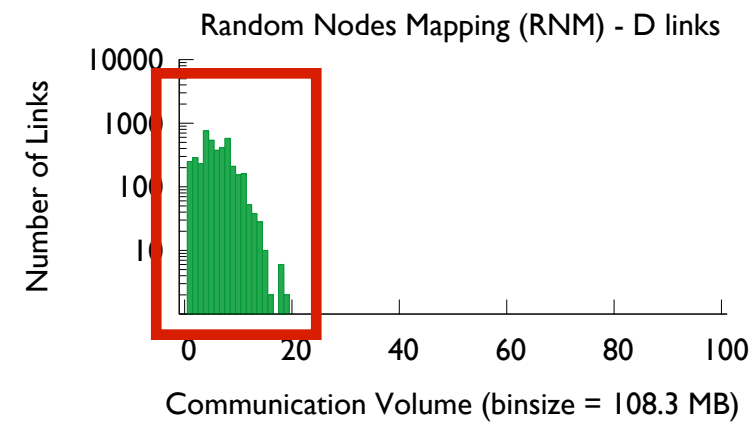
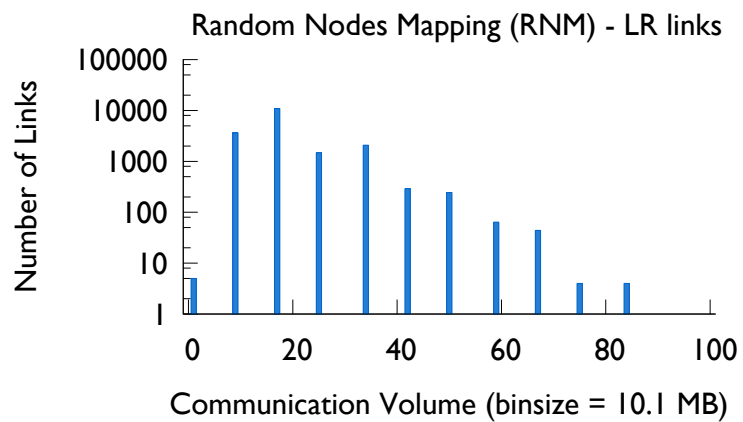
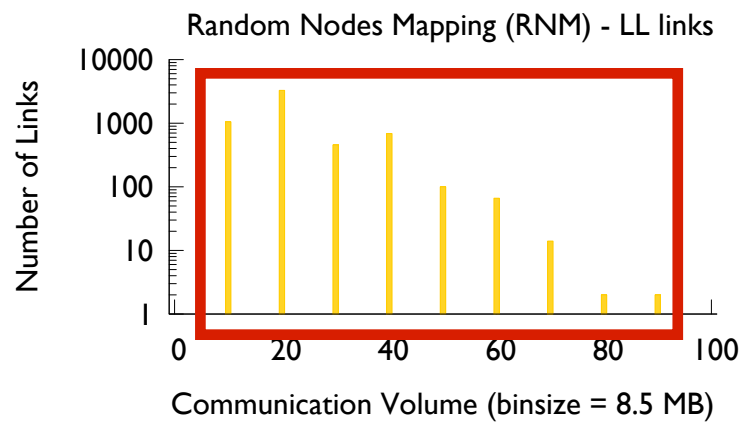
# 4D Stencil on 64 supernodes



# 4D Stencil on 64 supernodes

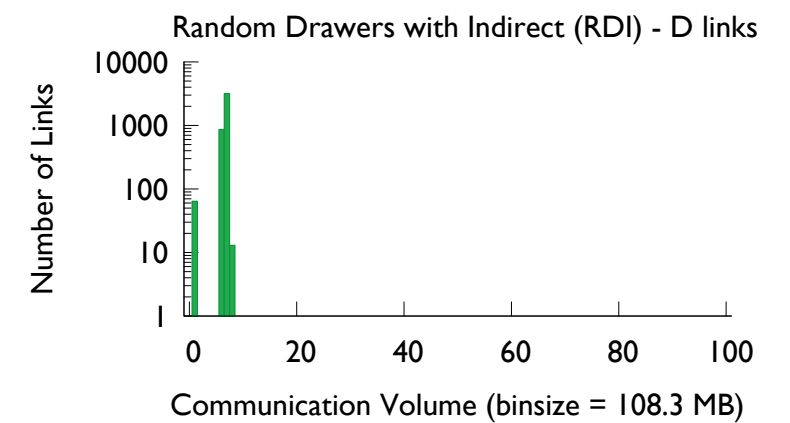
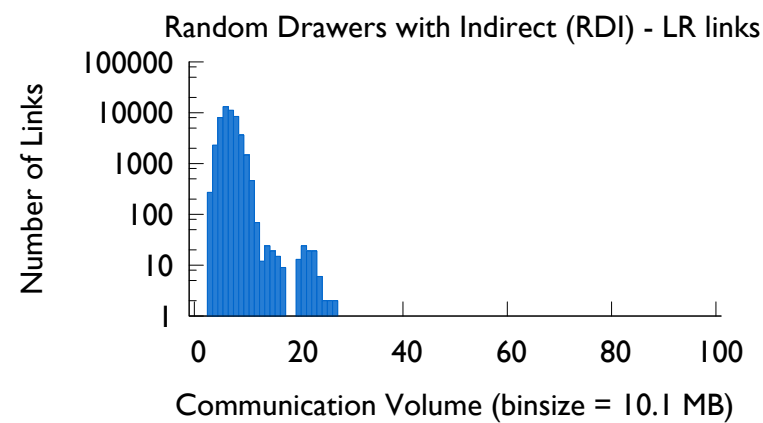
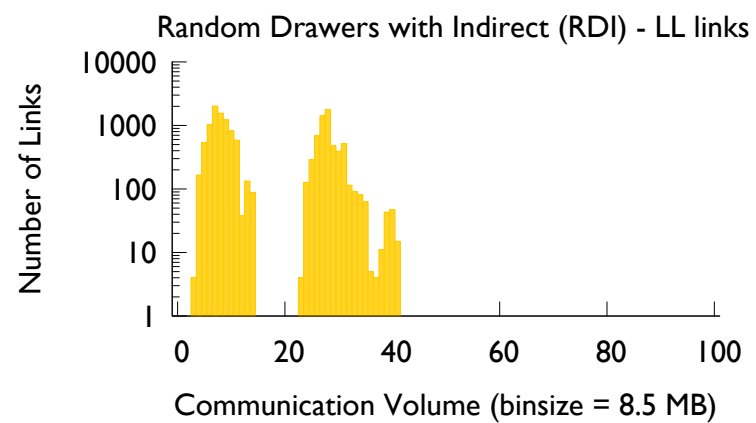
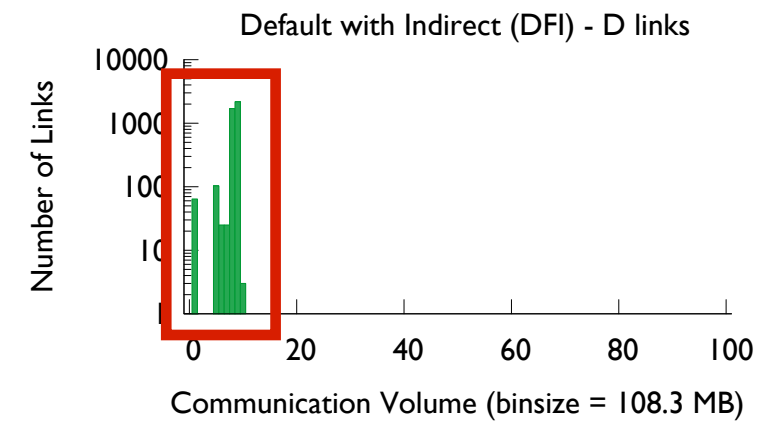
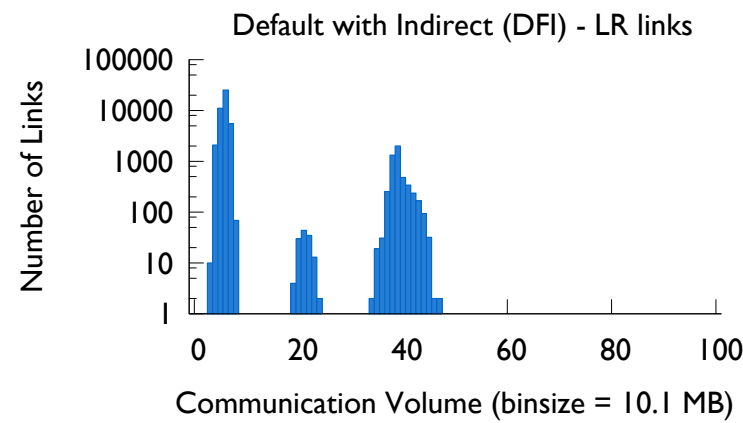
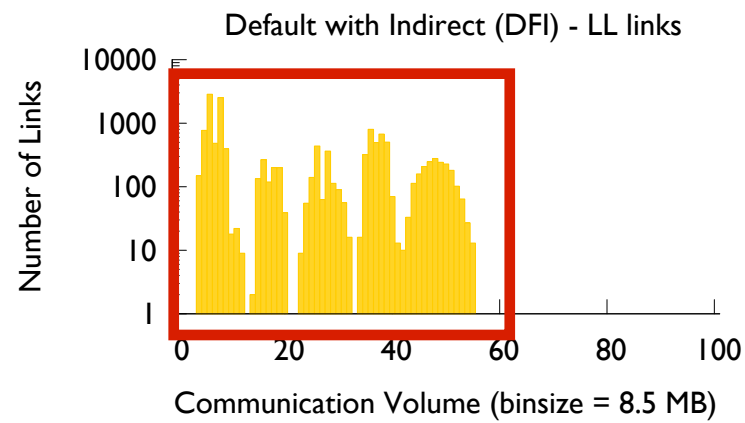
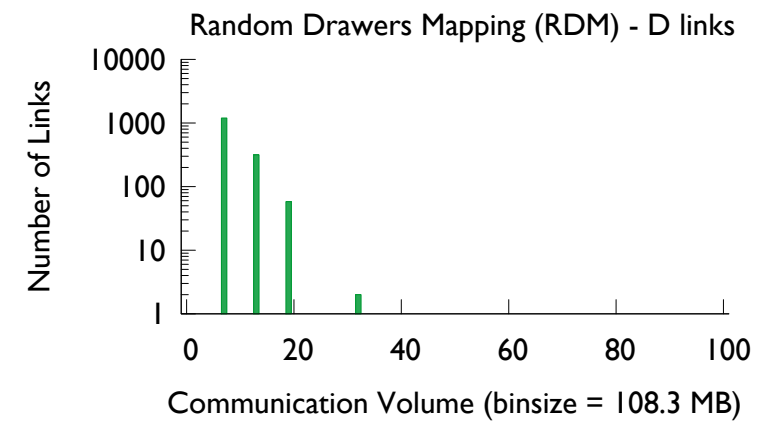
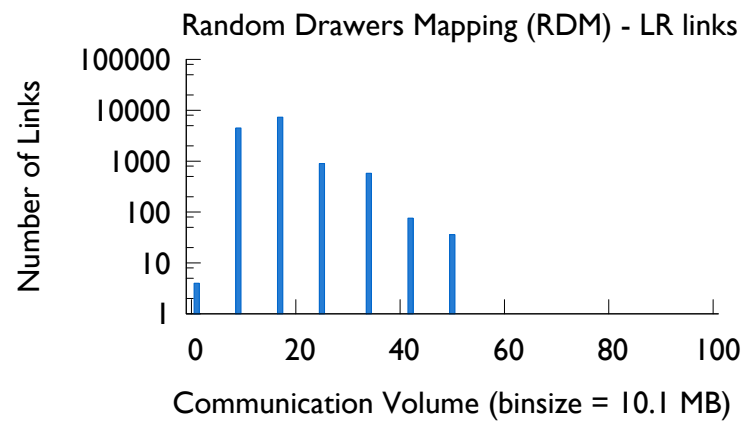
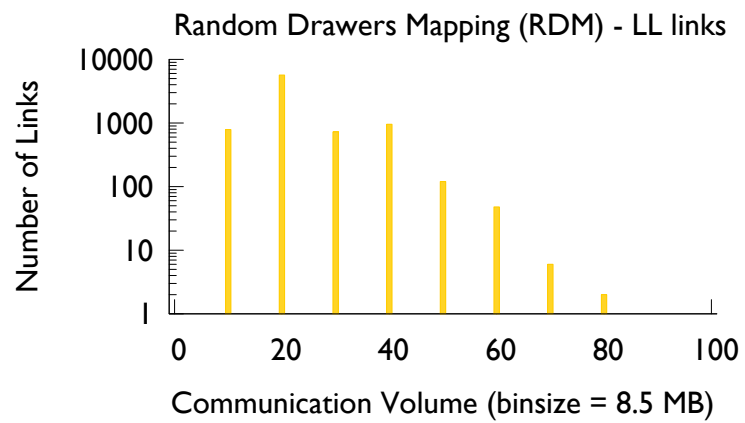
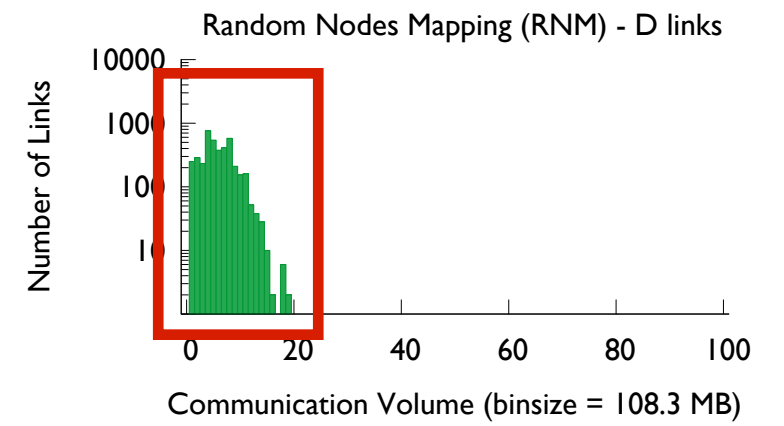
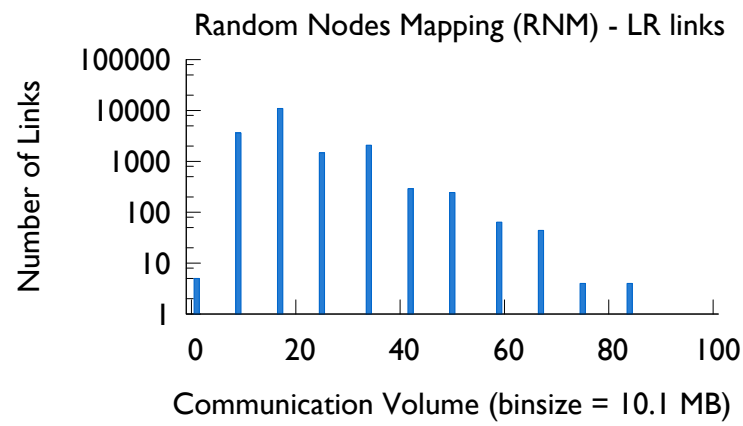
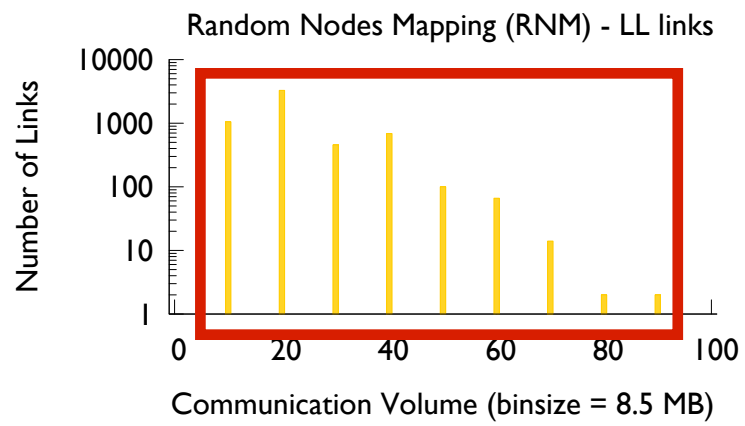


# 4D Stencil on 64 supernodes



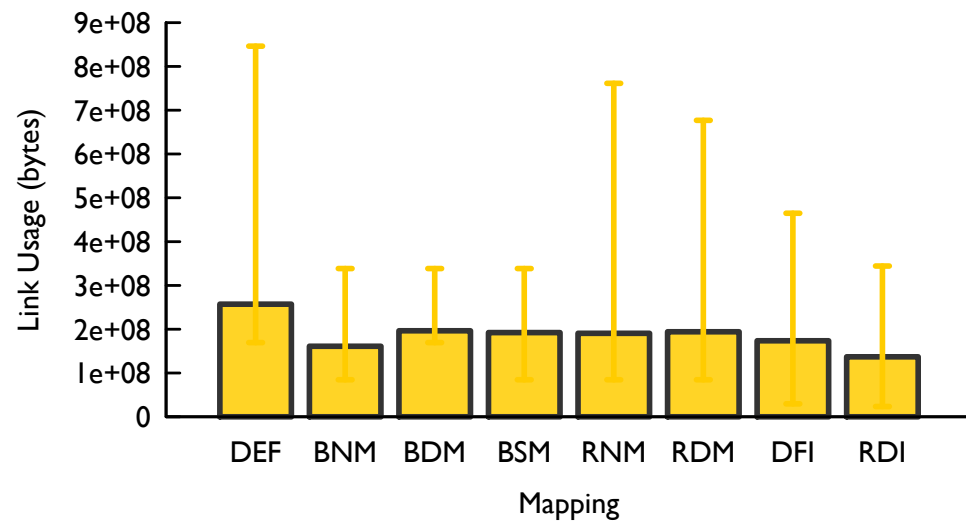


# 4D Stencil on 64 supernodes

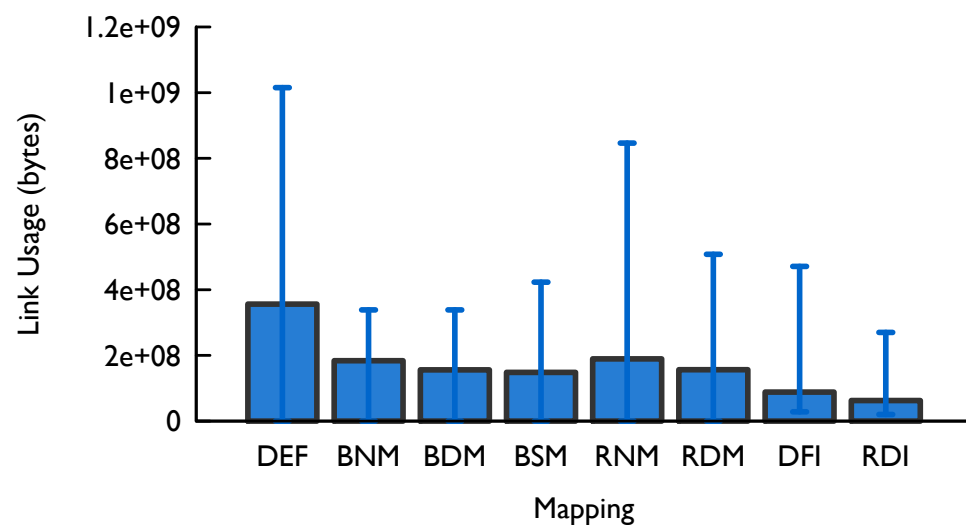


# 4D Stencil on 64 supernodes

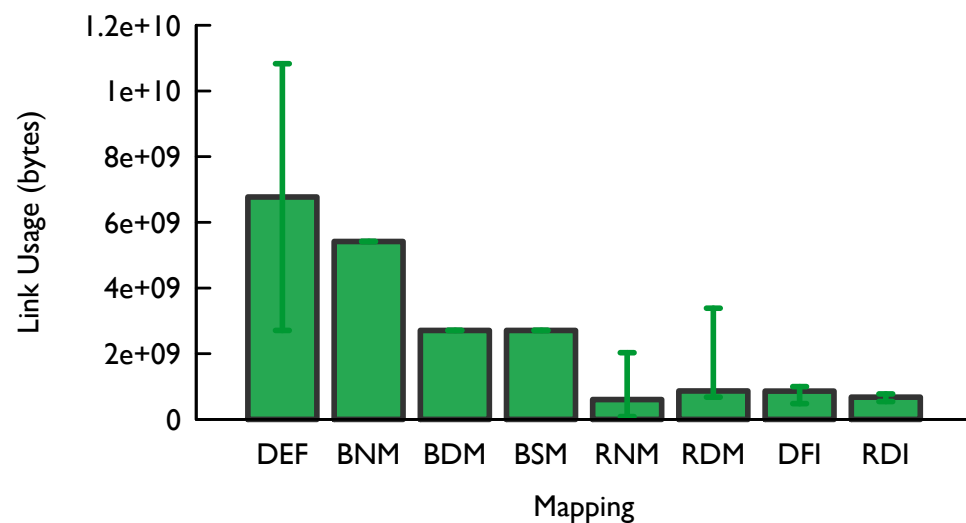
4D Stencil on 64 supernodes (LL links)



4D Stencil on 64 supernodes (LR links)

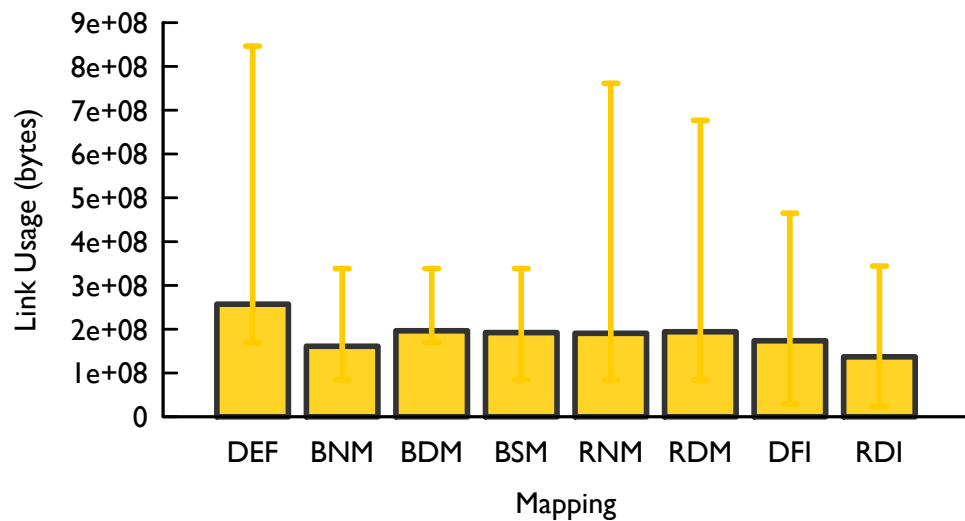


4D Stencil on 64 supernodes (D links)

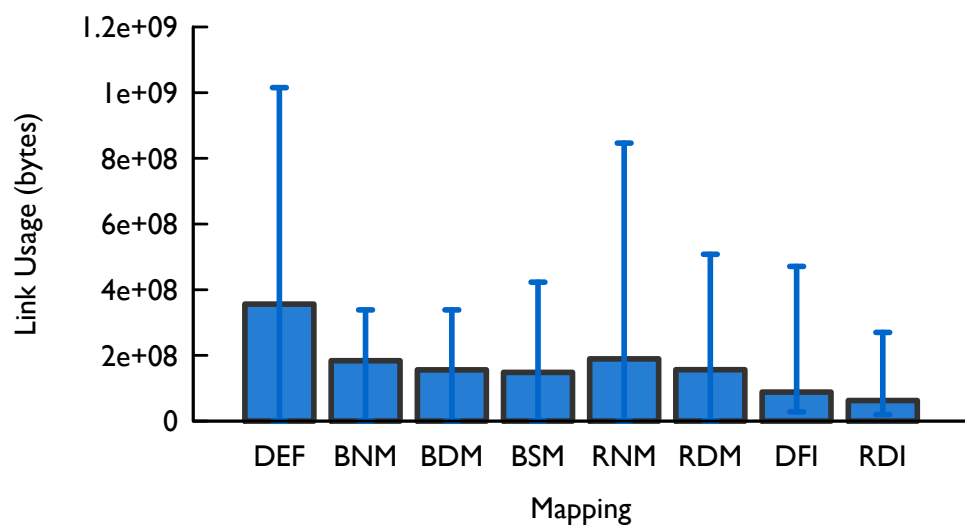


# 4D Stencil on 64 supernodes

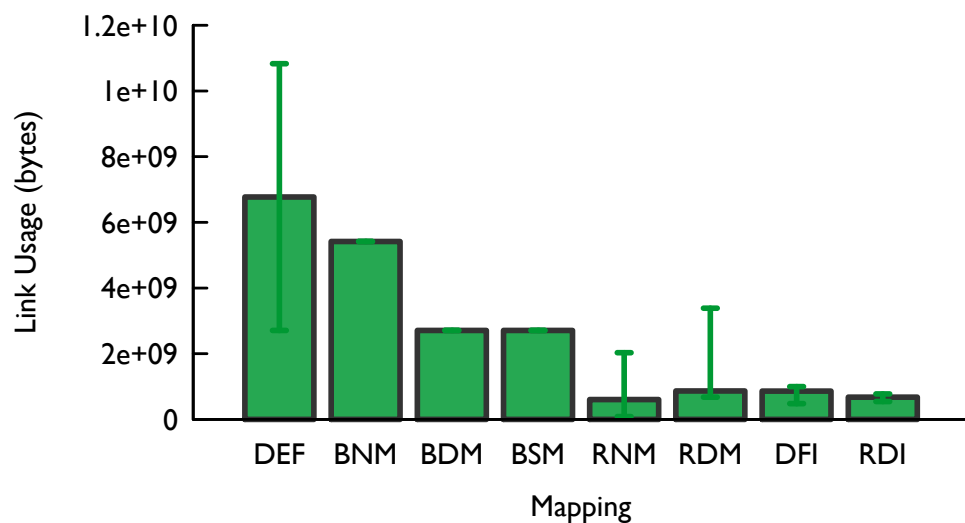
4D Stencil on 64 supernodes (LL links)



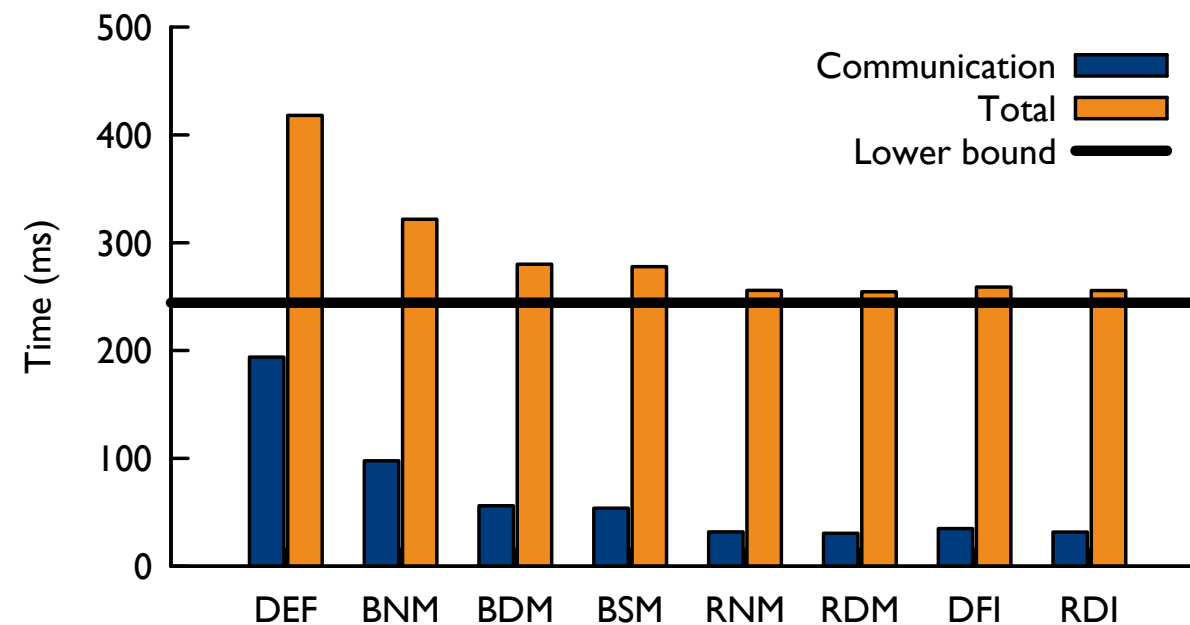
4D Stencil on 64 supernodes (LR links)



4D Stencil on 64 supernodes (D links)

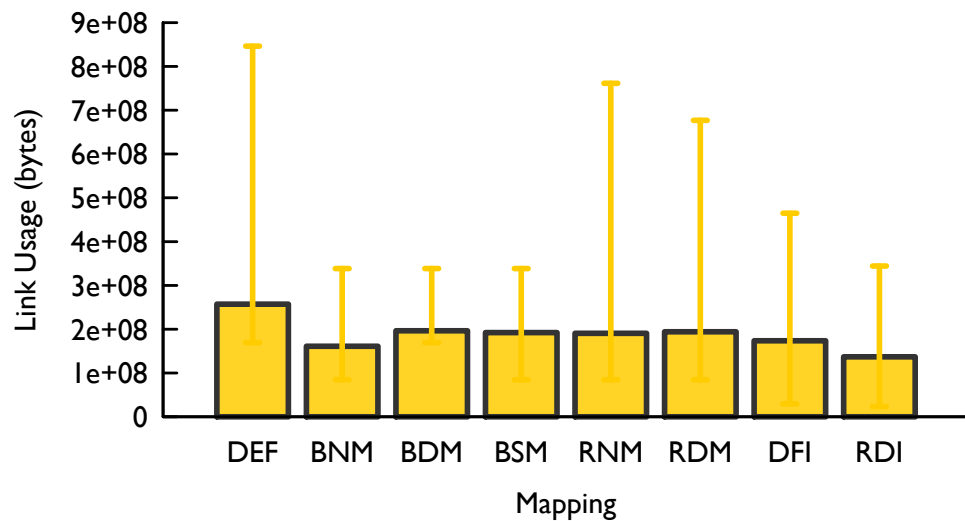


Performance of 4D Stencil on 64 supernodes

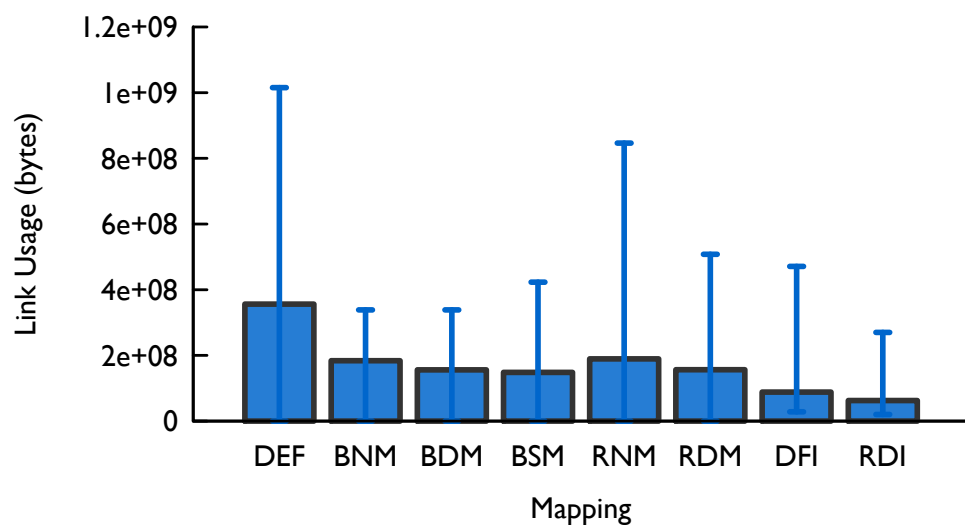


# 4D Stencil on 64 supernodes

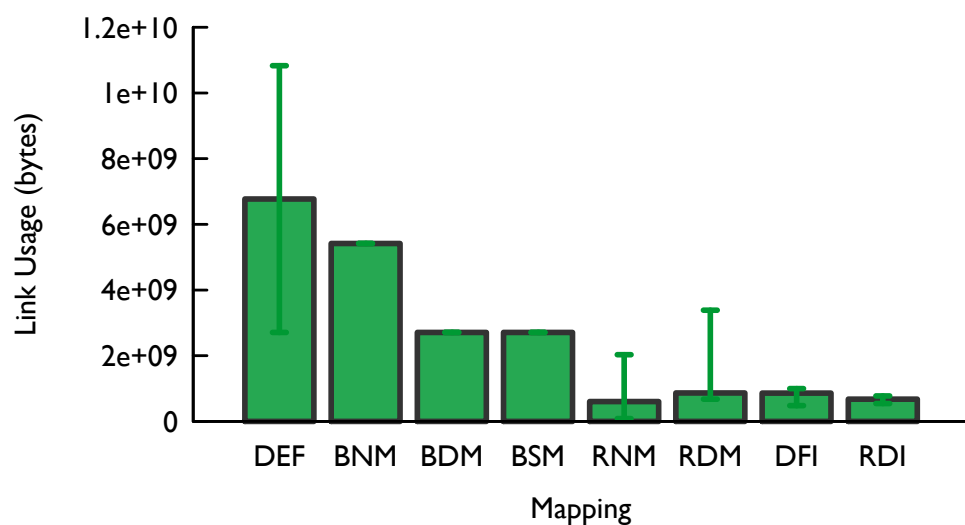
4D Stencil on 64 supernodes (LL links)



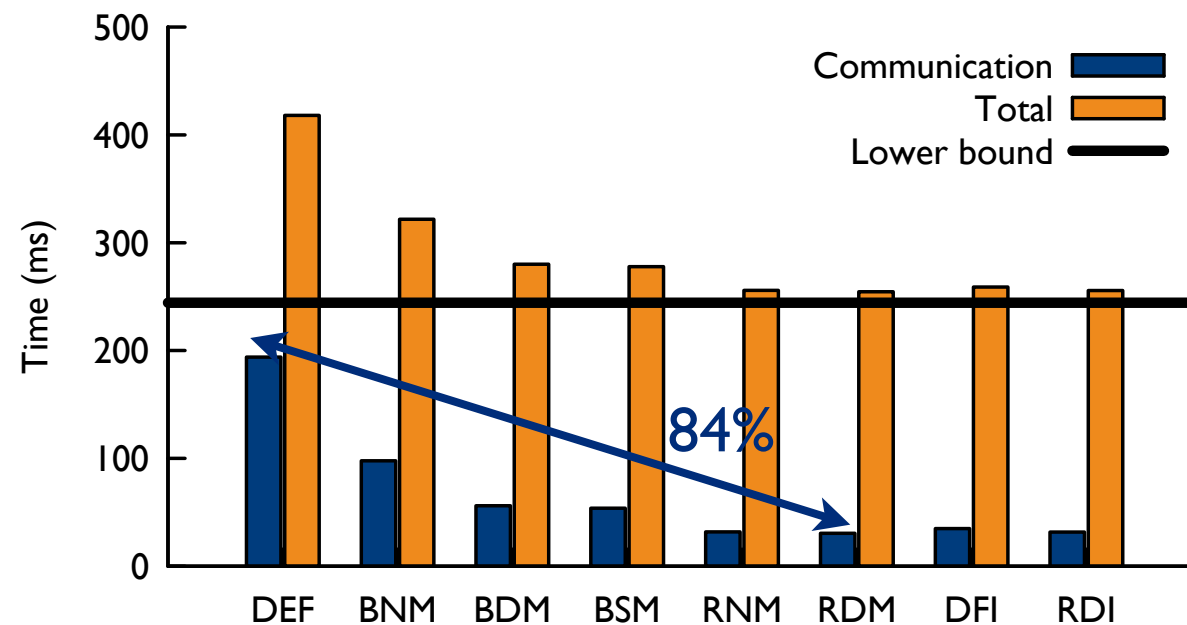
4D Stencil on 64 supernodes (LR links)



4D Stencil on 64 supernodes (D links)

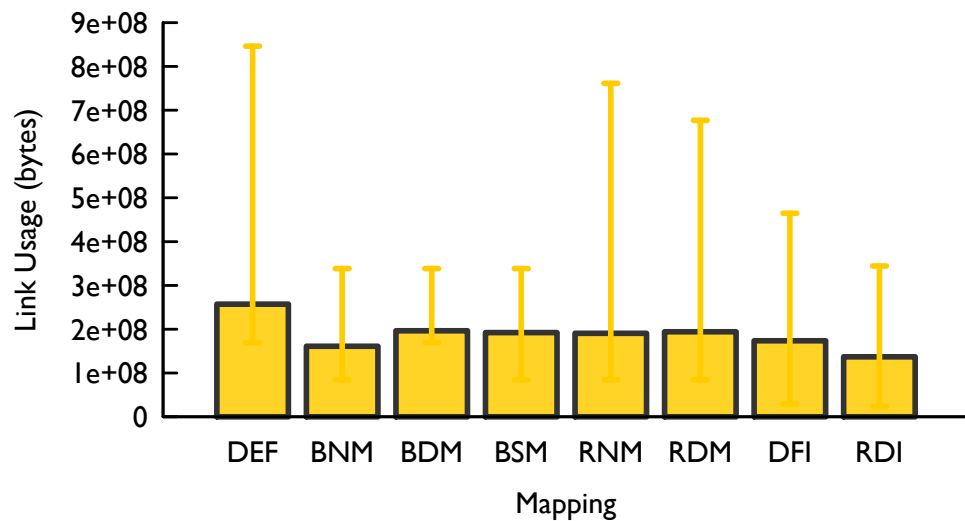


Performance of 4D Stencil on 64 supernodes

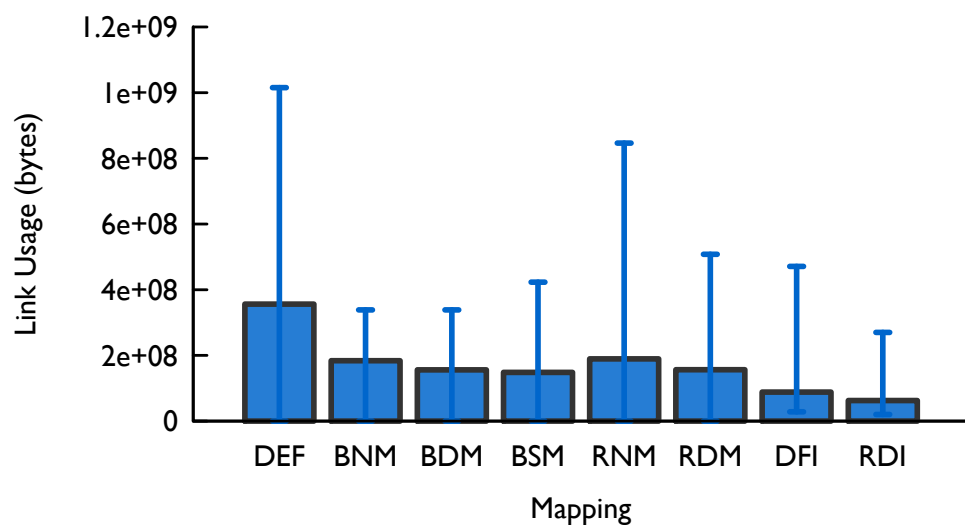


# 4D Stencil on 64 supernodes

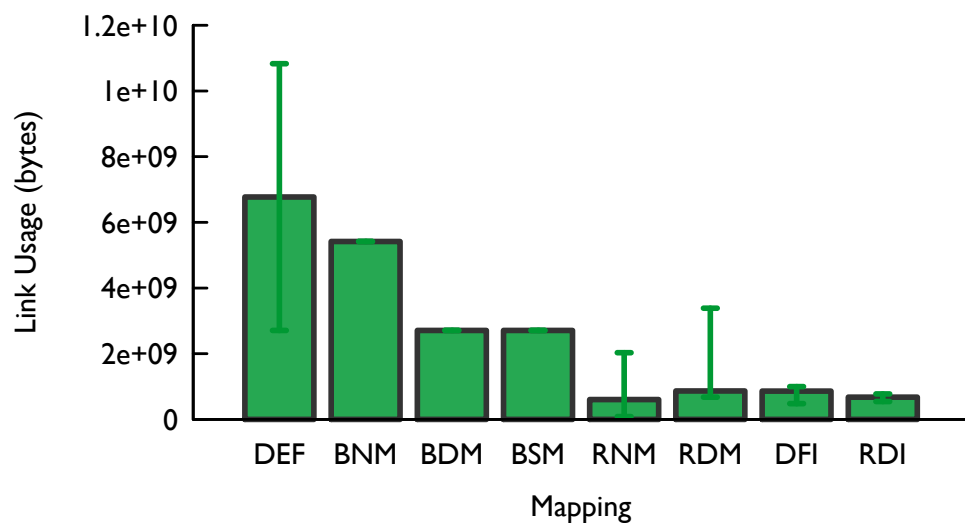
4D Stencil on 64 supernodes (LL links)



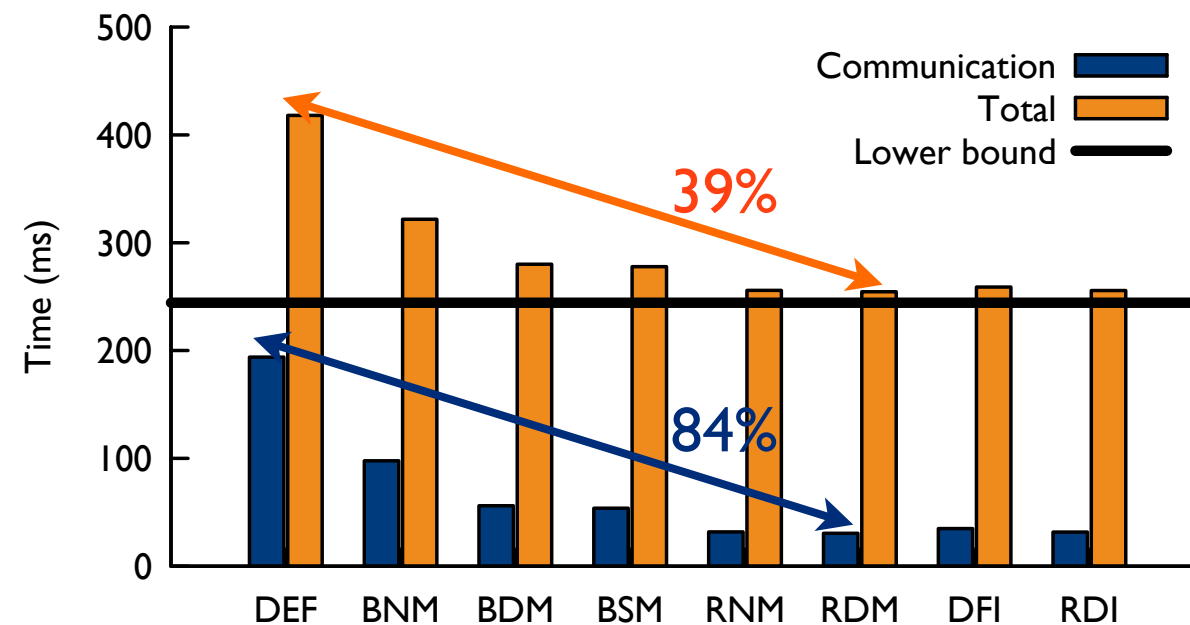
4D Stencil on 64 supernodes (LR links)



4D Stencil on 64 supernodes (D links)

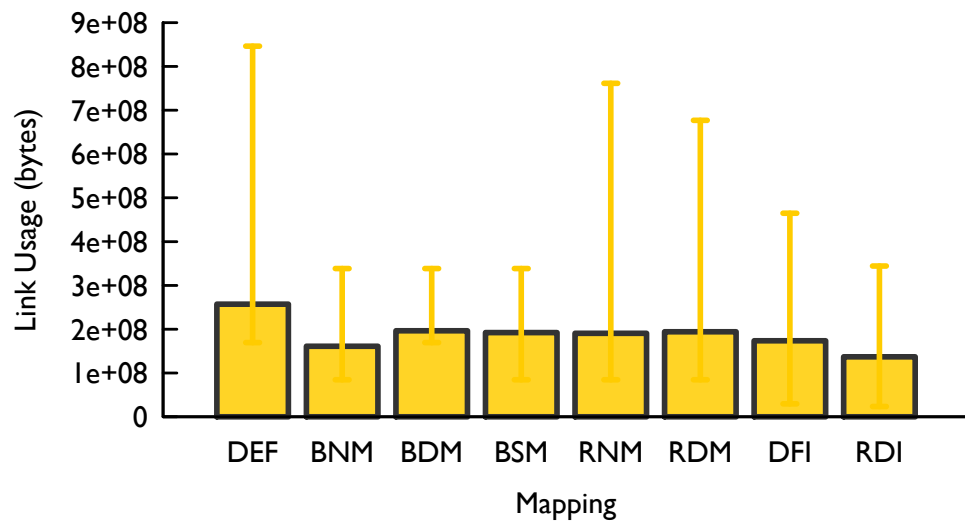


Performance of 4D Stencil on 64 supernodes

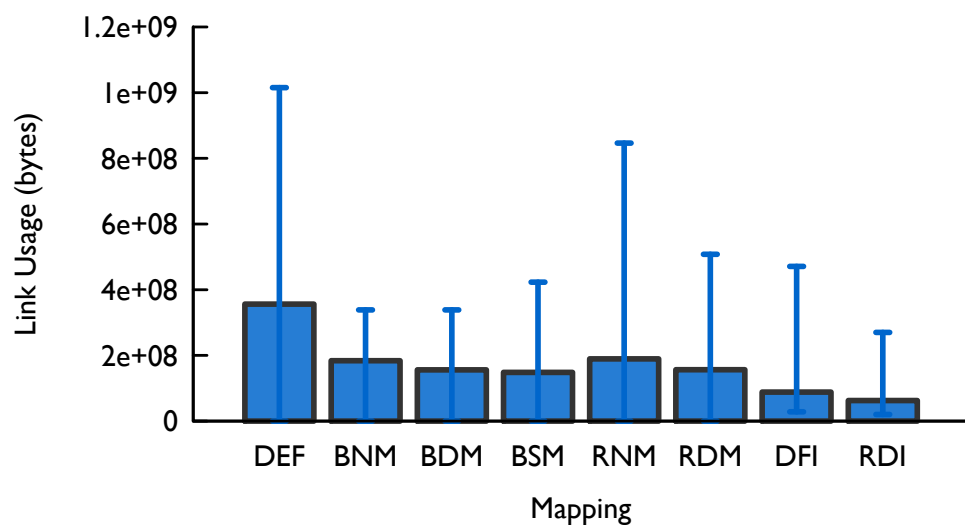


# 4D Stencil on 64 supernodes

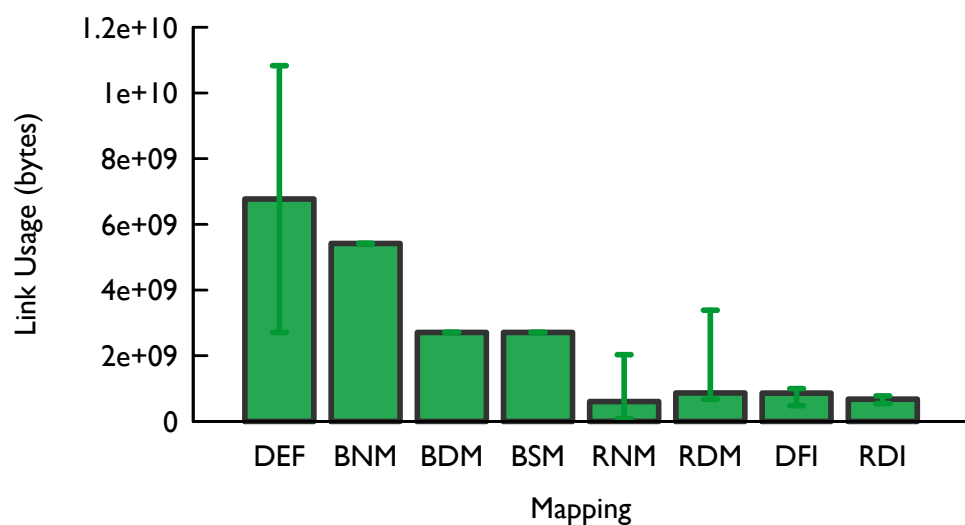
4D Stencil on 64 supernodes (LL links)



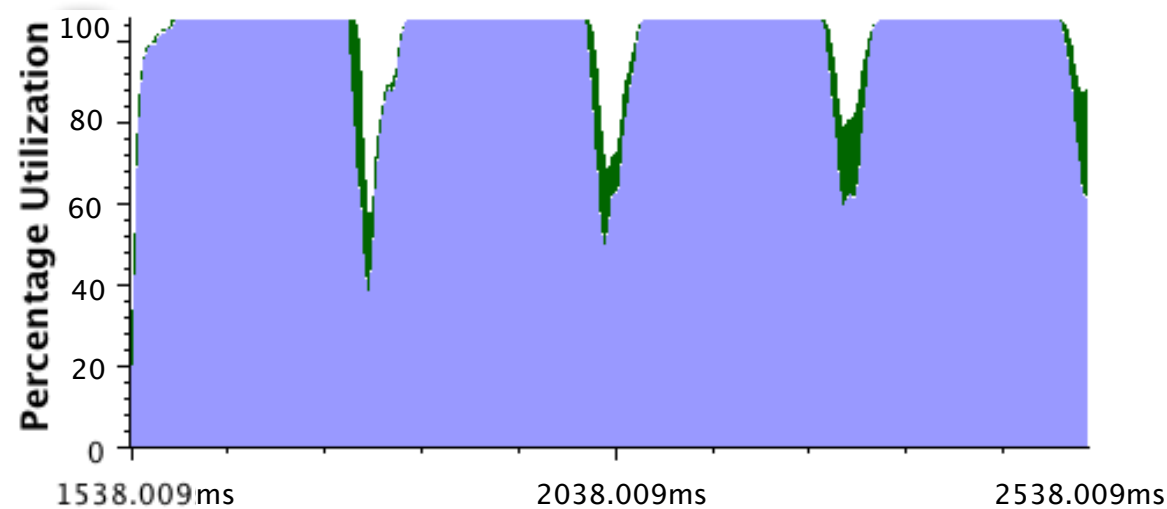
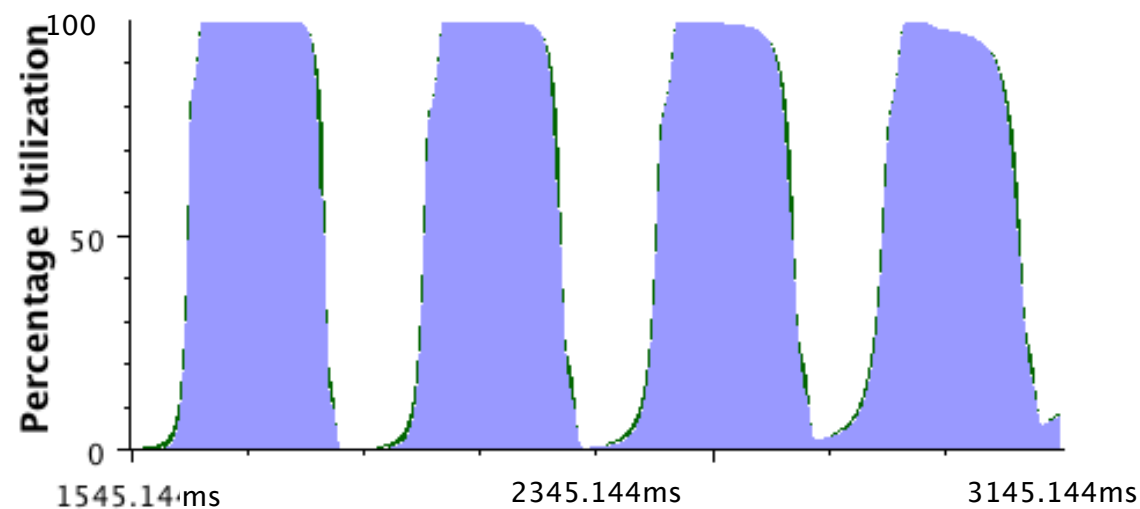
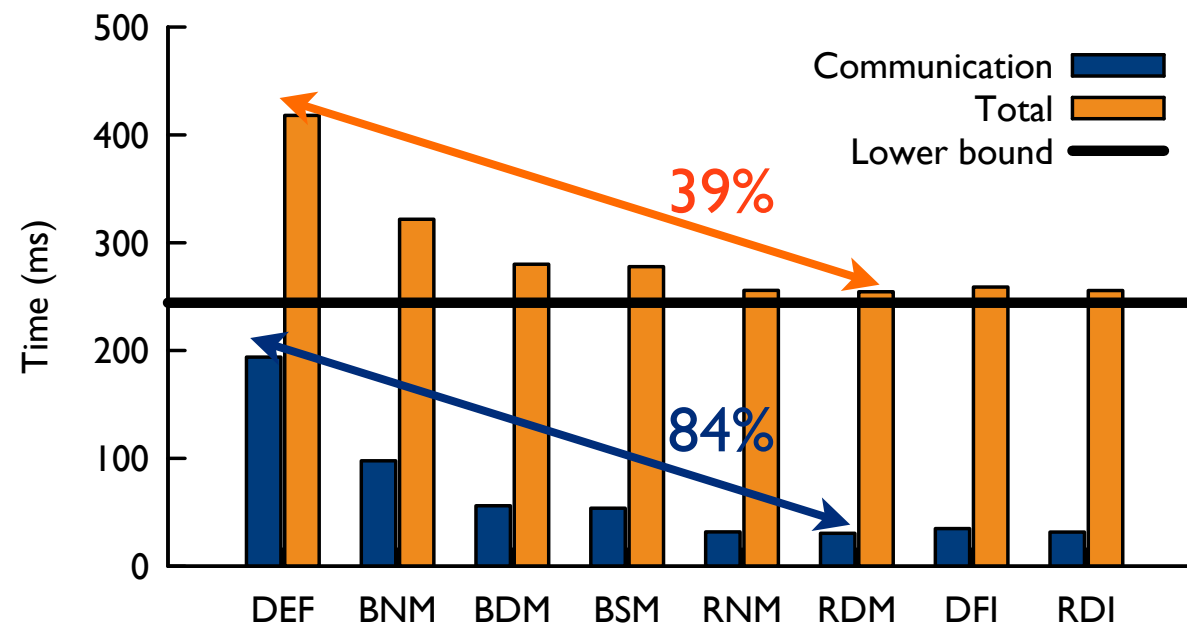
4D Stencil on 64 supernodes (LR links)



4D Stencil on 64 supernodes (D links)



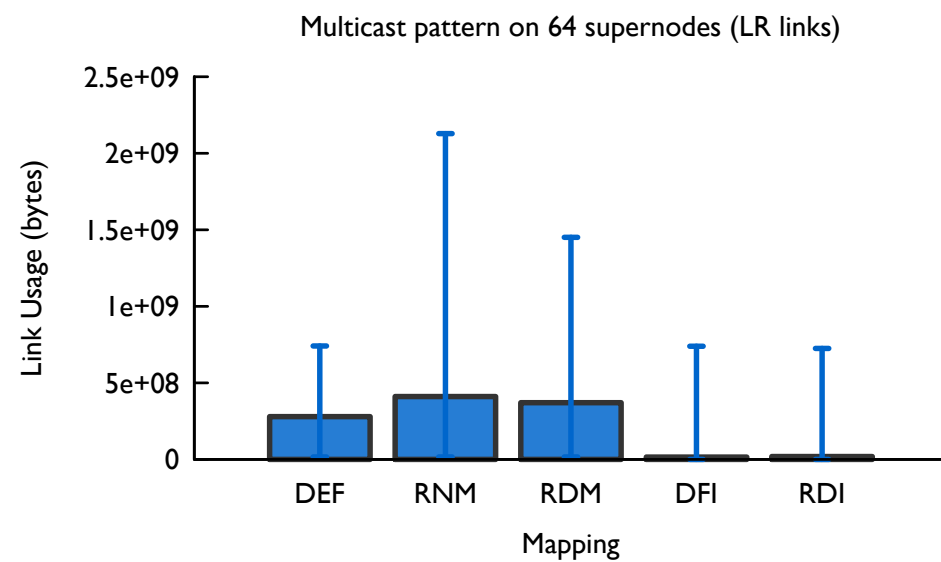
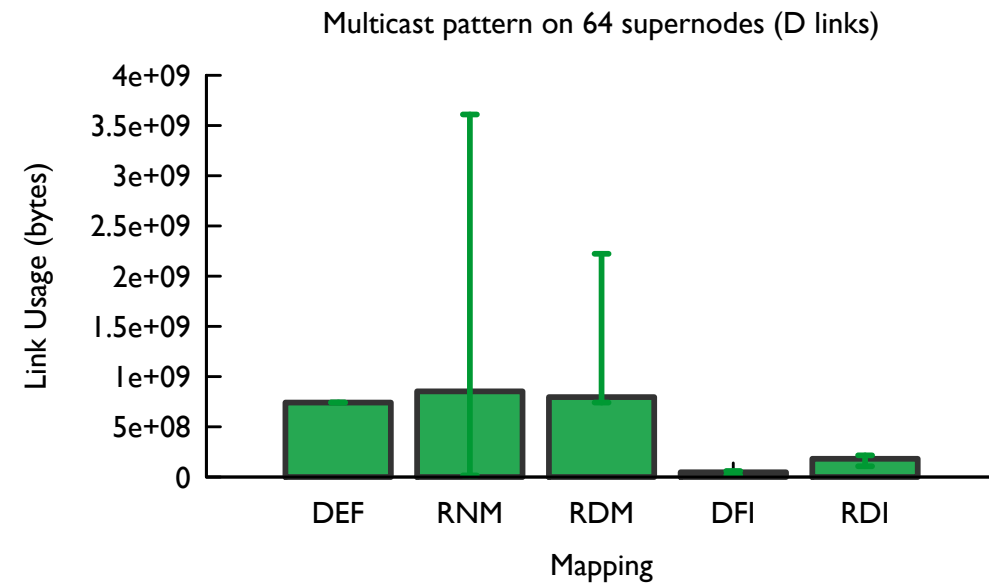
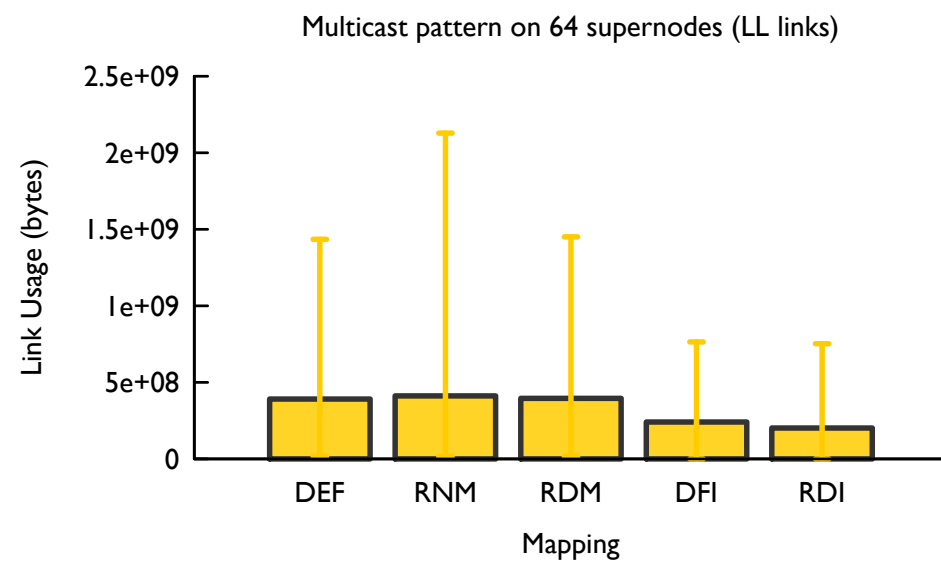
Performance of 4D Stencil on 64 supernodes



# n-targets multicast pattern

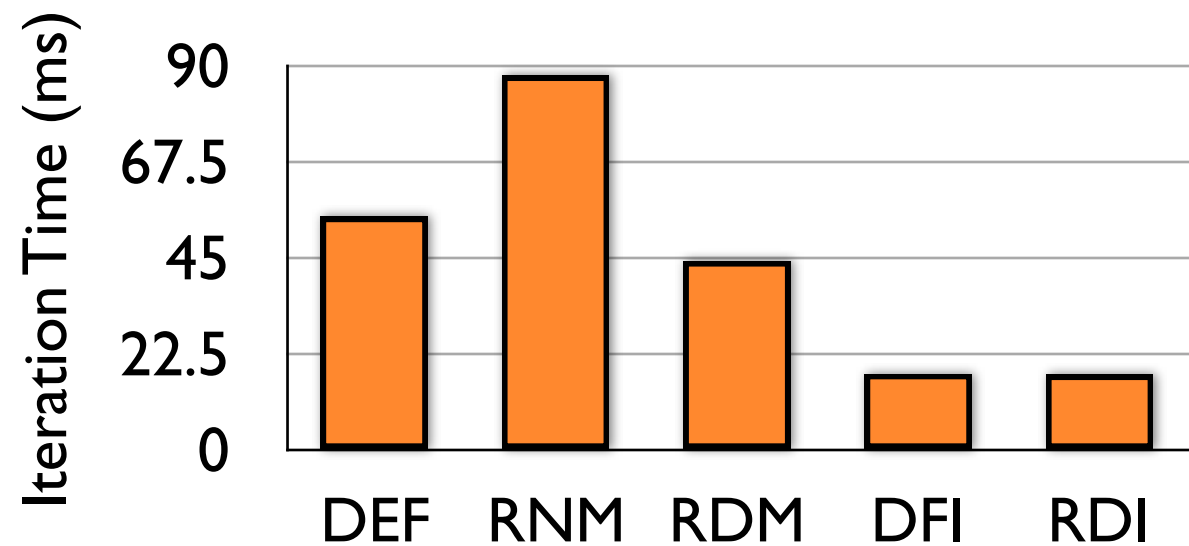
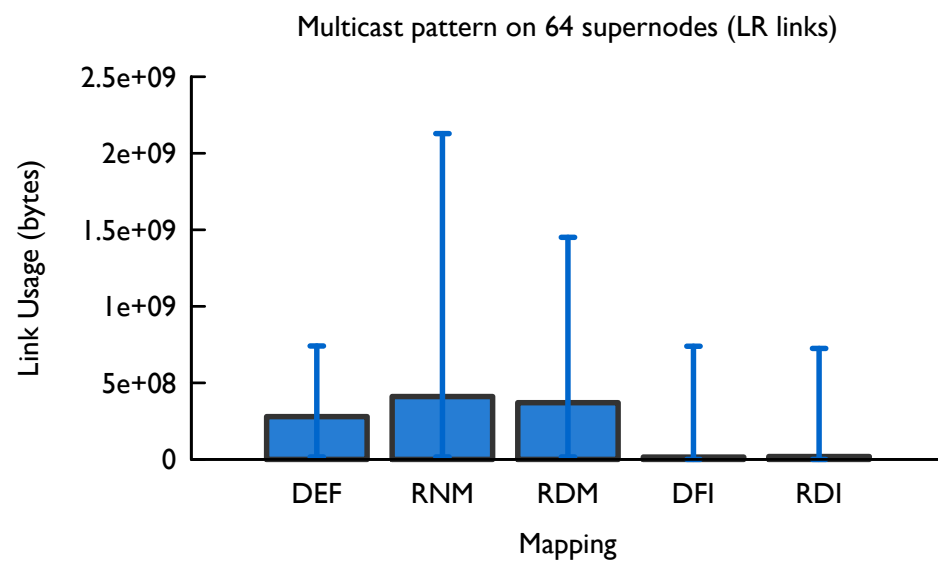
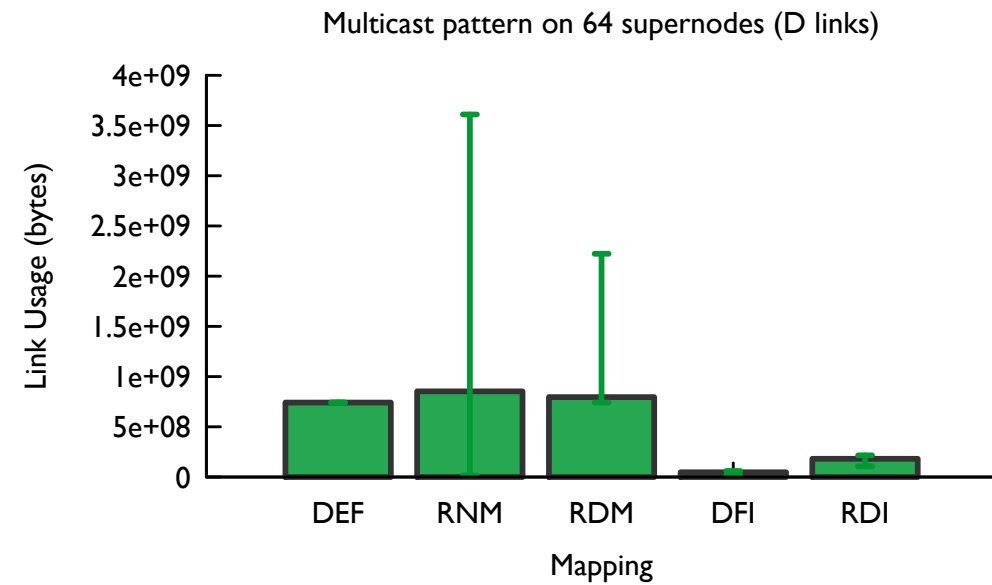
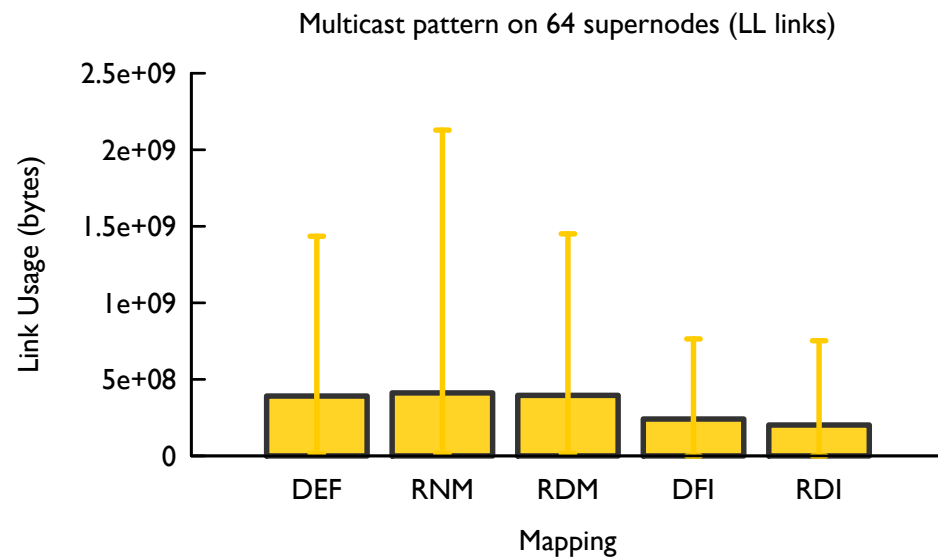
- Similar to the communication pattern in NAMD
- Each MPI task sends messages to 14 others
- Message size = 1 MB

# n-targets multicast pattern

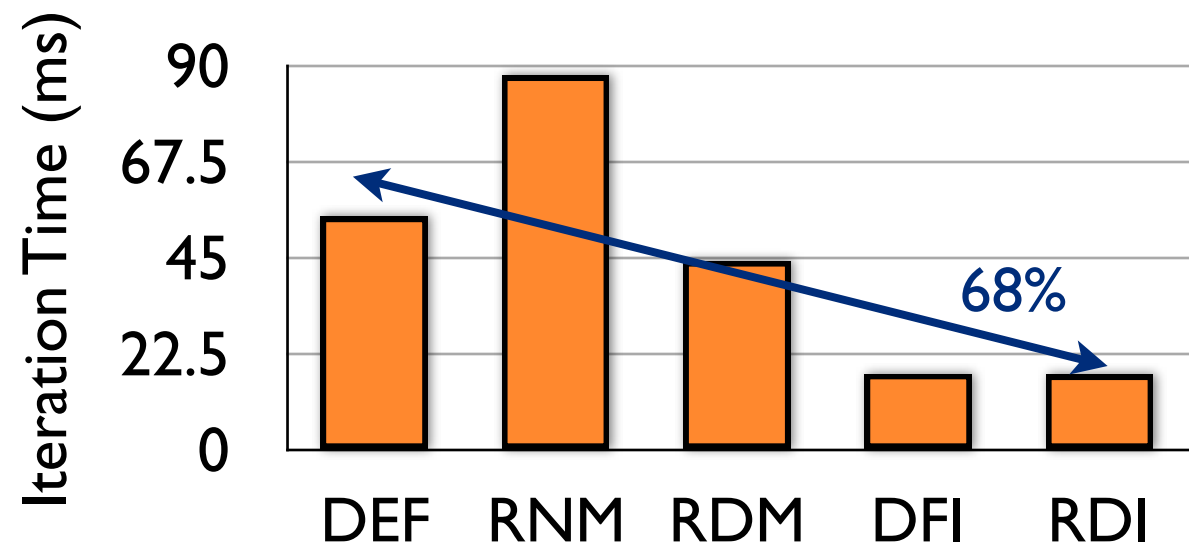
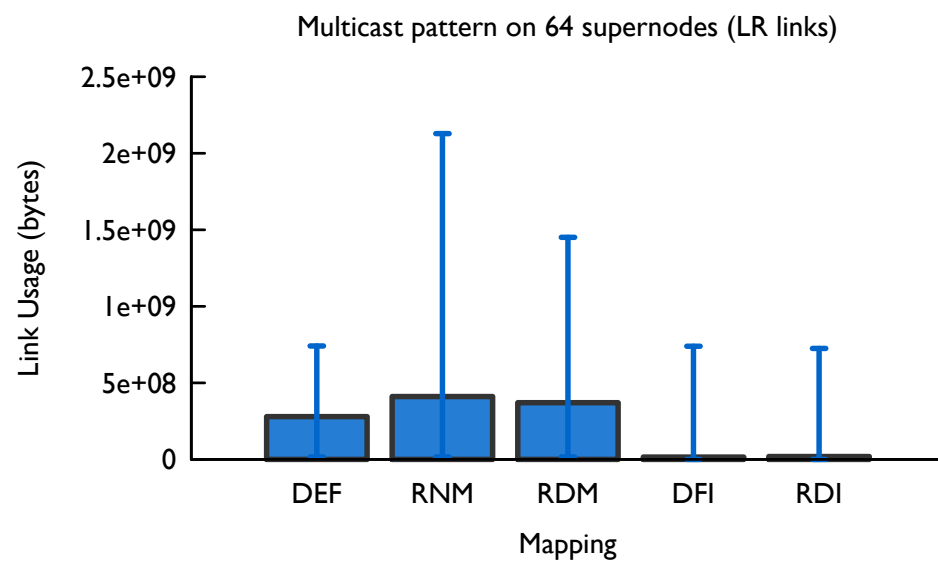
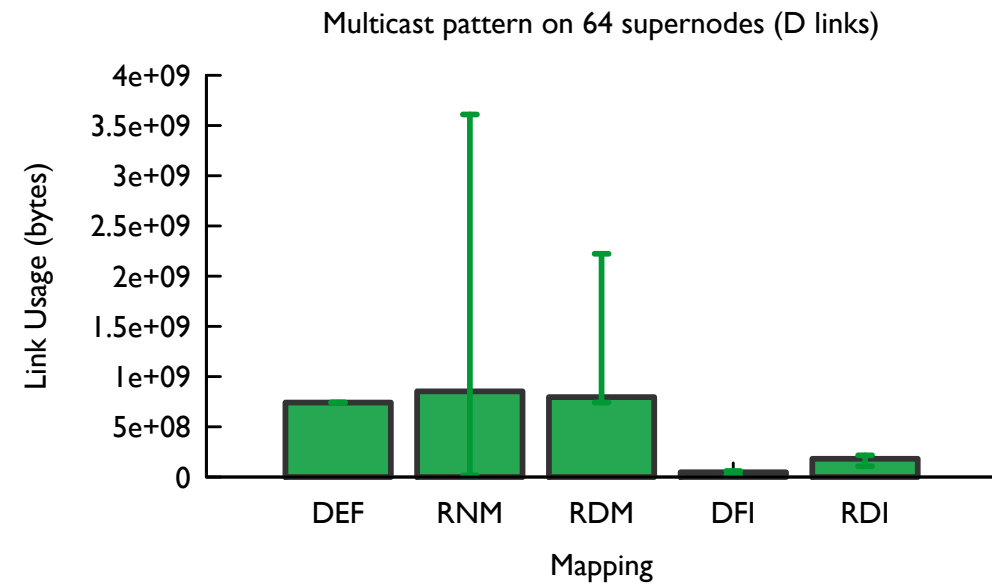
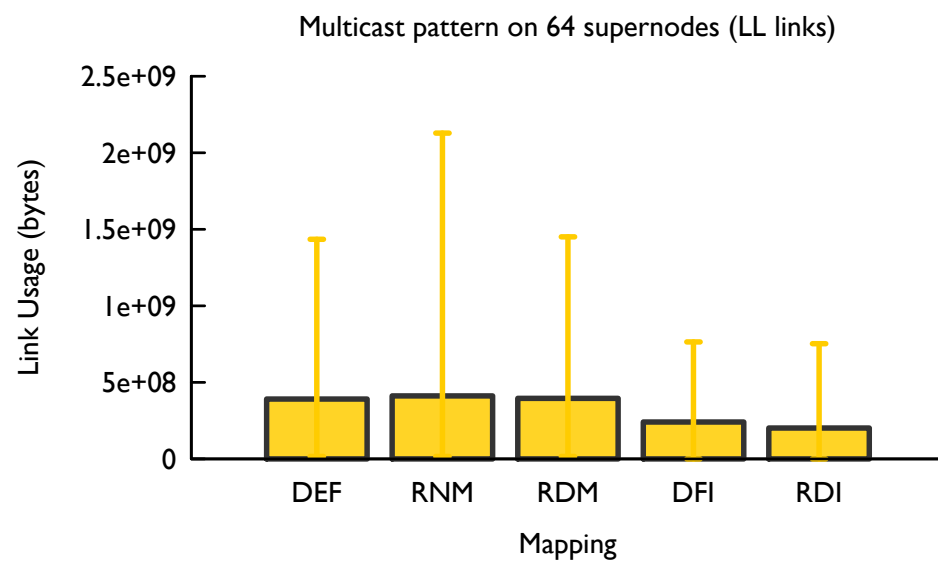




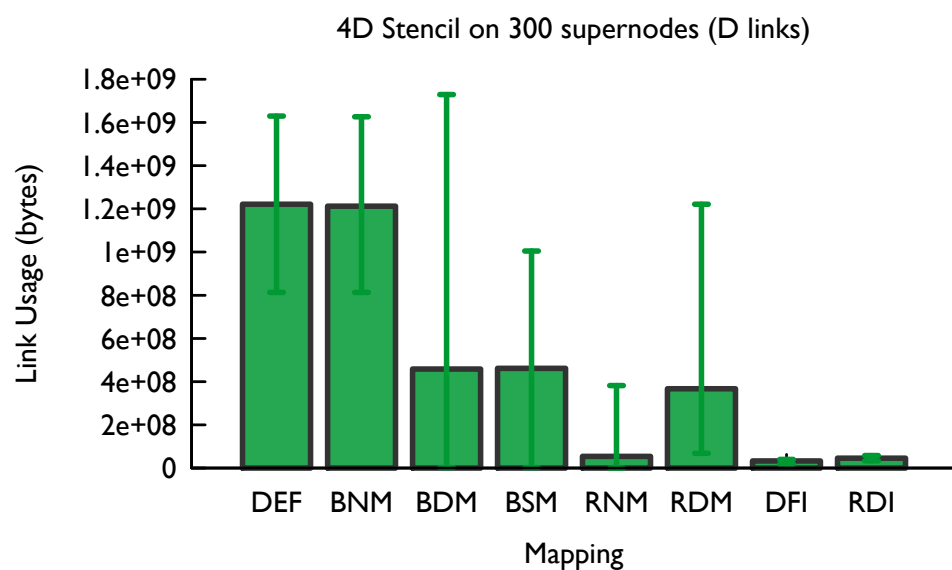
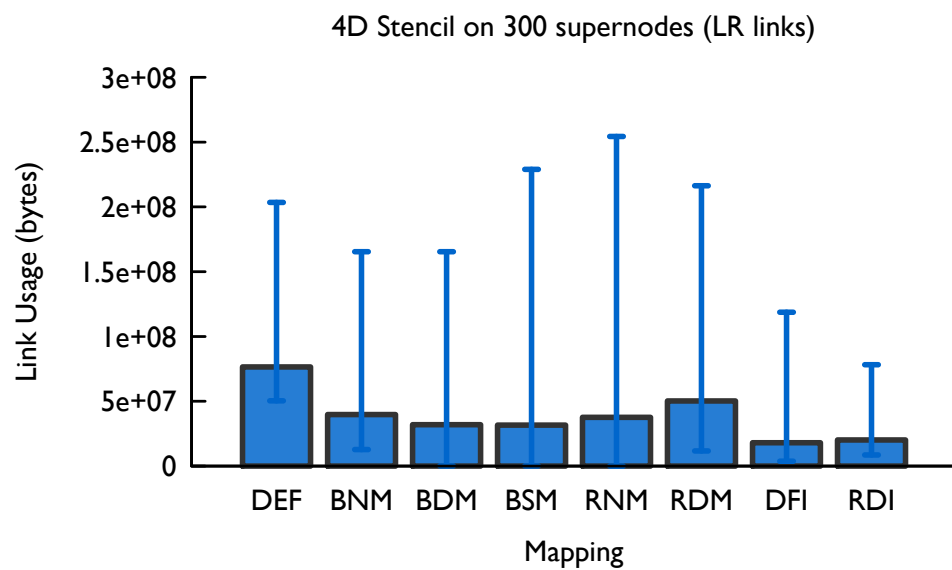
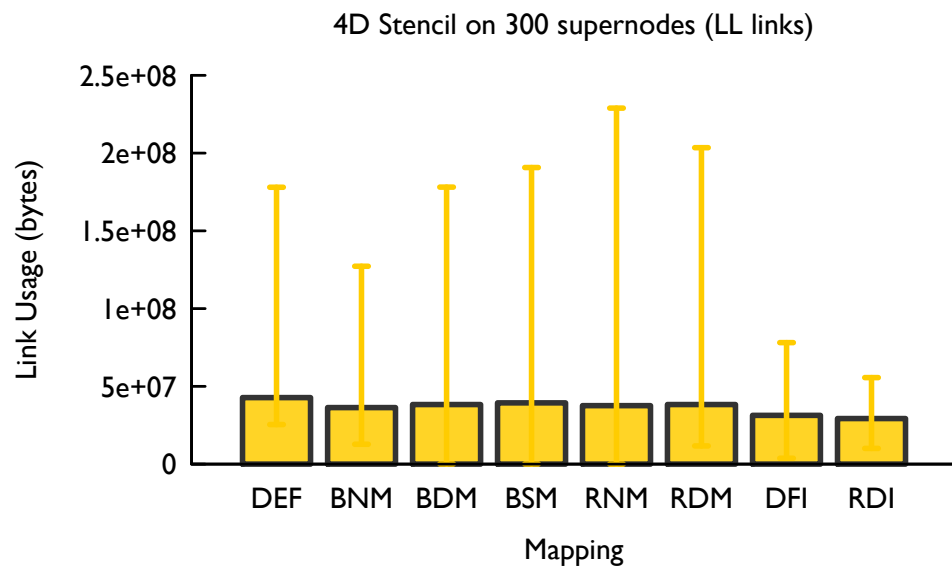
# n-targets multicast pattern



# n-targets multicast pattern



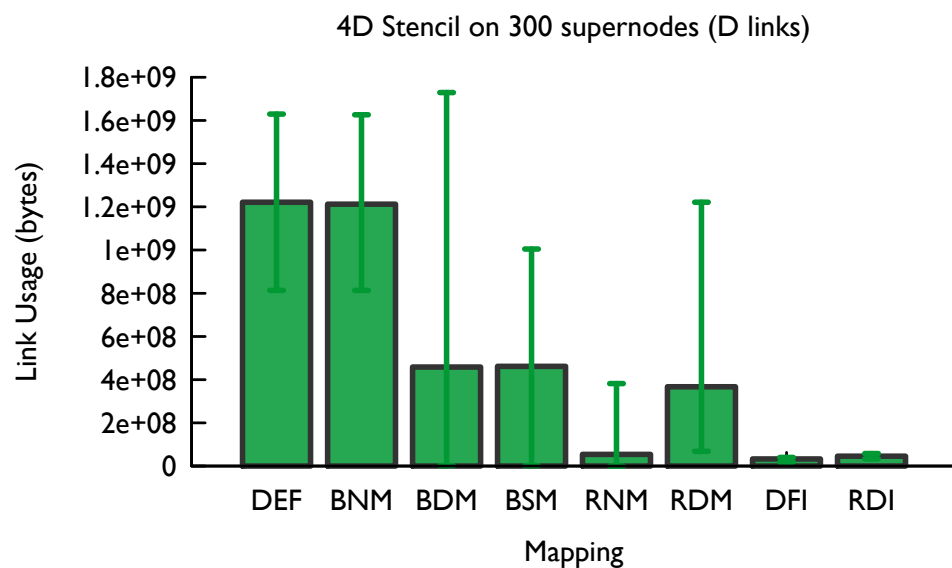
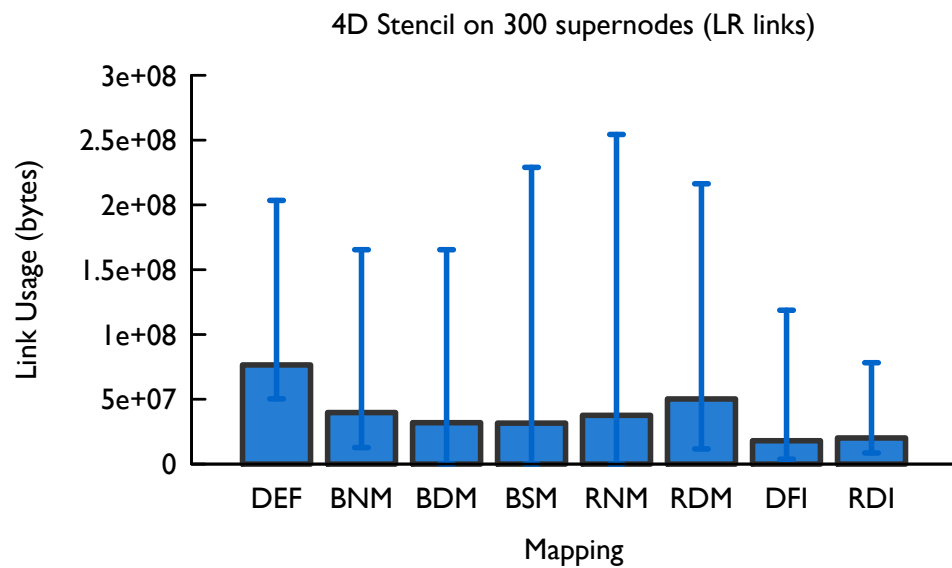
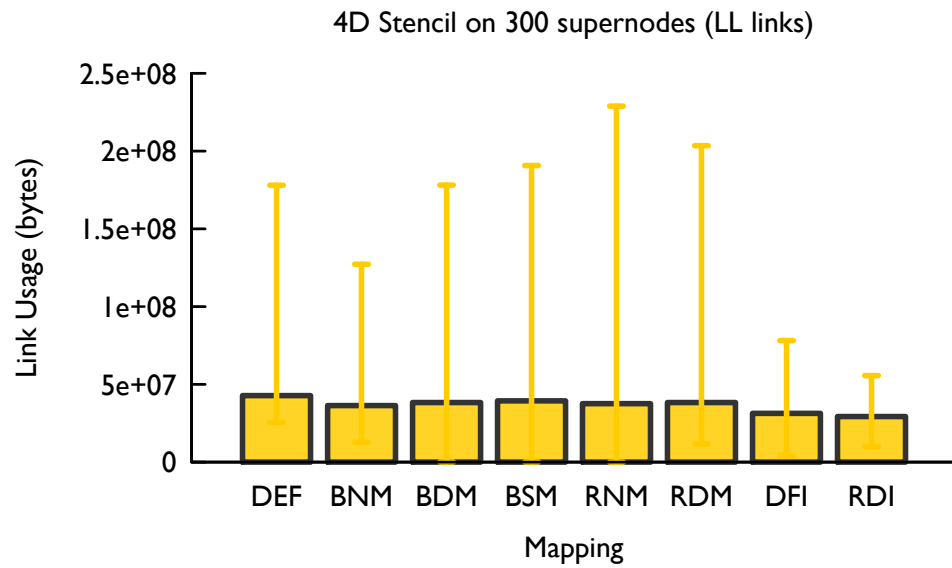
# 4D Stencil on 300 supernodes



- Largest detailed network simulation so far = 307,200 MPI tasks
- Non-power-of-2 leads to more complex mapping
- Message size = 1 MB

Text

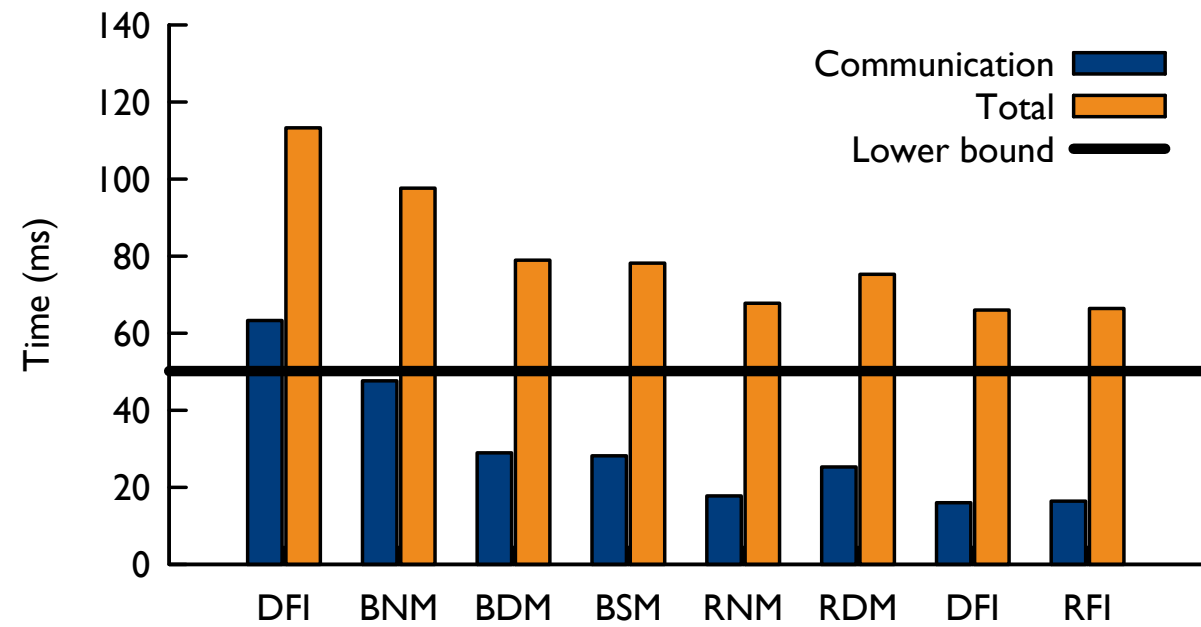
# 4D Stencil on 300 supernodes



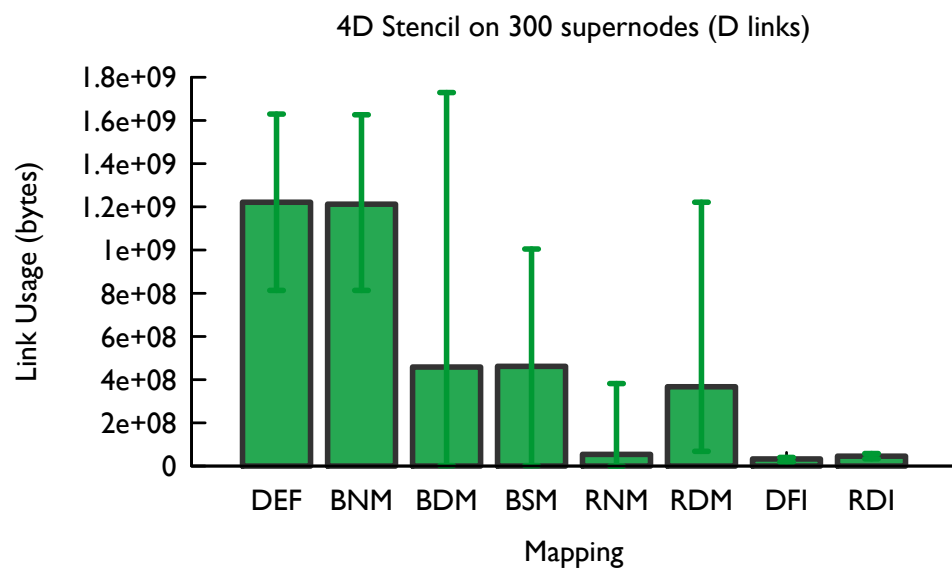
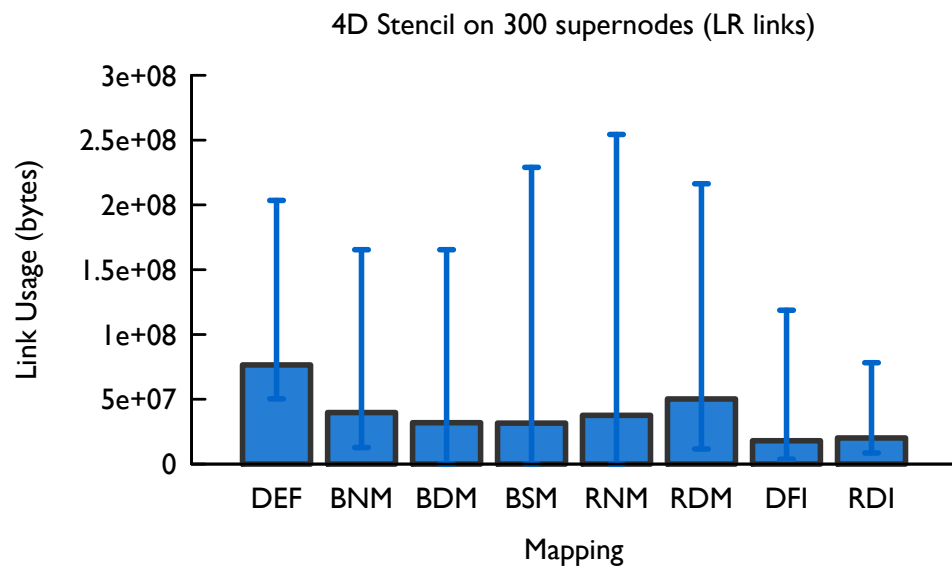
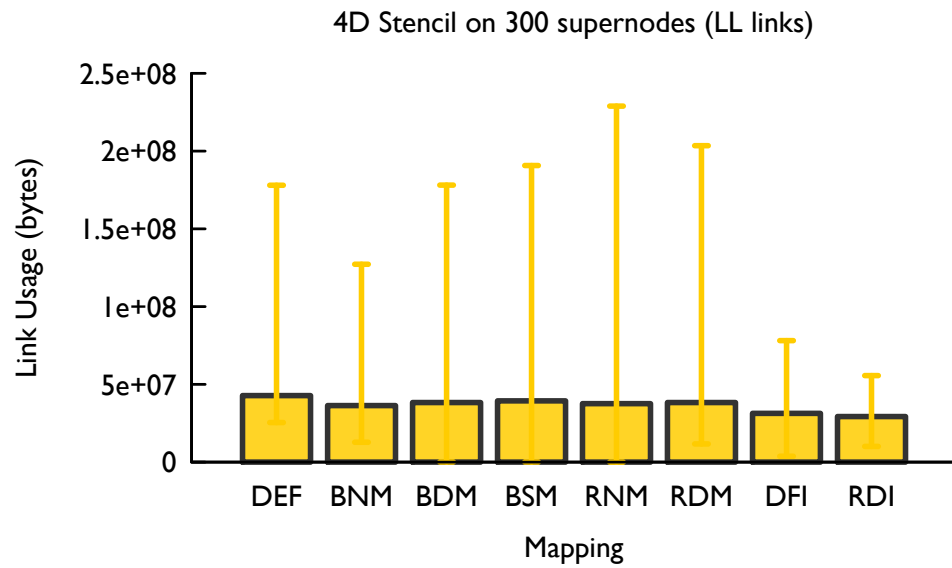
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## Text

Performance of 4D Stencil on 300 supernode



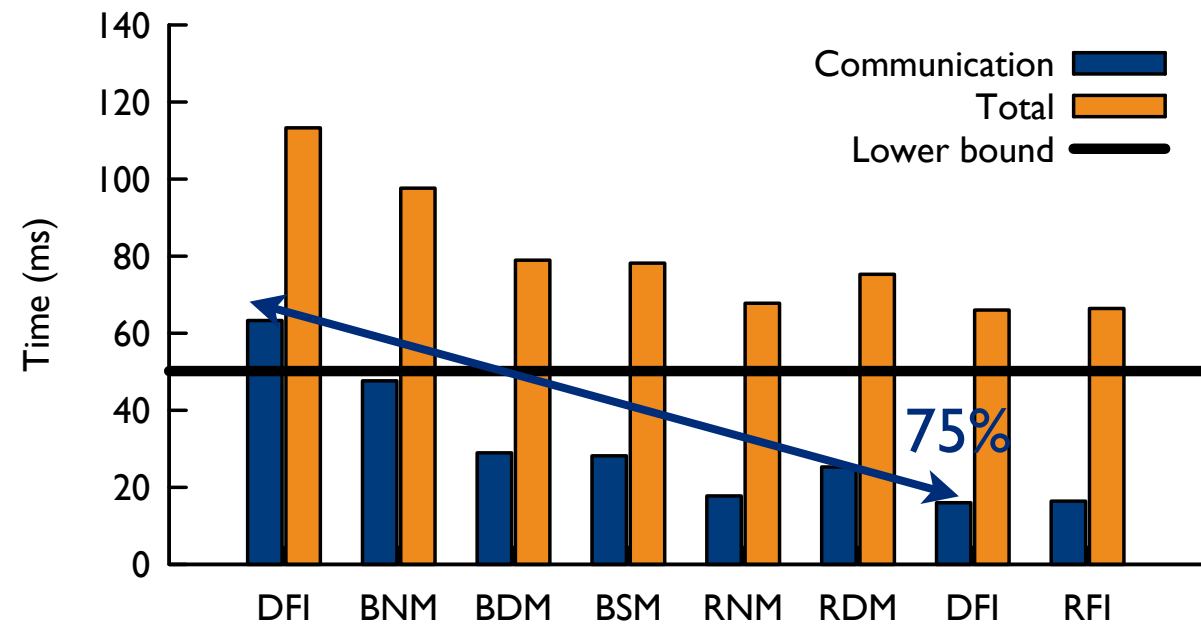
# 4D Stencil on 300 supernodes



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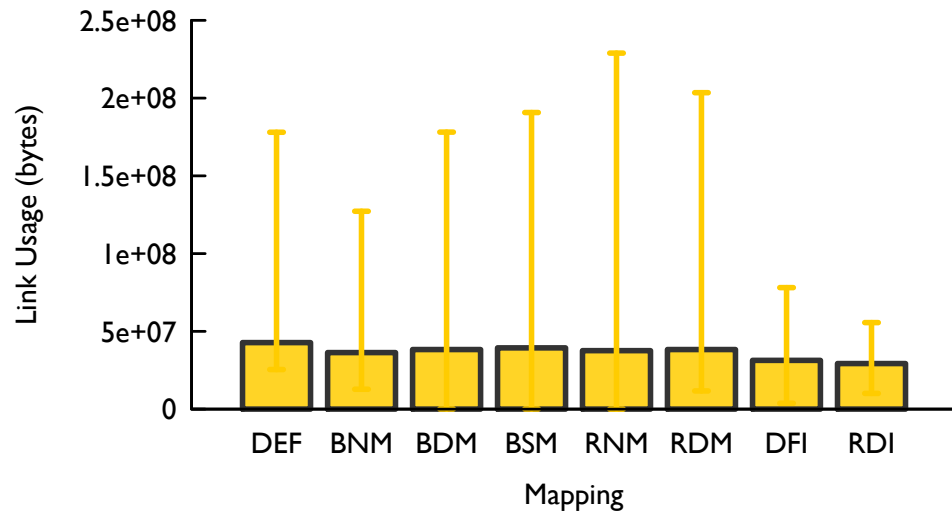
## Text

Performance of 4D Stencil on 300 supernode

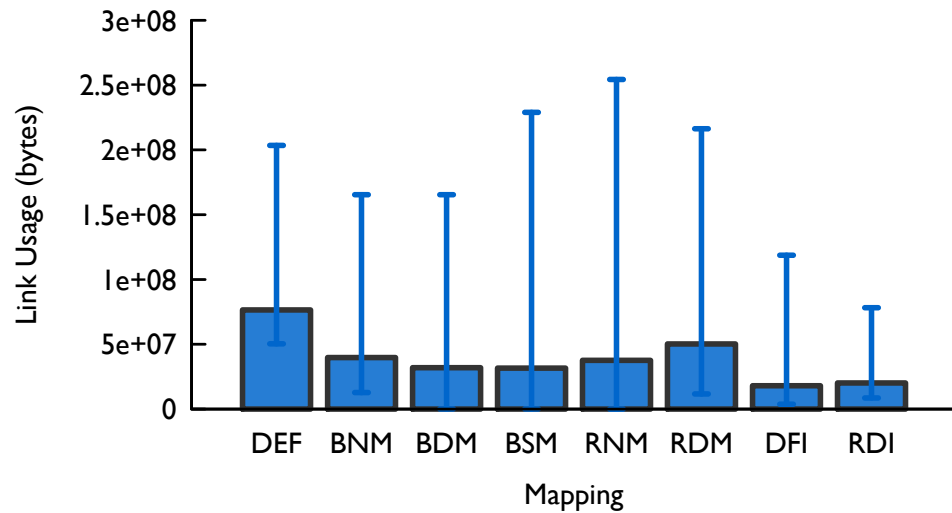


# 4D Stencil on 300 supernodes

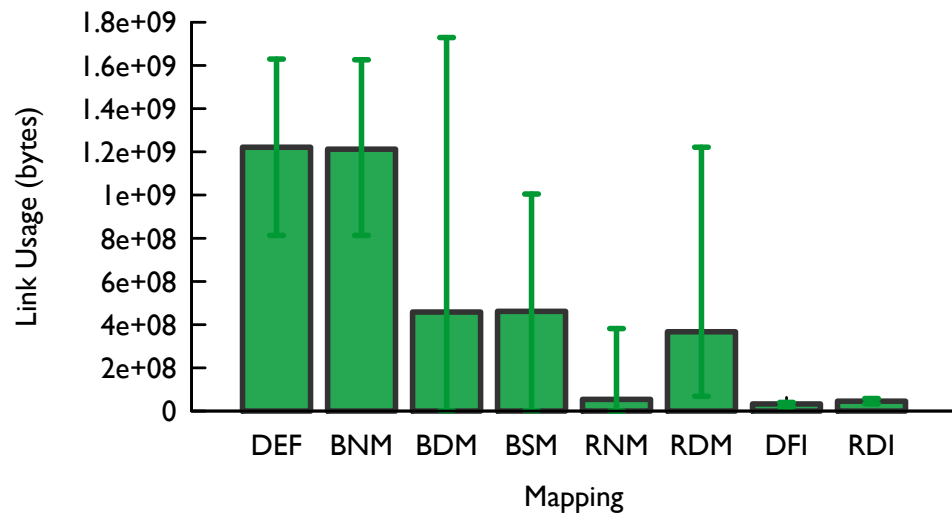
4D Stencil on 300 supernodes (LL links)



4D Stencil on 300 supernodes (LR links)



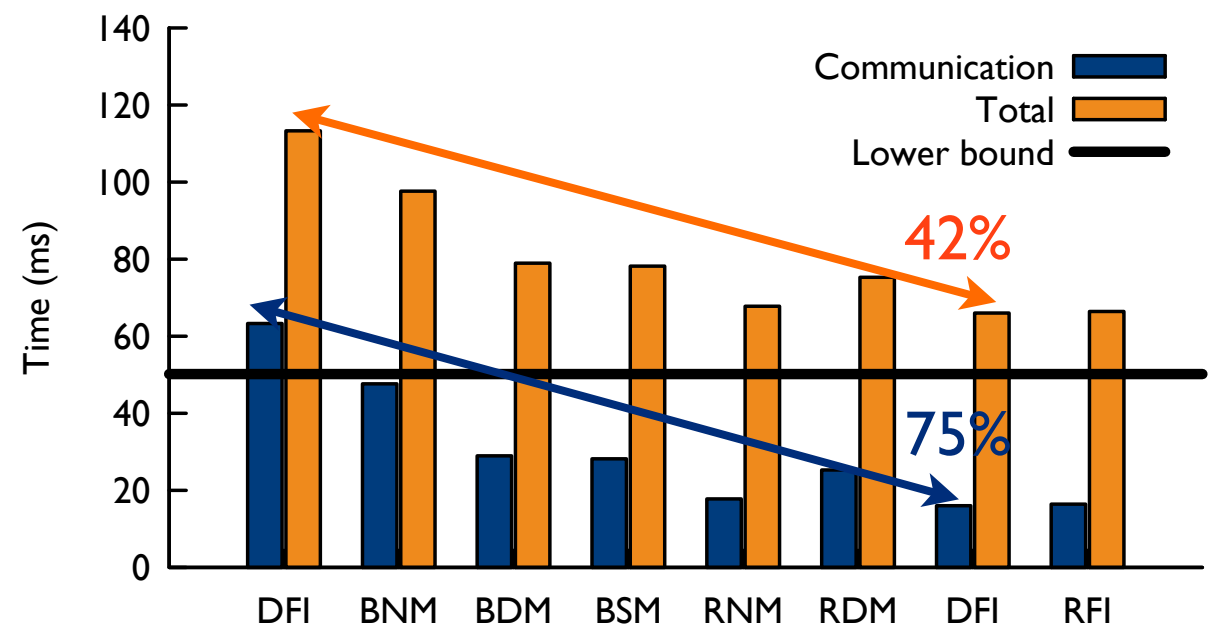
4D Stencil on 300 supernodes (D links)



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## Text

Performance of 4D Stencil on 300 supernode



# Summary

- Default MPI rank-ordered mapping on multi-level direct networks can lead to hot-spots
- Packet-level simulation to assist machine architects and application developers in making routing and mapping choices
- Conclusions:
  - With direct routing, random mapping at node granularity is best
  - With indirect routing, default mapping is good enough
- Utility of simulation-based analysis to analyze algorithms and design choices for future machines



# Questions?



More information at: <http://charm.cs.illinois.edu/research/topology>

Thanks to Ryan Mokos (PPL) for implementing the PERCS network model.  
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