Micro-RDC
Microelectronics Research Development Corporation

Radiation Hardened By Design 8 Bit RISC MicroController (KM-803301)

Feature Sheet

RHBD 8 Bit RISC CPU Features:

8-Bit RISC CPU

- 50 MHz Clock
- Based on Micro-RDC Enhanced Open Cores PIC
- Supports 2x96x8 Byte Register Files
- 8 bit GPIO
- Watch Dog Timer
- External Interrupt

Memory Sub Systems

- On Chip Internal Register File (2x96x8)
- Temporal Latch based Flip Flops
- On Chip 4Kx14bit EDAC Program RAM
- Bootup from External SPI EEPROM
- On Chip ROM for Testing and Bootup
- SPI Slave for Firmware Download and Upload to Silicon
- Support for 128 Kbytes External SPI Non Volatile Memory

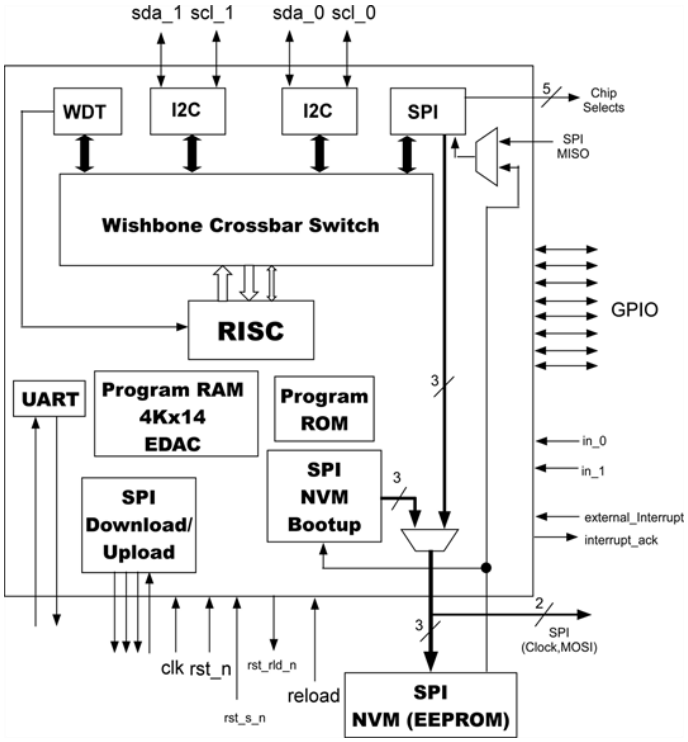
Communications

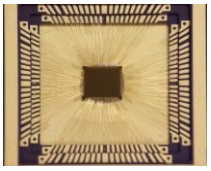
- Dual I2C Bus
- I2C Master/Slave
- I2C Master
- SPI Master with Multiple Slave Chip Enables

Peripherals

- I2C Primary Master
- I2C Secondary Master
- I2C Slave
- SPI Master with 8 Slave Selects
- SPI Slave

KM-803301 Block Diagram





KM-803301
172 pin CQFP (Evaluation)

IBM 90nm Low Power Process, using Micro-RDC Radiation-Hardened-By-Design (RHBD) Technology:

- Radiation Hardness (MIL-STD 883)
  - TID>1 Mrad(Si)
  - SEL immune > 75 MeV-cm2/mg (LET)
  - SRAM Error Rate: Supports scrubbing program SRAM to obtain < 1e-10 Errors/bit-day
  - Patented Temporal Latch: Provides SET immunity to pulse widths up to 1ns
- Operating range – Voltages: 1.2V to 3.3V IO; 1.2V Core; Temperature: -55ºC to +125ºC
- Clock: 10 MHz to 50 MHz
- Power consumption: 30 mW @ 50 MHz
- Development/Evaluation Kit including:
  - Development/Evaluation Board
  - Evaluation Sample

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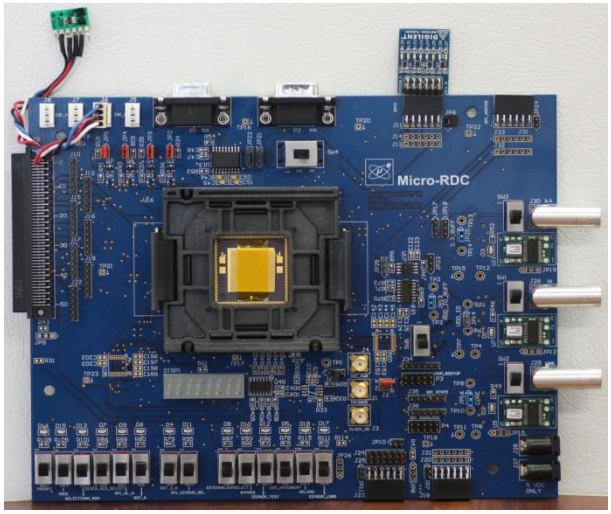
Radiation Hardened By Design 8 Bit RISC MicroController Development Support

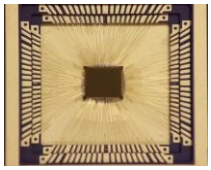
Development/Evaluation Kit and Development Support

RHBD KM-803301 CPU Development Support:

DEVELOPMENT / EVALUATION KIT:



KM-803301 CPU Development/Evaluation Board



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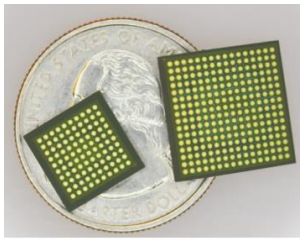

16x16 0.8 mm Pitch BGA

SOFTWARE/DEPLOYMENT SUPPORT:

- Full Support for CCS C and Assembly Firmware Development
- Firmware Download to Silicon via USB/SPI Interface
- Support to Program EEPROM from Intel Checksum HEX Files
- Support Writing XTEDS to EEPROM

EVALUATION BOARD FPGA 50MHz CLOCK DEVELOPMENT SUPPORT:

- Xilinx Spartan 3E 1200, Running at 50 MHz
- Support for Digilent Nexys2™ and Genesys™ Virtex-5 Development Boards
- Modules (PMOD™): SpaceWire LVDS, Dual I²C Bus Support, 1 Mbit NVM Bootup/XTEDS, RS-422 Tx and Rx

RECOMMENDED 8051XC APPLICATIONS:

- Space Avionics Plug and Play (SPA), SPA-S, SPA-U, SPA-1
- Spaceborne Sensor Networks
- Spaceborne 50 MHz SOC

For More Information Please Contact:

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