



Personal System/2
Model 55
Technical Reference

Second Edition (October 1990)

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Preface

This technical reference contains hardware and software interface information specific to the IBM Personal System/2 Model 55 computer. It is intended for those who develop hardware and software products for these systems. Users should understand computer architecture and programming concepts.

This publication consists of the following sections:

Section 1, "System Overview," describes the system, features and specifications.

Section 2, "Programmable Option Select," describes registers used for configuration.

Section 3, "System Board," describes the system specific hardware implementations.

This technical reference should be used with the following publications:

*IBM Personal System/2 Hardware Interface Technical Reference
– Architectures*

*IBM Personal System/2 Hardware Interface Technical Reference
– Common Interfaces*

*IBM Personal System/2 and Personal Computer BIOS Interface
Technical Reference*

These publications contain additional information on many of the subjects discussed in this technical reference.

Warning: The term "Reserved" describes certain signals, bits, and registers that should not be changed. Use of reserved areas can cause compatibility problems, loss of data, or permanent damage to the hardware. When the contents of a register are changed, the state of the reserved bits must be preserved. When possible, read the register first and change only the bits that must be changed.

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Section 1. System Overview

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Notes:

Description

The IBM Personal System/2 Model 55 is a desktop computer that features the Micro Channel architecture. It comes with a keyboard, and can support one internal diskette drive and one internal fixed disk drive.

The system can have either a Type 1 and Type 2 system board. The Type 2 system board contains additional memory for configuration information.

Programs can identify the system board by reading the model and submodel bytes. Interrupt hex 15, function code (AH)=hex C0, returns the model byte, submodel byte, and BIOS revision code. The following table lists the model and submodel bytes, the system board types, and the system clock speed for the two Model 55 system boards.

Model Byte	Submodel Bytes	System Clock	System Board Type
F8	0C	16 MHz	Type 1
F8	1E	16 MHz	Type 2

Figure 1-1. Model and Submodel Bytes

Refer to the *IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference* and its supplements for a listing of other systems.

System Board Features

The following figure lists the system board devices and features. The *IBM Personal System/2 Hardware Interface Technical Reference* manuals describe devices common to PS/2 products by type number.

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Device	Type	Features
Microprocessor	---	80386SX** 24-bit address and 16-bit data interface
System Timers	1	Channel 0 – System timer Channel 2 – Tone generation for speaker Channel 3 – Watchdog timer
ROM Subsystem	---	128KB (KB = 1024 bytes)
RAM Subsystem	---	1 to 8MB (MB = 1,048,576 bytes) Expandable on the channel to 16MB
CMOS RAM Subsystem	---	64-byte CMOS RAM with real-time clock, calendar, and battery Type 2 system board also has a 2KB CMOS RAM extension with battery
Video Subsystem	1	Auxiliary connector on the channel Analog output 256KB video memory
Audio Subsystem	1	Driven by: - System-timer channel 2 - The 'audio sum node' signal.
DMA Controller	1	Eight independent DMA channels Single or burst transfers and read verification
Interrupt Controller	1	16 levels of system interrupts Interrupts are level-sensitive
Keyboard/Auxiliary Device Controller	1	Keyboard connector Auxiliary device connector Password security
Diskette Drive Controller	1	Supports: - 1.44MB formatted diskette density - 720KB formatted diskette density.
Serial Controller	2	RS-232C interface Programmable as serial port 1 or 2 FIFO mode* and character mode
Parallel Controller	1	Programmable as parallel port 1, 2, or 3 Supports bidirectional input and output
Micro Channel Bus Adapter	---	Four channel connectors for Type 3 adapters: - One 16-bit connector with an auxiliary video extension - Two 16-bit connectors - One 2- by 36-pin card edge connector for the fixed disk drive.
Math Coprocessor Socket	---	Supports 80387SX** math coprocessor option Same clock speed as the system microprocessor

* The Model 55 supports FIFO through BIOS calls only.

Figure 1-2. System Board Devices and Features

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System Board I/O Address Map

Address (Hex)	Device
0000 - 001F	DMA Controller (0-3)
0020, 0021	Interrupt Controller (Master)
0040, 0042 - 0044, 0047	System Timers
0060	Keyboard, Auxiliary Device
0061	System Control Port B
0064	Keyboard, Auxiliary Device
0070, 0071	RT/CMOS and NMI Mask
0081 - 0083, 0087	DMA Page Registers (0-3)
0089 - 008B, 008F	DMA Page Registers (4-7)
0090	Central Arbitration Control Point
0091	Card Selected Feedback Register
0092	System Control Port A
0094	System Board Enable/Setup Register
0096	Adapter Enable/Setup Register
00A0, 00A1	Interrupt Controller (Slave)
00C0 - 00DF	DMA Controller (4-7)
00E0, 00E1	Reserved
00F0 - 00FF	Math Coprocessor
0100 - 0107	Programmable Option Select
01F0 - 01F8	Fixed Disk Drive Controller
0278 - 027B	Parallel Port 3
02F8 - 02FF	Serial Port 2 (RS-232C)
0378 - 037B	Parallel Port 2
03B4, 03B5, 03BA	Video Subsystem
03BC - 03BF	Parallel Port 1
03C0 - 03C5	Video Subsystem
03C6 - 03C9	Video DAC
03CA, 03CC, 03CE, 03CF	Video Subsystem
03D4, 03D5, 03DA	Video Subsystem
03F0 - 03F7	Diskette Drive Controller
03F8 - 03FF	Serial Port 1 (RS-232C)

Figure 1-3. System Board I/O Address Map

Specifications

Device	Number of Waits	Cycle Time (ns)
Microprocessor (16 MHz – 62.5 ns Clock)		
Access to System Board RAM: *		
Memory Read (Page Hit)	0	125
Memory Read (Anticipated Page Miss)	1	187.5
Memory Read (Page Miss)	2	250
Memory Write (Page Hit)	1	187.5
Memory Write (Anticipated Page Miss)	1	187.5
Memory Write (Page Miss)	2	250
Access to Channel:		
Default Transfer Cycle	2	250
Synchronous Transfer Cycle	4	375
Access to ROM	3	312
Refresh Rate (typically performed every 15.1 μ s)		625 (min)
Bus Master Access to System Board RAM		300 (min)
DMA Controller (8 MHz – 125 ns Clock):		
Single Transfer: 375 + (I/O Access + Memory Access)		
Burst Transfer: 375 + (I/O Access + Memory Access)N **		
System Board Memory Access		375
Default Transfer Cycle		250
Synchronous Transfer Cycle		375
* Adapters installed in the channel should not rely on monitoring system board memory access, because channel memory control signals may not be present during these accesses.		
** N is the number of transfers in the burst.		
Note: The cycle times shown for access to system board RAM is based on 85- or 100-nanosecond memory.		

Figure 1-4. Performance Specifications

The following figure describes the physical specifications of the system.

Size	
Width	406 mm (16.0 in.)
Depth	397 mm (15.6 in.)
Height	102 mm (4.0 in.)
Weight with DASD	8.64 kg (19 lb)
Cables:	
Power Cable	1.8 m (6 ft)
Keyboard Cable	1.8 m (6 ft)
Air Temperature:	
System On	15.6 to 32.2°C (60 to 90°F)
System Off	10.0 to 43.0°C (50 to 110°F)
Humidity:	
System On	8% to 80%
System Off	8% to 80%
Maximum Altitude	2133.6 m (7000 ft)
Heat Output	140 Watts(480 BTUs/hour)
Acoustical Readings	See Figure 1-6 on page 1-8
Electrical:	
Input Voltage (Range is switch selected; sinewave input is required)	
Low Range	90 (min) – 137 (max) Vac
High Range	180 (min) – 265 (max) Vac
Frequency	50 ± 3Hz/60 ± 3Hz
Input in Kilovolt-Ampere (kVA):	
Minimum Configuration (as shipped by IBM)	0.08 kVa
Maximum Configuration	0.24 kVa
Electromagnetic Compatibility	FCC Class B

Figure 1-5. Physical Specifications

Description	L _{WAd} in bels		L _{pAm} in dB		<L _{pA} > _m in dB	
	Operate	Idle	Operate	Idle	Operate	Idle
Model 55	5.0	4.7	43	43	40	40
Notes:						
L _{WAd}	is the declared sound power level for the random sample of machines.					
L _{pAm}	is the mean value of the A-weighted sound pressure levels at the operator position (if any) for the random sample of machines.					
<L _{pA} > _m	is the mean value of the A-weighted sound pressure levels at the one-meter positions for the random sample of machines.					
All measurements made in accordance with ANSI S12.10, and reported in conformance with ISO DIS 9296.						
The measurements are preliminary data and subject to change.						

Figure 1-6. Acoustical Readings

Power Supply

The power supply converts the ac input voltage to three dc outputs and provides power for the following:

- System board
- Channel adapters
- Internal DASD drives
- Auxiliary device
- Keyboard.

Outputs

The power supply provides separate voltage sources for the system board and the drives. The system-board voltages are +5 Vdc, +12 Vdc, and -12 Vdc. The drive voltages are +5 Vdc and +12 Vdc. The following is a list of the approximate power provided for system components.

System Component	Maximum Current	
	+12 Vdc	+5 Vdc
Internal Fixed Disk Drive (per power supply connector)	0.8 A	0.8 A
Auxiliary Device	None	300 mA
Keyboard	None	275 mA

Figure 1-7. Component Maximum Current

The following are the load currents allowed for each channel connector.

Supply Voltage	Maximum Current
+ 5.0 Vdc	1.6 A
+12.0 Vdc	0.175 A
-12.0 Vdc	0.040 A

Figure 1-8. Channel Load Current

The formulas used to determine the power requirements and the voltage regulation tolerances are in the Micro Channel adapter design information in the *Hardware Interface Technical Reference - Architectures* manual.

| Output Protection

| A short circuit placed on any dc output (between outputs or between an output and dc return) latches all dc outputs into a shutdown state with no damage to the power supply.

| If an overvoltage fault occurs (internal to the power supply), the power supply latches all dc outputs into a shutdown state before any output exceeds 130% of its nominal value.

| If either of these shutdown states is actuated, the power supply returns to normal operation only after the fault has been removed and the power switch has been turned off for at least ten seconds.

| Voltage Sequencing

| At power-on time, the output voltages track within 50 milliseconds of each other when measured at the 50% points.

Section 2. Programmable Option Select

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Notes:

Description

Programmable Option Select (POS) eliminates the need for switches by replacing their function with programmable registers. This section describes the POS information used on the Model 55 system board. For additional POS information, refer to the *IBM Personal System/2 Hardware Interface Technical Reference*.

Warning:

- IBM recommends that programmable options be set only through the System Configuration utilities. Directly setting the POS registers or CMOS RAM POS parameters can result in multiple assignments of the same system resource, improper operation of the feature, loss of data, or damage to the hardware.
- Application programs should not use the adapter identification (ID) unless absolutely necessary. Compatibility problems can result.
- If an adapter and the system board are in setup mode at the same time, bus contention occurs, no useful programming can take place, and damage to the hardware can occur.
- After setup operations are complete, the Adapter Enable/Setup register (hex 0096) should be set to hex 00, and the System Board Enable/Setup register (hex 0094) should be set to hex FF.
- The channel reset bit (bit 7) in the Adapter Enable/Setup register (hex 0096) must be 0 to program the adapters.
- The system board does not support 16-bit I/O operations to 8-bit POS registers. Using 16-bit I/O instructions on 8-bit POS registers causes incorrect data to be written to or read from the registers. Only 8-bit transfers are supported for setup operations.

Setup functions respond to I/O addresses hex 0100 through 0107 only when their unique setup signal is active. The following precautions must be taken before setting individual bits in the POS registers.

System Board Video Subsystem Setup:

- Bit 5 in the System Board Enable/Setup register (hex 0094) must be set to 0 to place the system board video into the setup mode.
- Bit 3 in the Adapter Enable/Setup register (hex 0096) must be set to 0 to avoid driving a 'setup' signal to an adapter.
- Bit 7 in the System Board Enable/Setup register must be set to 1 to avoid driving a 'setup' signal to other system board functions.

Adapter Setup:

- Bit 3 in the Adapter Enable/Setup register must be set to 1 to allow adapter setup.
- Bit 5 in the System Board Enable/Setup register must be set to 1 to avoid driving a 'setup' signal to the video subsystem.
- Bit 7 in the System Board Enable/Setup register must be set to 1 to avoid driving a 'setup' signal to a system board function.

Other System Board Setup:

- Bit 7 in the System Board Enable/Setup register must be set to 0 to allow setup of other system board functions.
- Bit 3 in the Adapter Enable/Setup register must be set to 0 to avoid driving a 'setup' signal to an adapter.
- Bit 5 in the System Board Enable/Setup register must be set to 1 to avoid driving a 'setup' signal to the video subsystem.

System Board POS Address Map

The following figure shows the organization of the I/O address space used by system board POS.

Address (Hex)	Function
0094	System Board Enable/Setup Register
0096	Adapter Enable/Setup Register
0100	POS Register 0—Reserved
0101	POS Register 1—Reserved
0102	POS Register 2—System Board I/O Register
0103	POS Register 3—Memory Enable Register
0104	POS Register 4—Memory Presence Register
0105	POS Register 5—Memory Control Register
0106	POS Register 6—Reserved
0107	POS Register 7—Reserved

Figure 2-1. System Board POS I/O Address Map

Card Selected Feedback

Whenever an adapter is addressed, it responds by setting the '-card selected feedback' (-CD SFDBK) signal to active. -CD SFDBK is derived from the address decode, driven by a totem-pole driver, and latched by the system board. It can be read through the Card Selected Feedback register at address hex 0091. Diagnostic and automatic configuration programs can use this signal to verify the operation of an adapter at a given address or DMA port. This signal must not be active during a setup cycle.

The Card Selected Feedback register is a read-only register at address hex 0091. It allows programs to monitor -CD SFDBK and determine if the video subsystem, system board I/O, or an adapter is addressed and functioning.

Bit	Function
7 - 1	Reserved
0	Card Selected Feedback

Figure 2-2. Card Selected Feedback Register (Hex 0091)

Bits 7 - 1 Reserved.

Bit 0 This bit is set to 1 whenever -CD SFDBK was active on a previous cycle or whenever the system board I/O functions (diskette drive, serial, or parallel interfaces) are accessed by an I/O cycle. Reading this register resets the bit to 0.

System Board Setup

The integrated I/O functions on the system board use POS information during setup. The diskette drive controller, serial port, and parallel port are treated as a single device. The video subsystem also is an integrated part of the system board, but POS treats it as a separate device. The System Board Enable/Setup register is used to place the system board or the video subsystem in the setup mode.

System Board Enable/Setup Register (Hex 0094)

This is a read/write register. All bits in this register default to 1 (enabled).

Bit	Function
7	Enable/-Setup System Board Functions
6	Reserved
5	Enable/-Setup Video Subsystem
4 - 0	Reserved

Figure 2-3. System Board Enable/Setup Register (Hex 0094)

Bit 7 When set to 0, this bit places various system board I/O functions in the setup mode. The diskette drive controller, serial port, and parallel port are controlled through System Board POS Register 2 (hex 0102). The POS information for memory is in System Board POS Register 3 (hex 0103), POS Register 4 (hex 0104), and POS Register 5 (hex 0105).

When set to 1, this bit enables the system board functions.

Bit 6 Reserved.

Bit 5 When this bit is set to 0, the video subsystem is placed in the setup mode and controlled through POS Register 2 (hex 0102). When this bit is set to 1 and bit 0 in POS Register 2 is set to 1, video is enabled.

Bit 0 of POS Register 2 is the video enable bit. When this bit is set to 0, the video subsystem does not respond to commands, addresses, or data. If video is being generated when the video enable bit is set to 0, the output is still generated. For information on BIOS calls to enable or disable the video, see the *IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference*.

Note: When video is disabled, access to the digital-to-analog converter (DAC) registers is disabled.

Bits 4 - 0 Reserved.

System Board POS Register 2 (Hex 0102)

When the system board is in the setup mode, this read/write register controls the diskette drive controller, serial port, and parallel port. Reading this register returns the current state of the following system board functions.

Bit	Function
7	Disable Parallel Port Extended Mode
6, 5	Parallel Port Select
4	Enable Parallel Port
3	Serial Port Select
2	Enable Serial Port
1	Enable Diskette Drive Interface
0	Enable System Board

Figure 2-4. System Board POS Register 2 (Hex 0102)

Bit 7 When set to 0, this bit allows the parallel port to be configured as an 8-bit, parallel, bidirectional interface. When set to 1, this bit disables the bidirectional mode. This bit is set to 0 at power-on time, and the power-on self-test (POST) sets it to 1.

Bits 6, 5 These bits select the configuration of the system board parallel port.

Bits	Assignment	Address (Hex)	Interrupt Level
00	Parallel 1	03BC - 03BF	7
01	Parallel 2	0378 - 037B	7
10	Parallel 3	0278 - 027B	7
11	Reserved	-----	-

Figure 2-5. Parallel Port Select Bits

Bit 4 When this bit and bit 0 are set to 1, the system board parallel port is enabled.

Bit 3 When set to 1, this bit sets the system board serial port as Serial 1 (addresses hex 03F8 through 03FF), which uses interrupt level 4. When set to 0, this bit sets the serial port as Serial 2 (addresses hex 02F8 through 02FF), which uses interrupt level 3.

- Bit 2** When this bit and bit 0 are set to 1, the system board serial port is enabled.
- Bit 1** When this bit and bit 0 are set to 1, the diskette drive interface is enabled.
- Bit 0** When set to 1, this bit allows bits 4, 2, and 1 to enable and disable their respective devices. When set to 0, this bit disables the system board parallel port, the system board serial port, and the diskette drive interface, regardless of the state of bits 4, 2, and 1.

System Board POS Register 3 (Hex 0103)

When the system board is in setup mode, this read/write register controls the system board memory.

Bit	Function
7 - 1	Reserved
0	Enable System Board RAM

Figure 2-6. System Board POS Register 3 (Hex 0103)

- Bits 7 - 1** Reserved
- Bit 0** When set to 1, this bit enables system board memory. When set to 0, this bit disables system board memory. All RAM installed on the system board is enabled or disabled by this operation.

System Board POS Register 4 (Hex 0104)

The system board has two memory connectors that support 1MB, 2MB, and 4MB memory cards. This read/write register contains information about the memory cards installed. POS Register 5 defines the connector.

Bit	Function
7 - 4	Memory Card ID
3 - 0	Enable Memory Card

Figure 2-7. System Board POS Register 4 (Hex 0104)

Bits 7 - 4 Bits 7 through 4 provide the memory card ID.

Bits 7 6 5 4	Size	Speed
0 0 0 0	4MB	80 ns ✓
0 0 0 1	2MB	100 ns ✓
0 0 1 0	1MB	100 ns ✓
0 0 1 1 - 0 1 0 0	Reserved	--
0 1 0 1	2MB	85 ns ✓
0 1 1 0	1MB	85 ns ✓
0 1 1 1 - 1 1 1 0	Reserved	--
1 1 1 1	No memory card installed	--

*Emer corrected
0 0 1 1 1 0
65 ns X*

Figure 2-8. Memory Card ID Bits

4MB Memory Cards

Bits 3 - 0 When set to 1, a 4MB memory card is enabled

1MB and 2MB Memory Cards

Bits 3, 2 Reserved

Bit 1 When set to 1, this bit enables the second 1MB on a 2MB memory card.

Bit 0 When set to 1, this bit enables a 1MB memory card or the first 1MB on a 2MB memory card.

System Board POS Register 5 (Hex 0105)

This is the memory control register.

Bit	Function
7, 6	Reserved
5	640KB - 1MB Split Enable
4	ROM Enable
3	Reserved = 1
2 - 0	Memory Connector Select for POS Register 4

Figure 2-9. System Board POS Register 5 (Hex 0105)

Bits 7, 6 Reserved.

Bit 5 When this bit is set to 0, system board RAM between 640KB and 1MB is enabled. Typically, 128KB of this memory is mapped to the system board ROM address space, and the remaining 256KB is mapped to the first available address following the last full 1MB block of

activated system board memory. When set to 1, this bit disables system board RAM between 640KB and 1MB.

Bit 4 This bit determines how addresses hex 0E0000 to 0FFFFF are assigned.

When this bit is set to 1, ROM is enabled; the read-access addresses are assigned to ROM and the write-access addresses are disabled. When this bit is set to 0, ROM is disabled; the read-access addresses are assigned to RAM and the write-access addresses are disabled. Bit 5 of this register must be set to 0 before ROM can be disabled.

Bit 3 This bit is reserved.

Bits 2 - 0 These bits select the memory connector to be used by POS Register 4.

Bits 2 1 0	Function
0 0 0	Memory Connector 1
0 0 1	Memory Connector 2
0 1 0 - 1 1 1	Reserved

Figure 2-10. Memory Connector Select for POS Register 4

Adapter Setup

The Adapter Enable/Setup register (hex 0096) selects the channel connector to be configured.

Bit	Function
7	Channel Reset
6 - 4	Reserved
3	Card Setup Enable
2 - 0	Channel Select 2 - 0

Figure 2-11. Adapter Enable/Setup Register (Hex 0096)

Bit 7 When set to 1, this bit activates the 'channel reset' signal to all connectors.

Bits 6 - 4 Reserved.

Bit 3 When set to 1, this bit enables the '-card setup' (-CD SETUP) signal selected by bits 2 through 0.

Bits 2 - 0 These bits are the address bits for -CD SETUP. Connectors 1 through 3 of the bus adapter are addressed as 0 through 2, respectively, and the fixed disk drive connector is addressed as 3. When bit 3 is set to 1, these bits select the connector that is put into setup.

Associated with each channel connector is a unique '-card setup' signal used to put the adapters in the setup mode, which allows access to the POS registers. The individual connectors are selected through the Adapter Enable/Setup register. Setup information is then read from or written to the selected adapter through I/O addresses hex 0100 through 0107.

Notes:

1. -CD SETUP goes active only when an operation is performed in the I/O address range hex 0100 through 0107.
2. The status of the Adapter Enable/Setup register (hex 0096) can be read by a program. However, when the register is read, bits 6 through 4 are set to 1.

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Description

This section describes the microprocessor, math coprocessor, channel differences, memory subsystems, and miscellaneous system ports and connectors for the Model 55. Additional information on these topics can be found in the *Hardware Interface Technical Reference* listed in the preface of this manual.

Microprocessor and Math Coprocessor

The 80386SX microprocessor used in the Model 55 runs at 16MHz and has a 24-bit address and a 16-bit data interface. The 80386SX microprocessor is software-compatible with the 80386 microprocessor.

The 80387SX math coprocessor is matched to the speed of the system microprocessor and operates in the synchronous mode. The 80387SX math coprocessor is software-compatible with the 80387 math coprocessor.

Micro Channel Implementation

This section describes the implementation of the Micro Channel architecture on Model 55 systems. For general Micro Channel architecture information, refer to the *Hardware Interface Technical Reference*.

Exception Reporting

Exceptions should be reported using the asynchronous channel check procedure. The synchronous channel check procedure is not supported.

Central Arbiter

The central arbitration control point gives intelligent subsystems on the channel the ability to share and control the system. It allows burst data transfers and prioritization of control between devices. The central arbiter supports up to 15 arbitrating devices (levels 0 through E) and the system microprocessor (level F).

Arbitration Bus Priority Assignments

The following figure shows the assignment of arbitration levels. The functions with the lowest arbitration level have the highest priority.

ARB Level	Primary Assignment
-2	Memory Refresh
-1	NMI
0	DMA Channel 0 (Programmable to any arbitration level)
1	DMA Channel 1
2	DMA Channel 2
3	DMA Channel 3
4	DMA Channel 4 (Programmable to any arbitration level)
5	DMA Channel 5
6	DMA Channel 6
7	DMA Channel 7
8 - E	Available
F	System Microprocessor

Figure 3-1. Arbitration Bus Priority Assignments

Note: Devices designed for arbitration level 0 or 1 should have limited bandwidth or short bursts so diskette overruns can be prevented or recovered by retry operations. The diskette drive controller, on arbitration level 2, can be held inactive by devices on levels 0 and 1, by a refresh operation, and by the previous controlling master. The diskette drive controller should not be held inactive for more than 12 microseconds to prevent overrun.

Nonmaskable interrupt (NMI) service is executed at a priority level higher than 0, called -1. Memory refresh is prioritized at -2, two levels higher than 0. Levels -1 and -2 are reached on the system board only, while the 'arbitrate/-grant' signal (ARB/-GNT) is in the arbitrate state.

When the central arbitration control point receives a level -1 request (NMI, a system-board internal signal), it activates -PREEMPT, waits for the end of transfer, and then places ARB/-GNT in the arbitrate state, which denies channel activity to arbitrating devices. The central arbitration control point gives the grant to the level -1 request, and holds ARB/-GNT in the arbitrate state until the operation is complete and the NMI is reset.

Central Arbiter Programming

The central arbitration control point provides access to programmable options through the Arbitration register, which is accessed at I/O address hex 0090. The bits are defined differently for read and write operations, as shown in the following figures.

Bit	Definition
7	Enable System Microprocessor Cycle
6	Arbitration Mask
5	Enable Extended Arbitration (Not Supported)
4 - 0	Reserved

Figure 3-2. Arbitration Register, Write to Hex 0090

Bit	Definition
7	Enable System Microprocessor Cycle
6	Arbitration Masked by NMI
5	Bus Time-Out
4	Reserved
3 - 0	Value of Arbitration Bus During Previous Grant State

Figure 3-3. Arbitration Register, Read Hex 0090

Bit 7 Setting this bit to 1 enables system microprocessor cycles during arbitration cycles. This bit can be set to 0 if an arbitrating device requires total control of the channel bandwidth. This bit is set to 0 by a system reset.

Reading this bit as a 1 indicates system microprocessor cycles are enabled during arbitration.

Bit 6 Setting this bit to 1 causes the central arbitration control point to enter the arbitration state. The system microprocessor controls the channel until this bit is reset to 0. This bit is set to 0 by a system reset.

Reading this bit as a 1 indicates that an NMI has occurred and has masked arbitration.

Warning: This bit should be set to 1 only by diagnostic routines and system error-recovery routines.

Bit 5 Setting this bit to 1 extends the arbitration cycle from a minimum of 400 nanoseconds to a minimum of 800 nanoseconds. The Model 55 does not support this mode of operation. Setting this bit to 1 can cause unpredictable results.

Reading this bit as a 1 indicates that a bus time-out has occurred. The bus-time-out indication is not reset until bit 6 of this register is set to 0.

Bit 4 This bit is reserved and should be 0.

Bits 3 - 0 These bits are undefined for a write operation and should be set to 0.

Reading these bits returns the arbitration level of the arbiter controlling the channel during the most recent grant state. This information allows the system microprocessor to determine the arbitration level of the device that caused a bus time-out.

Bus Adapter

The Model 55 uses a direct bus attachment board to provide four channel connectors:

- Two 16-bit Micro Channel connectors
- One 16-bit Micro Channel connector with an auxiliary video extension
- One card edge connector for the fixed disk drive.

The adapters are installed into the direct bus attachment board horizontally.

When in the setup mode, the fixed disk drive is addressed as channel connector 3 through the Adapter Enable/Setup register (hex 0096). See "Adapter Setup" on page 2-11. For more POS information about the fixed disk drive, refer to the technical reference for that drive.

The fixed disk drive connector is a 2- by 36-pin connector on the top edge of the direct bus attachment board. The following figure shows the signal assignments and pin numbering for the connector.

Pin	Side A I/O	Signal	Pin	Side B I/O	Signal
1	O	-CD SETUP	1	O	A15
2	O	A13	2	O	A14
3	N/A	Ground	3	N/A	Ground
4	O	A11	4	O	Reserved
5	O	A10	5	N/A	Ground
6	O	A09	6	O	A12
7	O	+5 Vdc	7	O	-CMD
8	O	A08	8	I	-CD SFDBK
9	O	A07	9	N/A	Ground
10	O	A06	10	I/O	D01
11	N/A	Ground	11	I/O	D03
12	O	A05	12	I/O	D04
13	O	A04	13	N/A	Ground
14	O	A03	14	O	CHRESET
15	O	+5 Vdc	15	I/O	D08
16	O	A02	16	I/O	D09
17	O	A01	17	N/A	Ground
18	O	A00	18	I/O	D12
19	O	+12 Vdc	19	I/O	D14
20	O	-ADL	20	I/O	D15
21	I	-PREEMPT	21	N/A	Ground
22	I	-BURST	22	I/O	D00
23	O	+5 Vdc	23	I/O	D02
24	I	ARB 00	24	I/O	D05
25	I	ARB 01	25	N/A	Ground
26	I	ARB 02	26	I/O	D06
27	N/A	+12 Vdc	27	I/O	D07
28	I	ARB 03	28	I/O	D10
29	O	ARB/-GNT	29	N/A	Ground
30	O	-TC	30	I/O	D11
31	N/A	+5 Vdc	31	I/O	D13
32	O	-S0	32	O	-SBHE
33	O	-S1	33	N/A	Ground
34	O	M/-IO	34	I	-CD DS 16
35	N/A	Ground	35	I	-IRQ 14
36	I	CD CHRDY	36	N/A	Ground

Figure 3-4. Fixed Disk Drive Connector

Diskette Drive Controller

The system board uses the Type 1 diskette drive controller. However, several pin assignments of the 2- by 20-pin connector are different from the ones shown in the *IBM Personal System/2 Hardware Interface Technical Reference*. The following figure shows the signal assignments and pin numbering for the connector.

Pin	I/O	Signal	Pin	I/O	Signal
1	N/A	Reserved	2	O	-High Density Select
3	N/A	+ 5 Vdc	4	N/A	Reserved
5	N/A	Ground	6	N/A	+ 12 Vdc
7	N/A	Ground	8	I	-Index
9	N/A	Ground	10	N/A	Reserved
11	N/A	Ground	12	O	-Drive Select
13	N/A	Ground	14	N/A	Reserved
15	N/A	Ground	16	O	-Motor Enable
17	N/A	Ground	18	O	-Direction
19	N/A	Ground	20	O	-Step
21	N/A	Ground	22	O	-Write Data
23	N/A	Ground	24	O	-Write Enable
25	N/A	Ground	26	I	-Track 0
27	N/A	Ground	28	I	-Write Protect
29	N/A	Ground	30	I	-Read Data
31	N/A	Ground	32	O	-Head 1 Select
33	N/A	Ground	34	I	-Diskette Change
35	N/A	Ground	36	N/A	Ground
37	N/A	Reserved	38	O	+ 5 Vdc
39	N/A	Ground	40	O	+ 12 Vdc

Figure 3-5. Diskette Drive Connector

Memory

The Model 55 uses the following types of memory:

- Read-only memory (ROM)
- Random access memory (RAM)
- RT/CMOS RAM.

ROM Subsystem

The ROM subsystem consists of 128KB. ROM is active at power-on time and is assigned the top of the first and last 1MB of address space (0E0000 to 0FFFFFF and FE0000 to FFFFFFF). After POST ensures that system memory is operating properly, the ROM code is copied to RAM at the same address space, and ROM is disabled.

ROM or RAM access at address space hex 0E0000 to 0FFFFFF is controlled by the ROM enable bit in System Board POS Register 5, hex 0105. When enabled, ROM is not parity-checked and operates with three 62.5-nanosecond wait states.

RAM Subsystem

The RAM subsystem on the system board starts at address hex 000000 of the address space. The RAM subsystem is 18 bits wide: 16 data bits and 2 parity bits. One parity bit is generated for each byte of data written. During a read operation, one parity bit is checked for each byte of data read by the device controlling the bus.

Two memory connectors are provided on the system board. Each connector can support 1MB, 2MB, or 4MB of memory.

The system enables and disables the 1MB and 2MB memory cards in 1MB blocks. Each 1MB block must start on a 1MB boundary. Because 128KB of I/O ROM, 128KB of system board ROM, and 128KB of video memory are mapped within the first 1MB of address space, the first physical 1MB of RAM cannot be mapped to contiguous addresses and is therefore split at the 640KB boundary creating a 384KB overflow. The high 128KB of the overflow is mapped to the system board ROM address space; the remaining 256KB, called the *split memory block*, is either disabled or mapped to the first available address following the last full 1MB of activated system board memory. Split-memory-block remapping and disabling are controlled by System Board POS Register 5, hex 0105.

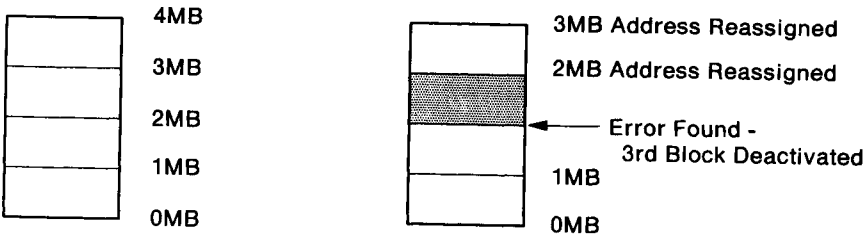
Note: The 4MB memory card cannot be enabled or disabled in 1MB blocks.

Additional memory can be added in any of the Micro Channel connectors. However, the total amount of memory installed must not exceed the 16MB addressing limit of the DMA controller. The total amount of usable memory is less than the amount of memory installed because of ROM-to-RAM remapping.

Error Recovery

If POST detects a memory error on the 1MB or 2MB memory card, an attempt is made to deactivate the physical 1MB block of memory that contains the error. The addresses assigned to the deactivated block are reassigned to the next physical block of system board memory, if installed (the first 1MB of memory address space cannot be assigned to memory installed in any of the Micro Channel connectors). If 1MB of valid system board memory cannot be found, the system sets the memory size according to the last good memory available and allows a system reset; however, if a minimum of 64KB of good memory cannot be found, POST cannot recover from the error.

Note: The 4MB memory card cannot be enabled or disabled in 1MB blocks.



Properly Functioning
Memory - 4MB Active

Error in 3rd Block of Memory -
3MB Active after Address Reassigned

Figure 3-6. Memory Error Address Reassignment

If the first physical 1MB of memory is disabled, the split-memory block and ROM-to-RAM remap feature will not be enabled.

System Memory Map

Memory is mapped by System Board POS Register 5, hex 0105.

Warning: IBM recommends that programmable options be set only through the System Configuration utilities. Directly setting the POS registers or CMOS RAM POS parameters can result in multiple assignments of the same system resource, improper operation of the feature, loss of data, or damage to the hardware.

The first 640KB of system board RAM is mapped starting at address hex 000000. A 256-byte and 1KB portion of this RAM is reserved as BIOS data areas. See the *IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference* for details.

The following figure shows the memory map for a properly functioning system. Memory can be mapped differently if POST detects an error in system board memory or RT/CMOS RAM. In the following figure, the variable X represents the number of 1MB blocks of system board memory starting at or above the hex 100000 boundary. The variable Y represents the number of 1MB blocks of addressable memory installed in the channel starting at or above the hex 100000 boundary (Y cannot exceed 14.75).

Hex Range	Function
000000 to 09FFFF	640KB System Board RAM
0A0000 to 0BFFFF	128KB Video RAM
0C0000 to 0DFFFF	Channel ROM
0E0000 to 0FFFFFFF	128K System Board ROM mapped to RAM
100000 to (100000 + XMB)	XMB System Board RAM
(100000 + XMB) to (100000 + XMB + 256KB)	256KB System Board RAM (Split Memory Block)
(100000 + XMB + 256KB) to (100000 + XMB + 256KB + YMB)	YMB Channel RAM
(100000 + XMB + 256KB + YMB) to FFFFFFFF	Not Used
FE0000 to FFFFFFFF	128KB System Board ROM (Same as 0E0000 to 0FFFFFFF)

Figure 3-7. System Memory Map

System Board Memory Connectors

The system board has two 72-pin memory connectors that support 1MB, 2MB, and 4MB memory cards. The following figure shows the pin assignments for the connectors.

Pin	I/O	Signal	Pin	I/O	Signal
1	N/A	Ground	37	I/O	Parity Data High
2	I/O	Data 0	38	I/O	Parity Data High
3	I/O	Data 0	39	N/A	Ground
4	I/O	Data 1	40	O	CAS 0
5	I/O	Data 1	41	O	CAS 2
6	I/O	Data 2	42	O	CAS 3
7	I/O	Data 2	43	O	CAS 1
8	I/O	Data 3	44	O	RAS 0
9	I/O	Data 3	45	O	RAS 1
10	O	+ 5 Vdc	46	O	Block Select 1
11	O	-CAS Parity	47	O	Write Enable
12	O	Address 0	48	N/A	Reserved
13	O	Address 1	49	I/O	Data 8
14	O	Address 2	50	I/O	Data 8
15	O	Address 3	51	I/O	Data 9
16	O	Address 4	52	I/O	Data 9
17	O	Address 5	53	I/O	Data 10
18	O	Address 6	54	I/O	Data 10
19	N/A	Reserved	55	I/O	Data 11
20	I/O	Data 4	56	I/O	Data 11
21	I/O	Data 4	57	I/O	Data 12
22	I/O	Data 5	58	I/O	Data 12
23	I/O	Data 5	59	O	+ 5 Vdc
24	I/O	Data 6	60	I/O	Data 13
25	I/O	Data 6	61	I/O	Data 13
26	I/O	Data 7	62	I/O	Data 14
27	I/O	Data 7	63	I/O	Data 14
28	O	Address 7	64	I/O	Data 15
29	O	Block Select 0	65	I/O	Data 15
30	O	+ 5 Vdc	66	O	Block Select 2
31	O	Address 8	67	I	Presence Detect 0
32	O	Address 9	68	I	Presence Detect 1
33	O	RAS 3	69	I	Presence Detect 2
34	O	RAS 2	70	I	Presence Detect 3
35	I/O	Parity Data Low	71	O	Block Select 3
36	I/O	Parity Data Low	72	N/A	Ground

RAS = Row Address Strobe
CAS = Column Address Strobe

Figure 3-8. System Board Memory Connectors

RT/CMOS RAM

The RT/CMOS RAM (real-time clock/complementary metal-oxide semiconductor RAM) chip contains the real-time clock and 64 bytes of CMOS RAM. The clock circuitry uses 14 bytes of this memory, and the rest is allocated to configuration and system status information. A battery is built into the chip to keep the RT/CMOS RAM active when the power supply is not on.

The Type 2 system board has an additional 2KB CMOS RAM extension with a built-in battery, for configuration and other system information.

The following figure shows the RT/CMOS RAM bytes and their addresses.

Address (Hex)	RT/CMOS RAM Bytes
000 - 00D	Real-Time Clock Bytes
00E	Diagnostic Status Byte
00F	Shutdown Status Byte
010	Diskette Drive Type Byte
011	Fixed Disk Drive Type Byte
012	Reserved
013	Reserved
014	Equipment Byte
015, 016	Low and High Base Memory Bytes
017, 018	Low and High Expansion Memory Bytes
019 - 031	Reserved
032, 033	Configuration CRC Bytes
034 - 036	Reserved
037	Date Century Byte
038 - 03F	Reserved

Figure 3-9. RT/CMOS RAM Address Map

RT/CMOS Address and NMI Mask Register (Hex 0070)

This register is used in conjunction with the RT/CMOS Data register (hex 0071) to read from and write to the RT/CMOS RAM bytes.

Bit	Function
7	NMI Mask
6	Reserved
5 - 0	RT/CMOS RAM Address

Figure 3-10. RT/CMOS Address and NMI Mask Register (Hex 0070)

Warning: The operation following a write to hex 0070 should access hex 0071; otherwise, intermittent malfunctions and unreliable operation of the RT/CMOS RAM can occur.

Bit 7 When this bit is set to 1, the NMI is masked off (disabled). This bit is set to 1 by a power-on reset. This is a write-only bit.

Bit 6 Reserved.

Bits 5 - 0 These bits are used to select RT/CMOS RAM addresses.

RT/CMOS Data Register (Hex 0071)

This register is used in conjunction with the RT/CMOS Address and Mask register (hex 0070) to read from and write to the RT/CMOS RAM bytes.

Bit	Function
7 - 0	RT/CMOS Data

Figure 3-11. RT/CMOS Data Register (Hex 0071)

RT/CMOS RAM I/O Operations

During I/O operations to the RT/CMOS RAM addresses, interrupts should be masked to prevent other interrupt routines from changing the RT/CMOS Address register before data is read or written. After I/O operations, the RT/CMOS Address and NMI Mask register (hex 0070) should be left pointing to Status Register D (hex 00D).

Warning: The operation following a write to hex 0070 should access hex 0071; otherwise, intermittent malfunctions and unreliable operation of the RT/CMOS RAM can occur.

Writing to the RT/CMOS RAM requires the following steps:

1. Write the RT/CMOS RAM address to the RT/CMOS Address and NMI Mask register (hex 0070).
2. Write the data to the RT/CMOS Data register (hex 0071).

Reading from the RT/CMOS RAM requires the following steps:

1. Write the RT/CMOS RAM address to the RT/CMOS and NMI Mask register (hex 0070).
2. Read the data from the RT/CMOS Data register (hex 0071).

Real-Time Clock Bytes (Hex 000-00D)

Bit definitions and addresses for the real-time clock bytes are shown in the following figure.

Address (Hex)	Function	Byte Number
000	Seconds	0
001	Second Alarm	1
002	Minutes	2
003	Minute Alarm	3
004	Hours	4
005	Hour Alarm	5
006	Day of Week	6
007	Date of Month	7
008	Month	8
009	Year	9
00A	Status Register A	10
00B	Status Register B	11
00C	Status Register C	12
00D	Status Register D	13

Figure 3-12. Real-Time Clock Bytes

Note: The Setup program initializes Status Registers A, B, C, and D when the time and date are set. Interrupt hex 1A is the BIOS interface to read and set the time and date, and it initializes the register the same way as the Setup program.

Status Register A (Hex 00A)

Bit	Function
7	Update in Progress
6 - 4	22-Stage Divider
3 - 0	Rate Selection Bits

Figure 3-13. Status Register A

- Bit 7** When set to 1, this bit indicates the time-update cycle is in progress. When set to 0, it indicates that the current date and time can be read.
- Bits 6 - 4** These bits identify which time-base frequency is being used. The system initializes these bits to binary 010, which selects a 32.768-kHz time base. This is the only value supported by the system for proper timekeeping.
- Bits 3 - 0** These bits allow the selection of a divider output frequency. The system initializes the rate selection bits to a binary 0110, which selects a 1.024-kHz square-wave output frequency and a 976.562-microsecond periodic interrupt rate.

Status Register B (Hex 00B)

Bit	Function
7	Set
6	Periodic Interrupt Enable
5	Alarm Interrupt Enable
4	Update-Ended Interrupt Enabled
3	Square Wave Enabled
2	Date Mode
1	24-Hour Mode
0	Daylight-Saving Time Enabled

Figure 3-14. Status Register B

- Bit 7** When set to 0, this bit updates the cycle, normally by advancing the counts at a rate of one per second. When set to 1, this bit immediately ends any update cycle in progress, and the program can initialize the 14 time bytes without any further updates occurring until this bit is set to 0.
- Bit 6** This bit is a read/write bit that allows an interrupt to occur at a rate specified by the rate and divider bits in Status Register A. When set to 1, this bit enables the interrupt. The system initializes this bit to 0.

- Bit 5** When set to 1, this bit enables the alarm interrupt. The system initializes this bit to 0.
- Bit 4** When set to 1, this bit enables the update-ended interrupt. The system initializes this bit to 0.
- Bit 3** When set to 1, this bit enables the square-wave frequency as set by the rate-selection bits in Status Register A. The system initializes this bit to 0.
- Bit 2** This bit indicates whether the binary-coded-decimal (BCD) or binary format is used for time-and-date calendar updates. When set to 1, this bit indicates the binary format. The system initializes this bit to 0.
- Bit 1** This bit indicates if the hours byte is in 12-hour or 24-hour mode. When set to 1, this bit indicates the 24-hour mode. The system initializes this bit to 1.
- Bit 0** When set to 1, this bit enables the daylight-saving-time mode. When set to 0, this bit disables the mode and the clock reverts to standard time. The system initializes this bit to 0.

Status Register C (Hex 00C)

Bit	Function
7	Interrupt Request Flag
6	Periodic Interrupt Flag
5	Alarm Interrupt Flag
4	Update-Ended Interrupt Flag
3 - 0	Reserved

Figure 3-15. Status Register C

Note: Interrupts are enabled by bits 6, 5, and 4 in Status Register B.

- Bit 7** When set to 1, this bit indicates that an interrupt has occurred; bits 6, 5, and 4 indicate the type of interrupt.
- Bit 6** When set to 1, this bit indicates that a periodic interrupt occurred.
- Bit 5** When set to 1, this bit indicates that an alarm interrupt occurred.
- Bit 4** When set to 1, this bit indicates that an update-ended interrupt occurred.
- Bits 3 - 0** Reserved.

Status Register D (Hex 00D)

Bit	Function
7	Valid RAM
6 - 0	Reserved

Figure 3-16. Status Register D

Bit 7 This read-only bit monitors the internal battery. When set to 1, this bit indicates that the real-time clock has power. When set to 0, it indicates that the real-time clock has lost power.

Bits 6 - 0 Reserved.

CMOS RAM Configuration

The following shows the bit definitions for the CMOS RAM configuration bytes.

Diagnostic Status Byte (Hex 00E)

Bit	Function
7	Real-Time Clock Chip Power
6	Configuration Record and Checksum Status
5	Incorrect Configuration
4	Memory Size Mismatch
3	Fixed Disk Controller/Drive C Initialization Status
2	Time Status Indicator
1	Adapter Configuration Mismatch
0	Adapter ID Time-Out

Figure 3-17. Diagnostic Status Byte

Bit 7 When set to 1, this bit indicates that the real-time clock chip lost power.

Bit 6 When set to 1, this bit indicates that the checksum is incorrect.

Bit 5 This is a power-on check of the equipment byte (hex 014). When set to 1, this bit indicates that the configuration information is incorrect.

Bit 4 When set to 1, this bit indicates that the memory size does not match the configuration information.

Bit 3 When set to 1, this bit indicates that the controller or fixed disk drive failed initialization.

- Bit 2** When set to 1, this bit indicates that the time is invalid.
- Bit 1** When set to 1, this bit indicates that the adapters do not match the configuration information.
- Bit 0** When set to 1, this bit indicates that a time-out occurred while an adapter ID was being read.

Shutdown Status Byte (Hex 00F): This byte is defined by the power-on diagnostic programs.

Diskette Drive Type Byte (Hex 010): This byte indicates the type of diskette drive installed.

Bit	Function
7 - 4	Diskette Drive Type
3 - 0	Reserved

Figure 3-18. Diskette Drive Type Byte

Bits 7 - 4 These bits indicate the diskette drive type.

Bits 7 6 5 4	Function
0 0 0 0	No drive present
0 0 1 1	High-capacity diskette drive (720KB)
0 1 0 0	High-density diskette drive (1.44MB)

Note: All combinations that are not shown are reserved.

Figure 3-19. Diskette Drive Type Bits

Bits 3 - 0 Reserved.

Fixed Disk Drive Type Byte (Hex 011): This byte defines the type of fixed disk drive installed. Hex 00 indicates that a fixed disk drive is not installed.

Note: For more information about fixed disk drive types, refer to the *IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference*.

Reserved Bytes (Hex 012, 013): These bytes are reserved.

Equipment Byte (Hex 014): This byte defines the basic equipment in the system for the power-on diagnostic tests.

Bit	Function
7, 6	Number of Diskette Drives
5, 4	Display Operating Mode
3, 2	Reserved
1	Math Coprocessor Presence
0	Diskette Drive Presence

Figure 3-20. Equipment Byte

Bits 7, 6 These bits indicate the number of diskette drives installed, as shown in the following figure.

Bits 7 6	Number of Diskette Drives
0 0	One Drive
0 1	Reserved
1 0	Reserved
1 1	Reserved

Figure 3-21. Installed Diskette Drive Bits

Bits 5, 4 These bits indicate the operating mode of the display attached to the video port, as shown in the following figure.

Bits 5 4	Display Operating Mode
0 0	Reserved
0 1	40-Column Mode
1 0	80-Column Mode
1 1	Monochrome Mode

Figure 3-22. Display Operating Mode Bits

Bits 3, 2 Reserved.

Bit 1 When set to 1, this bit indicates that a math coprocessor is installed.

Bit 0 When set to 1, this bit indicates that a diskette drive is installed.

Low and High Base Memory Bytes (Hex 015 and 016): These bytes define the amount of memory below the 640KB address space.

The value from these bytes represents the number of 1KB blocks of base memory. For example, hex 0280 is equal to 640KB. The low byte is hex 015; the high byte is hex 016.

Low and High Expansion Memory Bytes (Hex 017 and 018): These bytes define the amount of memory above the 1MB address space.

The hexadecimal values in these bytes represent the number of 1KB blocks of expansion memory. For example, hex 0800 is equal to 2048KB. The low byte is hex 017; the high byte is hex 018.

Reserved Bytes (Hex 019 through 031): These bytes are reserved.

Configuration CRC Bytes (Hex 032 and 033): These bytes contain the cyclic-redundancy-check (CRC) data for bytes hex 010 through hex 031 of the 64-byte CMOS RAM. The low byte is hex 033; the high byte is hex 032.

Reserved Bytes (Hex 034 through 036): These bytes are reserved.

Date Century Byte (Hex 037): Bits 7 through 0 of this byte contain the BCD value for the century. Refer to the *IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference* for information about reading and setting this byte.

Reserved Bytes (Hex 038 through 03F): These bytes are reserved.

Miscellaneous System Functions and Ports

Nonmaskable Interrupt

The nonmaskable interrupt (NMI) signals the system microprocessor that a parity error, a channel check, a system channel time-out, or a system watchdog time-out has occurred. The NMI stops all arbitration on the bus until bit 6 of the Arbitration register (I/O address hex 0090) is set to 0. This can result in lost data or an overrun error on some I/O devices. The NMI masks all other interrupts, and the IRET instruction restores the interrupt flag to the state it was in before the interrupt. A system reset causes a reset of the NMI.

The NMI requests from system board parity and channel check are subject to mask control with the NMI mask bit in the RT/CMOS Address register. The watchdog timer and system channel time-out are not masked by this bit. See "RT/CMOS Address and NMI Mask Register (Hex 0070)" on page 3-13. The power-on default of the NMI mask is 1 (NMI disabled). Before the NMI is enabled after a power-on reset, the parity-check and channel-check states are initialized by POST.

Warning: The operation following a write to hex 0070 should access hex 0071; otherwise, intermittent malfunctions and unreliable operation of the RT/CMOS RAM can occur.

System Control Port B (Hex 0061)

Bit definitions for the write and read functions of this port are shown in the following figures.

Bit	Function
7	Reset Timer 0 Output Latch (IRQ0)
6 - 4	Reserved
3	Enable Channel Check
2	Enable Parity Check
1	Speaker Data Enable
0	Timer 2 Gate to Speaker

Figure 3-23. System Control Port B (Write)

Bit	Function
7	Parity Check
6	Channel Check
5	Timer 2 Output
4	Toggles with Each Refresh Request
3	Enable Channel Check
2	Enable Parity Check
1	Speaker Data Enable
0	Timer 2 Gate to Speaker

Figure 3-24. System Control Port B (Read)

- Bit 7** When this bit is set to 1 during a write operation, IRQ0 is reset. When read as a 1, this bit indicates a parity check has occurred.
- Bit 6** When read as a 1, this bit indicates a channel check has occurred.
- Bit 5** When read, this bit indicates the condition of the timer/counter 2 'output' signal.
- Bit 4** When read, this bit toggles for each refresh request.
- Bit 3** When set to 0, this bit enables channel check. This bit is set to 1 during a power-on reset.
- Bit 2** When set to 0, this bit enables parity check. This bit is set to 1 during a power-on reset.
- Bit 1** When set to 1, this bit enables speaker data.
- Bit 0** When set to 1, this bit enables the timer 2 gate.

System Control Port A (Hex 0092)

Bit	Function
7 - 5	Reserved
4	Watchdog Timer Status
3	Security Lock Latch
2	Reserved = 0
1	Alternate Gate A20
0	Alternate Hot Reset

Figure 3-25. System Control Port A

Bits 7 - 5 Reserved.

Bit 4 This read-only bit indicates the watchdog timer status. When this bit is set to 1, a watchdog time-out has occurred. For more information about the watchdog timer, refer to the *IBM Personal System/2 Hardware Interface Technical Reference*.

Bit 3 This bit provides the security lock for the secured area of RT/CMOS. When this bit is set to 1, the 8-byte, power-on password is electrically locked. Once this bit is set by POST, it can be cleared only by turning the system off.

Bit 2 Reserved.

Bit 1 This bit is used to enable the 'address 20' signal (A20) when the microprocessor is in the real address mode. When this bit is set to 0, A20 cannot be used in real mode addressing. This bit is set to 0 during a system reset.

Bit 0

This bit provides an alternate method of resetting the system microprocessor. This alternate method supports operating systems requiring faster operation than was provided on the IBM Personal Computer AT*. Resetting the system microprocessor switches the microprocessor from the protected mode to the real address mode. The alternate reset takes 13.4 microseconds.

This bit is set to 0 by either a system reset or a write operation. When a write operation changes this bit from 0 to 1, the alternate reset pin is pulsed high for 100 to 125 nanoseconds. The reset occurs after a minimum delay of 6.72 microseconds. While the reset is occurring, the latch remains set so that POST can read this bit. If the bit is 0, POST assumes the system was just powered on. If the bit is 1, POST assumes a switch from the protected mode to the real mode has taken place.

When bit 0 is used to reset the system microprocessor to the real mode, the following procedure must be used.

1. Disable all maskable and non-maskable interrupts.
2. Reset the system microprocessor by writing bit 0 to 1.
3. Issue a Halt instruction to the system microprocessor.

If this procedure is not followed, the results will be unpredictable.

Note: Whenever possible, BIOS or A BIOS should be used as an interface to reset the system microprocessor to the real mode.

* Trademark of the International Business Machines Corporation.

Power-On Password

Eight bytes of RT/CMOS RAM are reserved for the power-on password and its check character. The microprocessor can access these bytes only during POST. After POST is completed, if a power-on password is installed, the password bytes are locked and cannot be accessed by a program.

Installing the password is a function of a program on the Reference Diskette. The power-on password does not appear on the screen when it is installed, changed, or removed. Once the power-on password has been installed, it can be changed only during POST.

The power-on password can be bypassed (erased) by using the following procedure:

1. Power off the system.
2. Disconnect the speaker/password security connector from the bus adapter.
3. Rotate the speaker/password security connector 180 degrees and reconnect it.
4. Power on the system.

The system unit cover can be physically locked to prevent access to the speaker/password security connector.

The Model 55 also has a keyboard password. See "Keyboard and Auxiliary Device Controller" in the *IBM Personal System/2 Hardware Interface Technical Reference* for more information.

Type 2 Serial Port Controller

Some Type 2 serial controllers used on the Model 55 system board do not respond as described in the *Hardware Interface Technical Reference*.

After the FIFO mode is enabled, bit 6 of the Interrupt Identification register is erroneously set to 0, indicating a Type 1 serial controller is installed. Any application program or operating system that uses bit 6 of the Interrupt Identification register as an indicator to determine FIFO support will default to the character mode. This indicator is ignored by the Model 55 BIOS. Therefore, programs that operate through BIOS can use the FIFO mode. The BIOS routines also clear any error indications remaining after a mode change.

Some application programs reset the received-data-ready indication by writing bit 0 of the Line Status register as a 0. This method can cause compatibility problems and is not supported by Type 1 or Type 2 serial controllers. To avoid compatibility problems, bit 0 of the Line Status register can be reset to 0 by reading the data and discarding the data if it is not used.

Hardware Compatibility

The Model 55 maintains many of the interfaces used by the IBM Personal Computer AT. In most cases command and status organization of these interfaces is maintained.

The functional interfaces for the Model 55 are compatible with the following interfaces:

- The Intel™ 8259 interrupt controllers (without edge triggering).
- The Intel 8253 timers driven from 1.193 MHz (timer 0 and 2 only).
- The Intel 8237 DMA controller-address/transfer counters, page registers and status fields only. The Command and Request registers are not supported. The rotate and mask functions are not supported. The Mode register is partially supported.
- Generally compatible with the National Semiconductor™ NS16550A serial communications controller.
- The Intel 8088, 8086, 80286, and 80386 microprocessors.
- The Intel 8272 diskette drive controller. The BIOS limits support to diskette drives that have a 3-millisecond step rate during recalibration.
- The Motorola™ MC146818 Time of Day Clock command and status (CMOS reorganized).
- The Intel 8042 keyboard port at address hex 0060.
- Display modes supported by the IBM Monochrome Display and Printer Adapter, the IBM Color/Graphics Monitor Adapter, and the IBM Enhanced Graphics Adapter.

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** Trademark of the National Semiconductor Corporation.

** Trademark of Motorola, Incorporated.

- The parallel printer ports (Parallel 1, Parallel 2, and Parallel 3) in compatibility mode.
- Generally compatible with the Intel 80387, 80287, and 8087 math coprocessors.

Whenever possible, BIOS or A BIOS should be used as an interface to reset the system microprocessor to the real mode.

The system microprocessor also can be reset to the real mode through bit 0 of port hex 0064 or hex 0092. When using either of these ports, the following procedure must be used.

1. Disable all maskable and non-maskable interrupts.
2. Reset the system microprocessor.
3. Issue a Halt instruction to the system microprocessor.

If this procedure is not followed, the results will be unpredictable.

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