Serial Port Controller

Figures

Description

The serial port controller is programmable and supports asynchronous communications. The controller automatically adds and removes start, stop, and parity bits. A programmable baud-rate generator allows operation from 50 baud to 345.6KB. The controller supports 5-, 6-, 7-, and 8-bit characters with 1, 1.5, or 2 stop bits. A prioritized interrupt system controls transmit, receive, error, line status, and data-set interrupts.

The serial port controller provides the following functions:

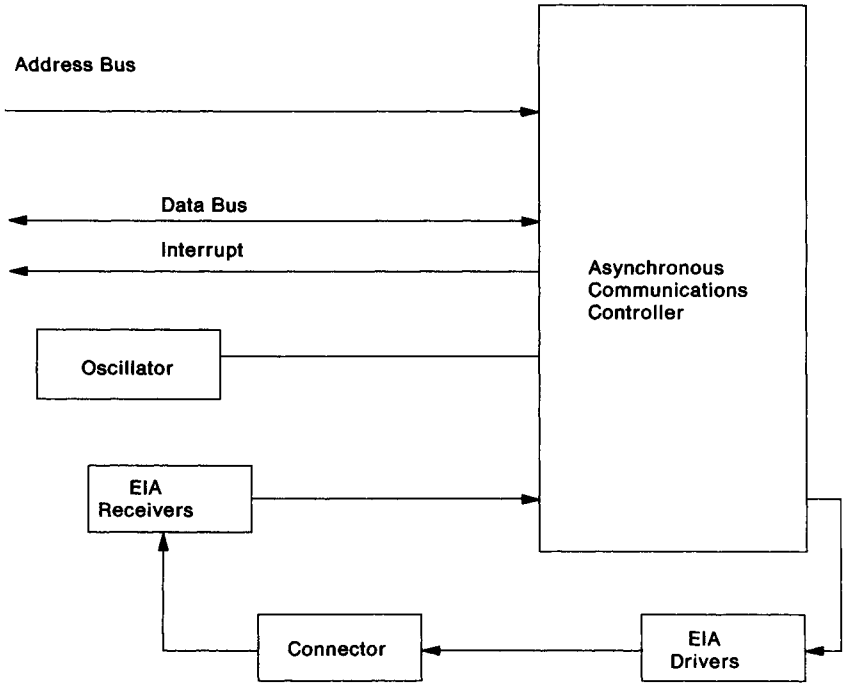
- Full double buffering in the character mode, eliminating the need for precise synchronization
- False-start bit detection
- Line-break generation and detection
- Modem control functions:
  - Clear to send (CTS)
  - Request to send (RTS)
  - Data set ready (DSR)
  - Data terminal ready (DTR)
  - Ring indicator (RI)
  - Data carrier detect (DCD).

Three types of serial port controllers have been used on the system boards. To programs, the Type 1 controller appears to be identical to the serial portion of the IBM Personal Computer AT IBM Personal Computer Serial/Parallel Adapter. The Type 2 controller incorporates all functions of the Type 1 and also provides support of the first-in-first-out (FIFO) mode. The Type 3 controller incorporates all functions of the Type 2 controller and provides the Direct Memory Access (DMA) mode.

Note: Some systems using the Type 2 controller do not support the FIFO mode. For information about individual systems refer to the system-specific technical reference manuals.

Support for the Type 1 controller is restricted to the functions that are identical to the NS16450. Using the Type 1 controller in the FIFO mode can result in nondetectable data errors. See "Registers" on page 11 for detailed FIFO information.

| The following figure is a block diagram of the serial port controller.



| *Figure 1. Serial Port Controller Block Diagram*

Communications Application

For Type 1 and Type 2 controllers the serial port can be addressed as either serial port 1 (Serial 1) or serial port 2 (Serial 2). For Type 3 controllers, the serial port can be addressed as any one of eight serial ports (Serial 1 through Serial 8). The following table illustrates the base addresses and their corresponding serial ports:

Serial Port	Compatible (Hex)	Enhanced (Hex)
Serial 1	03F8	83F8
Serial 2	02F8	82F8
Serial 3	3220	B220
Serial 4	3228	B228
Serial 5	4220	C220
Serial 6	4228	C228
Serial 7	5220	D220
Serial 8	5228	D228

Figure 2. Serial Port Register - Base Addresses

Type 1 and Type 2 controllers have only compatible registers. Type 3 controllers have both compatible and enhanced registers. In this section, serial port register addresses will contain a ***base c*** or a ***base e*** to signify the compatible or enhanced register base addresses, followed by an offset to be added to the base address to get the effective address of the register. The register assignments are controlled by Programmable Option Select (POS) and are made during system board setup.

Two interrupt lines are provided to the system. For Type 1 and Type 2 controllers, interrupt level 4 (IRQ4) is for Serial 1 and interrupt level 3 (IRQ3) is for Serial 2. For Type 3 controllers, there is no restriction. Either of the interrupt levels (IRQ3 and IRQ4) can be assigned to any of the eight serial ports. For the serial port controller to send interrupts to the interrupt controller, bit 3 of the Modem Control register must be set to 1.

The data format is shown in the following figure.

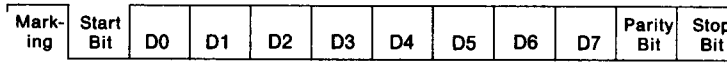


Figure 3. Serial Port Data Format

Data bit 0 (D0)is the first bit to be sent or received. The controller automatically inserts the start bit, the correct parity bit (if

programmed to do so), and the stop bits (1, 1.5, or 2 depending on the command in the Line Control register).

Programmable Baud-Rate Generator

The controller has a programmable baud-rate generator that can divide the clock input (11.0592 MHz) by any divisor from 1 to 65,535. In compatibility mode, a 1.8432 MHz clock is used. The output frequency of the baud-rate generator is the baud rate multiplied by 16. Two 8-bit latches store the divisor in a 16-bit binary format. The divisor latches are loaded during setup to ensure desired operation of the baud-rate generator. When either of the divisor latches is loaded, a 16-bit baud counter is immediately loaded. This prevents long counts on the first load.

Modem Status Interrupts

The modem status interrupts occur as soon as the corresponding input signals change state, whether the Received Data Status register is enabled or not. The current modem status is immediately available in the Modem Status register. However, the change in the modem status is reflected in the received-data-status character that follows the actual change.

Whenever the overrun error occurs, the interrupt is generated and the corresponding bit in the Line Status register is set. In character mode, when an overrun error occurs, the character in the Receiver Buffer register is overwritten. In the FIFO or DMA mode, when an overrun error occurs, the data in the FIFO mode is preserved, and the character in the Receive Shift register is overwritten. When the Received Data Status register is enabled, the overrun error is indicated in the received-status-byte of the first character received after the last error. The indicator stays on for only one character regardless of the number of characters lost, unless another error occurs.

The interrupts for parity error and frame error occur when the error character is the next one to be read from the FIFO mode in DMA, whether the Received Data Status register is enabled or not. Although these interrupts are reset by reading the Line Status register, the bits can cause an interrupt, but they do not identify which character had the error in DMA mode. The Received Data Status register must be enabled to determine which character had the error.

FIFO Modes of Operation

The serial port contains two register stacks of 16 bytes each. These register stacks are called FIFOs. One is the Receive FIFO and the other is the Transmit FIFO.

In the FIFO mode, the controller can operate in the interrupt mode or the polled mode. To enable the FIFO mode, set bit 0 in the FIFO Control register to 1.

Interrupt Mode

When the receiver interrupts are enabled in the Interrupt Enable register, they occur as follows:

- A received-data-available interrupt is issued to the system when the FIFO register has reached the programmed trigger level.
- The Interrupt Identification register's received-data-available condition is set when the trigger level is reached and, like the interrupt, is cleared when the register drops below the trigger level.
- The receiver-line-status interrupt has a higher priority than the received-data-available interrupt.
- Bit 0 in the Line Status register is set to 1 to indicate that a character is transferred from the Shift register to the FIFO register. It is set to 0 when the Receiver FIFO register is empty.

When the Receiver FIFO register and receiver interrupts are enabled, the following occurs:

- A FIFO time-out interrupt occurs if the following conditions exist:
  - At least 1 character is in the Receiver FIFO register.
  - The last character was received more than four continuous-character times ago (if 2 stop bits are programmed, the second one is included in this time delay).
  - The most recent system microprocessor read off the Receiver FIFO register was longer than four continuous-character times ago.

  This causes a maximum character-received to interrupt-issued delay of 160 milliseconds at 300 baud, with a 12-bit character.

- Character times are calculated by using the 'receiver clock' input for a clock signal (this makes the delay proportional to the baud rate).
- When a time-out interrupt has occurred, it is cleared, and the timer is reset when the system microprocessor reads one character from the Receiver FIFO register.
- When a time-out interrupt has not occurred, the time-out timer is reset after a new character is received, or after the system microprocessor reads the Receiver FIFO register.

When the Transmitter FIFO register and transmitter interrupts are enabled (FIFO Control register bit 0 and Interrupt Enable register bit 1 are set to 1), the following occurs:

- The transmitter-holding-register-empty interrupt (02) occurs when the Transmitter FIFO register is empty. It is cleared when the Transmitter Holding register is written to (1 to 16 characters can be written to the Transmitter FIFO register while this interrupt is being serviced), or the Interrupt Identification register is read.
- The transmitter-FIFO-register-empty indications are delayed one character time minus the last stop-bit time whenever both of the following occur:
  - Bit 5 (transmitter-holding-register-empty) of the Line Status register is set to 1.
  - There have not been at least two bytes in the Transmitter FIFO register at the same time since the last time bit 5 of the Line Status register was set to 1.

  The first transmitter interrupt after changing bit 0 in the FIFO Control register is immediate, if enabled.

Character time-out and Receiver FIFO register trigger-level interrupts have the same priority as the current received-data-available interrupt. The transmitter-FIFO-register-empty interrupt has the same priority as the current transmitter-holding-register-empty interrupt.

Polled Mode

To put the controller in the FIFO polled mode, disable the interrupts through the Interrupt Enable register and enable the FIFO mode. The Receiver and Transmitter FIFO registers are controlled separately. Either or both registers can be in the polled mode of operation.

In the FIFO-polled mode of operation, the system reads the status of the Receiver and Transmitter FIFO register through the Line Status register.

- The data-ready bit indicates whether or not the Receiver FIFO register contains data.
- The error bits indicate the type of error. Character error status is handled the same way as when in the interrupt mode. The Interrupt Identification register is not affected because bit 2 of the Interrupt Enable register is set to 0.
- Line Status register bit 5 indicates when the Transmitter FIFO register is empty.
- Line Status register bit 6 indicates that both the Transmitter FIFO register and Transmitter Shift register are empty.
- Line Status register bit 7 indicates any errors in the Receiver FIFO register.

There is no trigger level reached or time-out condition indicated in the FIFO polled mode; however, the Receiver and Transmitter FIFO registers are still fully capable of holding characters.

DMA Modes of Operation

In addition to the character mode and the FIFO mode of the Type 2 controller, the Type 3 controller supports the use of DMA for receiving and transmitting. The Type 3 controller also provides new functions and new interrupts, many of which are available in the FIFO mode.

The presence of a Type 3 controller can be detected by enabling the DMA transmit mode (bit 6 in Enhanced Function register 1), reading bits 6 and 7 of the Interrupt ID register, and then disabling the DMA transmit mode. If bit 6 is a 1 and bit 7 is a 0, then a Type 3 controller is installed. If the FIFO mode is enabled, but not the DMA transmit mode, then bits 6 and 7 in the Interrupt ID register read as 1. If character mode is enabled, then bits 6 and 7 are 0.

The DMA mode uses separate DMA channels for transmitting and receiving. In addition, the transmit and receive modes may be set independently. (Operating the receiver in DMA mode and the transmitter in FIFO mode will conserve DMA channels). This allows a high performance receiving function and requires only one interrupt per 16 characters transmitted.

Receive Mode

While in receive mode, the Type 3 controller signals the needs to transfer data when the Receive FIFO register has reached the receiver trigger level or when a timeout occurs. The data is then transferred from the controller until the FIFO register is empty or the DMA Terminal Count (TC) is reached. A timeout occurs if there is at least one character in the FIFO register and a character has not been read in the last four character times. An interrupt on the transmit terminal count and the receive terminal count occur independently.

Transmit Mode

While in the transmit mode, data is transferred until the FIFO register is full or the end of the data is reached.

Two separate terminal count interrupts are available: one for transmit and the other for receive.

Received Data Status Register

When received, a status byte can be placed in the FIFO register with each data byte. This option is available in the DMA receive mode and in the FIFO mode. The status byte is defined as the Received Data Status register and is stored after the corresponding data byte. The bit definitions of Received Data Status register are as follows:

Bit	Description
7	Data Carrier Detect
6	Clear to Send
5	Data Set Ready
4	Break
3	Framing
2	Parity Error
1	Overrun Error
0	Error/Break

Figure 4. Received Data Status Register

Bit 7 This bit indicates the state of the '-data carrier detect' signal (-DCD).

Bit 6 This bit indicates the state of the '-clear to send' signal (-CTS).

Bit 5 This bit indicates the state of the '-data send ready' signal (-DSR).

| **Bit 4** This bit determines Break (BI)

| **Bit 3** This bit determines Framing (FE)

| **Bit 2** This bit determines Parity Error (PE)

| **Bit 1** This bit determines Overrun Error (OE)

| **Bit 0** This bit determines the Error/Break. Bit 0 is set and reset.

| Bit 0 is set to 1 when an error or break occurs and remains set for
| subsequent characters until it is reset to 0 by a software command
| (write hex 03 to the Enhanced Command register). This allows
| scanning of the received data (in memory or as it exits from the FIFO
| mode) to find the character that was received with an error. While
| the error/break bit indicates that an error has occurred, it is not
| possible to distinguish multiple errors from single errors without
| checking the status of each character that has this bit set.

| Bit 0 is set to 1 and reset to 0 before the Received Data status
| register is placed in the FIFO mode. This means that up to eight
| characters have bit 0 set after the Reset Error/Break Indicator
| command is given and there are no additional errors.

| When the Received Data Status register is enabled the Receive FIFO
| register can hold eight data bytes and eight status bytes.

| Transmit Commands

| New transmit commands provide better software control of the
| transmitter and allow the insertion of special control characters such
| as XON and XOFF into the the transmitted data stream. The new
| transmit commands are available in both the DMA transmit mode and
| in the FIFO mode. The new transmit commands are:

- | Start Sending - starts or continues transmit
- | Stop Sending - stops transmit.

| To insert a character in the transmitted data stream, stop the
| transmitter by issuing the Stop Sending command, write a character
| to the Transmitter Holding register, and then start the transmitter by
| issuing the Start Sending command.

Modem Pacing

Modem pacing is handled by several new functions without software involvement, which are available in the DMA mode and the FIFO mode. These new functions also prevent the async port from receiving invalid data.

The transmitter and receiver are controlled by the following signals:

- The '-clear-to-send' signal
  - When this signal is equal to 0, the transmitter is turned off.
- The '-data-carrier-detect' signal
  - When this signal is equal to 0, the transmitter is turned off.
- The '-data-set-ready' signal
  - When this signal is equal to 0, the transmitter and the receiver are turned off.

Character Orientated Pacing

Three software-programmable registers are provided to handle character oriented pacing. The contents of these registers are compared to each received character. If there is a match, a preprogrammed action takes place. The possible actions on a match are interrupt, delete character, stop transmitter, and start transmitter. If an error or break occurs in a received character, it is not compared.

Receive Character Count Register

This register enables the user to keep track of the number of characters sent to the central processing unit or the DMA. The Receive Character Count Interrupt is asserted when the counter is decremented to 0, provided that bit 0 of the Enhanced Function register 1 is set.

Byte Pacing

The Byte Pacing function is useful when the Type 3 controller is communicating with a slow processor. This function enables the Type 3 controller to transmit every byte at 16 times the Receive Character Count value or 256 times the RCCR value. The result of this product is called RCLK time.

Enhanced Interrupts

Several new interrupts are available to support the DMA mode, the Receive Character Count register, and the Character Compare registers. The new interrupts are:

- Interrupt on Transmitter FIFO and transmitter-shift-register-empty
- Interrupt on Terminal Count in the DMA transmit mode
- Interrupt on Terminal Count in the DMA receive mode
- Interrupt on Receiver Character Count equals 0
- Interrupt on Character Compare Register Match.

Serial Port Controller Programming Considerations

The serial port uses either the Type 1, Type 2, or Type 3 serial communications controller. The following should be considered when programming the serial controller:

- The Type 1 serial controller does not support the FIFO mode.
- Some systems using the Type 2 controller do not support the FIFO mode. For more information, refer to the system-specific technical reference manuals.
- The Type 1 or Type 2 serial port on the system board can be configured to either Serial 1 or Serial 2 using the system configuration utilities programs. The Type 3 can be configured as Serial 1 through 8.
- Before changing the Line Control register, make sure the Transmitter Holding register is empty.

Registers

The controller has several accessible registers. These control the operations of the controller and transmit and receive data. The system programmer can gain access to or control any of the controller registers through the system microprocessor.

Compatible Registers

Type 1, Type 2 and Type 3 controllers have certain registers that are common to them all. These registers will be referred to as Compatible registers. Type 3 controllers have additional registers that Type 1 and Type 2 controllers do not have. These registers will be referred to as Enhanced registers.

Serial Port	Compatible (Hex)	Enhanced (Hex)
Serial1	03F8	83F8
Serial 2	02F8	82F8
Serial 3	3220	B220
Serial 4	3228	B228
Serial 5	4220	C220
Serial 6	4228	C228
Serial 7	5220	D220
Serial 8	5228	D228

Figure 5. Serial Port Register - Base Addresses

The bit definitions of the Interrupt Enable register, Interrupt Identification register, and Line Status register have been modified from the Type 1 controller registers. A FIFO Control register has been added to support the FIFO mode.

Note: Using the Type 1 controller in the FIFO mode can result in nondetectable data errors.

Specific registers are selected according to the figure below and the figure on the following page.

Address Offsets	R/W	Register
+ 0 *	W	Transmitter Holding Register
+ 0 *	R	Receiver Buffer Register
+ 0 *	R/W	Divisor Latch, Low Byte
+ 1 *	R/W	Divisor Latch, High Byte
+ 1 *	R/W	Interrupt Enable Register
+ 2	R	Interrupt Identification Register
+ 2	W	FIFO Control Register
+ 3	R/W	Line Control Register
+ 4	R/W	Modem Control Register
+ 5	R	Line Status Register
+ 6	R/W	Modem Status Register
+ 7	R/W	Scratch Register

Note: *The DLAB state is controlled by bit 7 of the Line Control register.

Figure 6. Serial Port Compatible Register Address Offsets

Port Address Offsets	EFR3 Bits 2 1 0	R/W	Register
+ 0	x x x	W	Enhanced Command
+ 1	x x x	R	Reserved
+ 2	x x x	R	Enhanced Interrupt Identification
+ 3	x x x	R/W	Enhanced Function 1
+ 4	x x x	R/W	Enhanced Function 2
+ 5	x x x	R/W	Enhanced Function 3
+ 5 *	0 0 0	R/W	Char Compare Function 0
+ 5 *	0 0 1	R/W	Char Compare Reg 0
+ 5 *	0 1 0	R/W	Char Compare Function 1
+ 5 *	0 1 1	R/W	Char Compare Reg 1
+ 5 *	1 0 0	R/W	Char Compare Function 2
+ 5 *	1 0 1	R/W	Char Compare Reg 2
+ 6 *	x x x	R/W	Char Compare Data Reg
+ 7	x x x	R./W	Receive Character Count

*The Char Compare Function Register (CCFR) and the Char Compare Register (CCR) are selected by writing the address to the Enhanced Function Register 3 and the data is read or written by reading or writing to the Char Compare Data Register (CCDR).

Figure 7. Serial Port Enhanced Register Address Offsets

Transmitter Holding Register (Base c + 0)

The Transmitter Holding register contains the character to be sent when the (DLAB) divisor latch access bit 1 equals 0. Bit 0 is the least-significant bit and the first bit sent serially, as shown below.

Bit	Description
7	Data Bit 7
6	Data Bit 6
5	Data Bit 5
4	Data Bit 4
3	Data Bit 3
2	Data Bit 2
1	Data Bit 1
0	Data Bit 0

Figure 8. Transmitter Holding Register (Base c + 0)

Receiver Buffer Register (Base c + 0)

The Receiver Buffer register contains the received character and can be accesses when the divisor-latch-access bit (DLAB) equals 0. Bit 0 is the least-significant bit and the first bit received serially, as shown in the following figure.

Bit	Description
7	Data Bit 7
6	Data Bit 6
5	Data Bit 5
4	Data Bit 4
3	Data Bit 3
2	Data Bit 2
1	Data Bit 1
0	Data Bit 0

Figure 9. Receiver Buffer Register (Base c + 0)

Divisor Latch Register (Base c + 1)

The Divisor Latch register is used to program the baud-rate generator. The value in this register forms the divisor of the clock input (1.8432 MHz or 11,0592MHz), which establishes the desired baud-rate (DLAB = 1).

Bit	Description
7	Bit 7
6	Bit 6
5	Bit 5
4	Bit 4
3	Bit 3
2	Bit 2
1	Bit 1
0	Bit 0

Figure 10. Divisor Latch Register, Low Byte (Base c + 1)

Note: If bit 6 of the Enhanced Function register 2 is set to 0, then the input clock of the baud-rate generator is 1.8432 MHz. Otherwise, the input clock is 11.0592 MHz.

Divisor Latch Register (Base c + 0)

The Divisor Latch register is used to program the baud-rate generator. The value in this register forms the divisor of the clock input (1.8432 MHz or 11,0592MHz), which establishes the desired baud-rate (DLAB = 0).

Bit	Description
7	Bit 7
6	Bit 6
5	Bit 5
4	Bit 4
3	Bit 3
2	Bit 2
1	Bit 1
0	Bit 0

Figure 11. Divisor Latch Register, Low Byte (Base c + 0)

Bit	Description
7	Bit 15
6	Bit 14
5	Bit 13
4	Bit 12
3	Bit 11
2	Bit 10
1	Bit 9
0	Bit 8

Figure 12. Divisor Latch Register, High Byte (Base c + 1)

Figure 13 on the following page illustrates the use of baud-rate generator with a frequency of 1.8432 MHz.

Note: Data speed should not exceed 19,200 baud (For Type 1 and Type 2).

Desired Baud Rate Rate	Divisor Used to Generate 16x Clock (Decimal)	(Hex)	Percent of Error Difference between Desired and Actual
50	2304	0900	--
75	1536	0600	--
110	1047	0417	0.026
134.5	857	0359	0.058
150	768	0300	--
300	384	0180	--
600	192	00C0	--
1200	96	0060	--
1800	64	0040	--
2000	58	003A	0.69
2400	48	0030	--
3600	32	0020	--
4800	24	0018	--
7200	16	0010	--
9600	12	000C	--
19200	6	0006	--

Figure 13. Baud Rates at 1.8432 MHz (Low Frequency Mode)

The following figure illustrates the use of the baud rate generator with a frequency of 11.0592 MHz.

Desired Baud Rate	Divisor Used to Generate 16x Clock (Decimal)	(Hex)	Percent of Error Difference between Desired and Actual
50	13824	3600	--
75	9216	2400	--
110	6284	188C	0.006
134.5	5139	1413	0.001
150	4608	1200	--
300	2304	900	--
600	1152	480	--
1200	576	240	--
1800	384	180	--
2000	346	15A	0.116
2400	288	120	--
3600	192	C0	--
4800	144	90	--
7200	96	60	--
9600	72	48	--
19200	36	24	--
31250	22	16	0.538
38400	18	12	--
57600	12	C	--
115200	6	6	--
172800	4	4	--
345600	2	2	--

Note: Divisor of 1 not supported. Data speed must not exceed 345.6Kbaud.

Figure 14. Baud Rates at 11.0592 MHz (High Frequency Mode)

Interrupt Enable Register (Base c + 1)

This 8-bit register allows the four types of controller interrupts to separately activate the 'chip interrupt output' signal. The interrupt system can be completely disabled by setting bits 0 through 3 of the Interrupt Enable register to 0. Similarly, by setting the appropriate bits of this register to 1, selected interrupts can be enabled. Disabling prevents the controller from generating the external interrupt to the system. All other system functions operate normally, including the setting of the Line Status and Modem Status registers (DLAB = 0).

Bit	Description
7 - 4	Reserved = 0
3	Modem-Status Interrupt
2	Receiver-Line-Status Interrupt
1	Transmitter-Holding-Register-Empty Interrupt
0	Received-Data-Available Interrupt (Character and FIFO Mode) and Time-Out Interrupts (FIFO Mode Only)

Figure 15. Interrupt Enable Register (Base c + 1)

Bits 7 - 4 These bits are reserved and always set to 0.

Bit 3 When set to 1, this bit enables the modem-status interrupt.

Bit 2 When set to 1, this bit enables the receiver-line-status interrupt.

Bit 1 When set to 1, this bit enables the transmitter-holding-register-empty interrupt.

Bit 0 When set to 1, this bit enables the received-data-available interrupt. In the FIFO mode, this bit also enables the time-out interrupts.

FIFO Control Register (Base c + 2)

The FIFO Control register is a write-only register at the same location as the read-only Interrupt Identification register. The FIFO Control register enables the FIFO registers, clears the FIFO registers, and sets the Receiver FIFO register trigger level.

Note: The Transmitter and Receiver FIFO registers are not accessible serial controller registers.

The contents of the FIFO Control register are shown in the following figure.

Bit	Description
7, 6	Receiver FIFO Register Trigger
5 - 3	Reserved = 0
2	Transmitter FIFO Register Reset
1	Receiver FIFO Register Reset
0	FIFO Mode Enable

Figure 16. FIFO Control Register (Base c+2)

Bits 7, 6 These bits select the trigger level for the receiver-register interrupt, as shown in the following figure.

Bits 7 6	Receiver Trigger Level
0 0	01 Byte
0 1	04 Bytes
1 0	08 Bytes
1 1	14 Bytes

Figure 17. Trigger Level

Bits 5 - 3 These bits are reserved and always set to 0.

Bit 2 When this bit is set to 1, all bytes in the Transmitter FIFO register are cleared and its counter logic is reset to 0. The Transmitter Shift register is not cleared. This bit is self-clearing.

Bit 1 When this bit is set to 1, all bytes in the Receiver FIFO register are cleared and its counter logic is reset to 0. The Transmitter Shift register is not cleared. This bit is self-clearing.

Bit 0 When this bit is set to 1, the FIFO mode is enabled. When this bit is changed, the transmit and receive (XMIT and RCV) FIFOs are cleared. When writing to any other FIFO Control register bits, this bit must be a 1.

Interrupt Identification Register (Base c + 2)

To minimize programming overhead during character mode transfers, the controller prioritizes interrupts into four levels:

- Priority 1 - Receiver-line-status
- Priority 2 - Received-data-available
- Priority 2 - Time-out (FIFO mode)
- Priority 3 - Transmitter-holding-register-empty
- Priority 4 - Modem status.

Information about a pending interrupt is stored in the Interrupt Identification register. When this register is addressed, the pending interrupt with the highest priority is held, and no other interrupts are acknowledged until the system microprocessor services that interrupt.

Bit	Description
7, 6	FIFO Registers Enabled
5, 4	Interrupt ID, Bit 4
3	Interrupt ID, Bit 2
2	Interrupt ID, Bit 1
1	Interrupt ID, Bit 0
0	Interrupt Not Pending

Figure 18. Interrupt Identification Register (Base c + 2)

Bits 7,6 Programs can determine whether a Type 1, Type 2, or Type 3 controller is present by reading these two bits when bit 0 of the FIFO Control register is set to 1. If bits 7 and 6 are set to 1, the Type 2 controller is present and FIFO support is provided. If bit 6 is set to 0, the controller is a Type 1 and the FIFO mode should not be used.

Bit 7	Bit 6	Version
0	0	Type 1 controller
1	0	N/A
0	1	Type 3 controller
1	1	Type 2 controller

Figure 19. Type controllers for Bits 7 and 6

Note: Some systems using the Type 2 controller do not support the FIFO mode. For information about individual systems refer to the system-specific technical reference manuals.

Bits 5, 4 These bits are always set to 0.

Bit 3 In the FIFO mode, this bit is set to 1, along with bit 2, to indicate that a time-out interrupt is pending. In the character mode, this bit is always set to 0.

Bits 2, 1 These two bits identify the pending interrupt with the highest priority.

Bit 0 When this bit is set to 1, no interrupt is pending and polling (if used) continues. When this bit is set to 0, an interrupt is pending, and the contents of this register can be used as a pointer to the appropriate interrupt service routine. This bit can be used in hard-wired, prioritized, or polled conditions to indicate if an interrupt is pending.

Figure 20 on page 21 illustrates the Interrupt Control functions, beginning with the highest priority and ending with the lowest priority.

Bits 5 4 3 2 1 0	Type	Cause	Interrupt Reset Control
0 0 0 1 1 0	Receiver Line Status	Overrun, Parity, or Framing Error or Break Interrupt	Read the Line Status Register
0 0 0 1 0 0	Received Data Available	Data in the Receiver Buffer or the Trigger Level Has Been Reached.	Read the Receiver Buffer Register or FIFO Register Drops Below the Trigger Level.
0 0 1 1 0 0*	Character Time-Out Indication	No Characters Have Been Removed From or Put Into the Receiver FIFO Register During the Last Four Character Times, and at Least 1 Character is in it at This Time.	Read the Receiver Buffer Register
0 0 0 0 1 0	Transmitter Holding Register Empty	Transmitter Holding Register is Empty	Read the Interrupt Identification Register or Write to Transmitter Holding Register
0 0 0 0 0 0	Modem Status	Change in Signal Status From Modem	Read the Modem Status Register

* FIFO Mode Only

Figure 20. Interrupt Control Functions

Line Control Register (Base c + 3)

The format of asynchronous communications is programmed through the Line Control register.

Bit	Description
7	Divisor Latch Access Bit
6	Set Break
5	Stick Parity
4	Even Parity Select
3	Parity Enable
2	Number of Stop Bits
1	Word Length Select, Bit 1
0	Word Length Select, Bit 0

Figure 21. Line Control Register (Base c + 3)

Bit 7 This bit is set to 1 to gain access to the divisor latches of the baud-rate generator. It is set to 0 to gain access to the Receiver Buffer, Transmitter Holding, or Interrupt Enable registers.

Bit 6 When this bit is set to 1, set break is enabled. The serial output is forced to the spacing state and remains there regardless of other transmitter activity. When this bit is set to 0, set break is disabled.

Bit 5 When bits 5, 4, and 3 are set to 1, the parity bit is sent and checked as a logical 0. When bits 5 and 3 are set to 1, and bit 4 is set to 0, the parity bit is sent and checked as a logical 1. If bit 5 is set to 0, stick parity is disabled.

Bit 4 When this bit and bit 3 are set to 1, an even number of logical 1s are transmitted and checked in the data word bits and parity bit. When this bit is set to 0, and bit 3 is set to 1, an odd number of logical 1s are transmitted and checked in the data word bits and parity bit.

Bit 3 When set to 1, a parity bit is generated (transmit data) or checked (receive data) between the last data-word bit and stop bit of the serial data. (The parity bit produces an even or odd number of 1s when the data-word bits and the parity bit are summed).

Bit 2 This bit, with bits 0 and 1, specifies the number of stop bits in each serial character sent or received, as shown in the following figure.

Bits 2 1 0	Number of Stop Bits	Word Length
0 0 0	1	5 Bits
0 0 1	1	6 Bits
0 1 0	1	7 Bits
0 1 1	1	8 Bits
1 0 0	1.5	5 Bits
1 0 1	2	6 Bits
1 1 0	2	7 Bits
1 1 1	2	8 Bits

Word length is specified by bits 1 and 0 in this register.

Figure 22. Stop Bits and Word Length

Bits 1, 0 These bits specify the number of bits in each serial character that is sent or received.

Modem Control Register (Base c + 4)

This 8-bit register controls the data exchange with the modem, data set, or peripheral device emulating a modem.

Bit	Description
7 - 5	Reserved = 0
4	Loop Mode
3	Out 2 (IRQ Output Control)
2	Out 1
1	Request-to-Send
0	Data-Terminal-Ready

Figure 23. Modem Control Register (Base c + 4)

Bits 7 - 5 These bits are reserved and always set to 0.

Bit 4 This bit provides a loopback feature for diagnostic testing of the serial port. When bit 4 is set to 1:

- Transmitter-serial-output is set to the marking state.
- Receiver-serial-input is disconnected.
- Output of the Transmitter Shift register is "looped back" to the Receiver Shift register input.

  Note: The Transmitter and Receiver Shift registers are not accessible NS16550 registers.
- The modem control inputs (CTS, DSR, DCD, AND RI) are disconnected.
- The modem control outputs (DTR, RTS, OUT 1, AND OUT 2) are internally connected to the four modem control inputs.
- The modem control output pins are forced inactive.

When the serial port is in the diagnostic mode, transmitted data is immediately received. This feature allows the system microprocessor to verify the transmit-data and receive-data paths of the serial port.

When the serial port is in the diagnostic mode, the receiver and transmitter interrupts are fully operational. The modem control interrupts are also operational, but their sources are the lower four bits of the Modem Control

register instead of the four modem control input signals. The interrupts are still controlled by the Interrupt Enable register.

Bit 3 When this bit is set to 0, the IRQ signal is disabled, the IRQ signal is always disabled.

Bit 2 This bit is not used in a normal mode. In loop mode, its status is reported to bit 6 (RI) of the Modem Status register.

Bit 1 This bit controls the '-request to send' signal (-RTS) modem control output. When this bit is set to 1, -RTS is active. When this bit is set to 0, -RTS is inactive.

Bit 0 This bit controls the '-data terminal ready' signal (-DTR) modem control output. When this bit is set to 1, -DTR is active. When this bit is set to 0, -DTR is inactive.

Line Status Register (Base c + 5)

This 8-bit read-only register provides the system microprocessor with status information about the data transfer.

Note: Writing to this register can produce unpredictable results.

Bit	Description
7	Error in Receiver FIFO Register
6	Transmitter Shift Register Empty
5	Transmitter Holding Register Empty
4	Break Interrupt
3	Framing Error
2	Parity Error
1	Overrun Error
0	Data Ready

Figure 24. Line Status Register (Base c + 5)

Bit 7 In FIFO mode, this bit indicates that a parity error, framing error, or break occurred. This bit is cleared when the Line Status register is read in the FIFO mode. It is set to 0 in the Character mode.

Bit 6 This bit is set to 1 to indicate the Transmitter Holding register and the Transmitter Shift register are both empty. This bit is set to 0 when either register contains a data character.

In the FIFO or DMA mode, this bit is set to 1 when the Transmitter FIFO register and the Transmitter Shift register are both empty.

Bit 5 This bit indicates that the controller is ready to accept the next character for transmission. This bit is set to 1 to indicate that a character was transferred from the Transmitter Holding register to the Transmitter Shift register. This bit is set to 0 when a character is written to the Transmitter Holding register.

This bit also causes the controller to issue an interrupt if the interrupt is enabled.

In the FIFO or DMA register, this bit is set to 1 when the Transmitter FIFO register is empty. It is set to 0 when at least one byte is written to the Transmitter FIFO register.

Bit 4 This bit is set to 1 to indicate the received data input is held in the spacing state for longer than a fullword transmission time (the total time of start bit + data bits + parity + stop bits). This bit is reset to 0 when the Line Status register is read.

When a break interrupt occurs, only one zero character is loaded into the Receiver FIFO register. The next character is loaded after the receiver serial input changes to the marking state and receives the next valid start bit.

Note: Bits 1 through 4 are the error conditions that produce a receiver-line-status interrupt whenever any of the corresponding conditions are detected and the interrupt is enabled.

Bit 3 This bit is set to 1 when the stop bit, following the last data bit or parity bit, is at a spacing level. This indicates that the received character did not have a valid stop bit (framing error). This bit is reset to 0 when the Line Status register is read.

Note: In the FIFO or DMA mode, the framing error (or parity error for bit 2) is associated with the particular character in the Receiver FIFO register that it applies to. The error is indicated to the system microprocessor when its associated character is at the top of the Receiver FIFO register.

Bit 2 This bit is set to 1 to indicate a parity error (the received character does not have the correct even or odd parity, as selected by the even-parity-select bit). This bit is reset to 0 when the Line Status register is read.

Bit 1 When set to 1, this bit indicates that data in the Receiver Buffer register was not read before the next character was transferred into the Receiver Buffer register, destroying the previous character. This bit is reset to 0 when the Line Status register is read.

If the FIFO or DMA mode data continues to fill the Receiver FIFO register beyond the trigger level, an overrun error occurs. The overrun occurs only after the Receiver FIFO register is full and the next character is completely received in the Receiver Shift register. An overrun error is indicated to the system microprocessor when it happens. The character in the Receiver Shift register is overwritten, but it is not transferred to the Receiver FIFO register.

Bit 0 This bit is the receiver data-ready indicator. It is set to 1 when a complete incoming character has been received and transferred into the Receiver Buffer register or the Receiver FIFO register. This bit is reset to 0 by reading the Receiver Buffer register or by reading all of the data in the Receiver FIFO register.

Modem Status Register (Base c + 6)

This 8-bit register is used to monitor the current state of the control lines from the modem (or external device). Also, bits 3 through 0 indicate change information.

Bit	Description
7	Data-Carrier-Detect
6	Ring Indicator
5	Data-Set-Ready
4	Clear-to-Send
3	Delta-Data-Carrier-Detect
2	Trailing Edge Ring Indicator
1	Delta-Data-Set-Ready
0	Delta-Clear-to-Send

Figure 25. Modem Status Register (Base c + 6)

Bit 7 This bit is the inverted '-data carrier detect' signal (-DCD) modem control input. If bit 4 of the Modem Control register is set to 1, this bit is equivalent to bit 3 in the Modem Control register.

Bit 6 This bit is the inverted '-ring indicator' signal (-RI) modem control input. If bit 4 of the Modem Control register is set to 1, this bit is equivalent to bit 2 in the Modem Control register.

Bit 5 This bit is the inverted '-data set ready' signal (-DSR) modem control input. If bit 4 of the Modem Control register is set to 1, this bit is equivalent to bit 0 in the Modem Control register.

Bit 4 This bit is the inverted '-clear to send' signal (-CTS) modem control input. If bit 4 of the Modem Control register is set to 1, this bit is equivalent to bit 1 in the Modem Control register.

Bit 3 When set to 1, this bit indicates that the '-data carrier detect' signal (-DCD) modem control input has changed state since the last time it was read by the system microprocessor.

Note: Whenever bit 0, 1, 2, or 3 is set to 1, a modem status interrupt is generated.

Bit 2 When set to 1, this bit indicates that the '-ring indicator' signal (-RI) modem control input has changed from an active condition to an inactive condition.

Bit 1 When set to 1, this bit indicates that the '-data set ready' signal (-DSR) modem control input has changed state since the last time it was read by the system microprocessor.

Bit 0 When set to 1, this bit indicates that the '-clear to send' signal (-CTS) modem control input has changed state since the last time it was read by the system microprocessor.

Scratch Register (Base c + 7)

This register can be used by the system microprocessor as a temporary buffer or work area.

Enhanced Registers

The registers in this section are only available with the Type 3 controller. These registers are:

- Enhanced Command Register
- Enhanced Interrupt ID Register
- Enhanced Function Register 1
- Enhanced Function Register 2
- Enhanced Function Register 3
- Character Compare Data Register
- Receive Character Count Register.

Enhanced Command Register (Base e + 0)

This write-only register is used to issue the new commands: Stop Sending, Start Sending, and Reset Error/Break Indicator. A write to the register causes the command to be executed.

Bits	Description
7 - 2	Reserved
1, 0	Command Bits

Figure 26. Enhanced Command Register

Bits 7-2 These bits are reserved and always written as 0 to allow future expansion of the command bits.

Bits 1,0 These command bits (CB1-CB0) enable Stop Sending and Start Sending.

CB1	CB0	Command
0	0	Reserved
0	1	Start Sending
1	0	Stop Sending
1	1	Reset Error/Break Indicator

Figure 27. Command Decode

Start Sending - This command starts or continues transmitting in the DMA or the FIFO mode. Characters in the FIFO mode are transmitted first. This command is used in the FIFO mode to restart the

transmitter if it has been stopped by a Stop Sending command or by a Stop on Match function. In DMA mode, the transmit DMA request (TX DMA REQ) will not be active until the Start Sending Command is issued.

Stop Sending - This command empties the Transmitter Shift register and stops transmitting, regardless of the FIFO mode. After the transmitter is stopped, a character is written to the Transmitter Holding register. The character is then loaded into the Shift register and transmitted. After the character is written to the transmitter-holding-register-empty, the interrupt can be enabled. When the interrupt occurs, it signals that the send-single-character operation is complete. If multiple characters are written to the Transmitter Holding register, with the transmitter-holding register-empty interrupt enabled, multiple interrupts occur. To ensure that all characters have been transmitted, wait for the appropriate number of transmitter-holding register-empty interrupts before issuing the next Start Sending command to resume transmitting the FIFO register. There is no interrupt associated with this command. The shift register operation is not affected by this command.

Reset Error/Break - This command resets the Error/Break bit in the received-data-status byte, which is optionally stored with received data. The Reset command affects the next status byte, which is stored in the FIFO register.

The logic for controlling the Error/Break bit is at the input of the Receive FIFO. If there is an error for the current character being received, the corresponding status byte will have the Error/Break bit set. When the command to reset the Error/Break indicator is issued, the indicator is 0 in the next received-data-status byte placed in the FIFO register, unless that byte also has an error.

Check each byte that has the Error/Break bit set and issue a Reset command every time an error is found. This procedure should minimize the overhead associated with error detection.

Reserved Register (Base e + 1)

This is a reserved register.

Enhanced Interrupt ID Register (Base e + 2)

The pending interrupt is determined by decoding bits 1 through 5. For interrupt reset purposes, reading this register is equivalent to reading the Interrupt ID register.

Bits	Description
7 - 6	Reserved
5 - 1	Interrupt ID
0	Interrupt Pending

Figure 28. Enhanced Interrupt ID Register

Bits 7 - 6 These bits are reserved and are always set to 0.

Bits 5 - 1 These bits are the encoded IDs of the pending interrupt.

Bit 0 This bit indicates if an interrupt is pending. When it is a 0, an interrupt is pending, and bits 1 - 5 identify the interrupt. When it is a 1, no interrupt is pending.

The new interrupts have higher priority than the existing Type 2 controller interrupts. After a new interrupt has been enabled, interrupt priority exists. The following figure illustrates the Enhanced Interrupt Control functions, beginning with the highest priority and ending with the lowest priority.

Bits 5 4 3 2 1 0	Type	Source	Interrupt Reset Control
1 0 0 0 0 0	Receive TC	TC on DMA Receive	Read the Enhanced Interrupt Register
1 0 0 0 1 0	Transmit TC	TC on DMA Transmit	Read the Enhanced Interrupt Register
1 1 0 0 0 0	CC0 Match	Match on CC0	Read the Enhanced Interrupt ID Register
1 1 0 0 1 0	CC1 Match	Match on CC1	Read the Enhanced Interrupt ID Register
1 1 0 1 0 0	CC2 Match	Match on CC2	Read the Enhanced Interrupt ID Register
1 0 0 1 0 0	RCCR = 0	Receive Character Count	Read the Enhanced Interrupt ID Register
1 0 0 1 1 0	Transmitter Empty	THR and TSR Empty	Read the Enhanced Interrupt ID Register
0 0 0 1 1 0	Receiver Line Status	Overrun, Parity, or Framing Error or Break Interrupt	Read the Line Status Register
0 0 0 1 0 0*	Received Data Available	Data in the Receiver Buffer or the Trigger Level Has Been Reached.	Read the Receiver Buffer Register or FIFO Register Drops Below the Trigger Level.
0 0 1 1 0 0**	Character Time-Out Indication	No Characters Have Been Removed From or Put Into the Receiver FIFO Register During the Last Four Character Times	Read the Receiver Buffer Register in FIFO Mode. In DMA Mode Read EIIR to Reset.
0 0 0 0 1 0	Transmitter Holding Register Empty	Transmitter Holding Register is Empty	Read the Interrupt Identification Register or Write to Transmitter Holding Register
0 0 0 0 0 0	Modem Status	Change in Signal Status from Modem	Read the Modem Status Register

Note: *No trigger level interrupt in DMA Mode. ** FIFO and DMA Mode

Figure 29. Enhanced Interrupt Control Functions

Enhanced Function Register 1 (Base e + 3)

This register is a read and write register that enables new interrupts and DMA modes. A logical 1 enables the function and a logical 0 disables the function.

Bits	Description
7	DMA Receive
6	DMA Transmit
5	Enable Receive Data Status
4	Terminal Count Receive
3	Terminal Count Transmit
2	Stop Transmitter Line Error
1	Transmitter Empty
0	Receive Character Count Register

Figure 30. Enhanced Function Register 1 (Base e+3)

Bit 7 This bit enables the DMA receive mode. The FIFO mode must be enabled (bit 0 in the FIFO Control register) before the DMA receive mode is enabled. The FIFO trigger level can be programmed, as appropriate, by writing to bits 6 and 7 in the FIFO Control register.

Bit 6 This bit enables the DMA transmit mode. The FIFO mode must be enabled (bit 0 in the FIFO Control Register) before the DMA transmit mode is enabled. Initially, a Start Sending command must be issued to start actual transmission. TX REQ cannot be generated until a Start Sending Command is issued.

Bit 5 This bit enables alternate bytes of data followed by Received Data status, to be stored in the Receive FIFO register. When this bit is set to 1, the Receive FIFO register has a capacity of eight data bytes plus eight status bytes. If a status byte is at the bottom of the FIFO register, the Line Status register indicates a good byte regardless of the status of the associated data byte. The enhanced-received-data-status bit should be set as part of the async port initialization. Toggling this bit while receiving serial data produces undefined results.

Note: No data is received during the time the FIFO register is cleared and the received-data status bit is toggled. Resetting this bit disables the storing of received data status.

Bit 4 This bit enables an interrupt when the terminal count is reached on a DMA receive operation. This signals that the last character of the last DMA buffer has been filled and that the FIFO register can fill and overrun if new DMA buffers are not allocated.

Bit 3 This bit enables an interrupt when the terminal count is reached on a DMA transmit operation. This signals that the last character in the last DMA buffer has been read into the FIFO register.

Bit 2 When set, this bit stops the transmitter after the Shift register empties on any received line error (OE, PE, FE, BI). The received line error is detected before the character is placed in the FIFO or DMA mode. The receiver continues to function normally. The transmitter can be restarted with the Start Sending command. If an interrupt is desired, the enable-line-status interrupt bit must be set in the Interrupt Enable register.

Bit 1 This bit enables an interrupt when the Transmit Hold register and Transmit Send register are empty in Character mode, or when the FIFO register and Transmit Send register are empty in the FIFO or DMA mode. The transmitter empty bit in the Line Status register is changed from 0 to 1.

Bit 0 This bit enables an interrupt when the Receive Character Count register is decremented to zero.

Enhanced Function Register 2 (Base e + 4)

This read and write register enables the transmitter controls, the modem pacing, and the baud-rate functions. A logical 1 enables the function and a logical 0 disables the function.

Bits	Description
7	Byte Pacing
6	Set High Frequency Rate
5	Set Slow Transmit Rate
4	Set Slow Receiver Rate
3	Receive the Receiver via DSR
2	Control the Transmitter via DCD
1	Control the Transmitter via DSR
0	Control the Transmitter via CTS

Figure 31. Enhanced Function Register 2 (Base e + 4)

Bit 7 This bit affects byte pacing. This function supports a slow processor, from which a Type 3 controller transmits data. When this bit is high, every byte of data is transmitted at a pacing rate of 256 times the Receive Character Count register value 'receiver clocks'. Interrupt is generated when the Receive Character Count register reaches 0 and the Enhanced Function Register One equals 1. When this bit is

low, the Receive Character Count register is used for counting receiving characters if the Receive Character Count register is loaded with a value greater than 0.

Bit 6 This bit sets the high-frequency rate. When set to 1 this bit selects a a 11.0592 frequency.

Note: Applications that select the 11.0592 MHz rate should reset this bit to 0 when exiting.

This allows higher bit rates to be selected, up to a maximum rate of 345,600 bits per second on transmit and receive. If this bit is set, then the divisor latches must be set to 2 or greater.

Bit 5 This bit sets the slow transmit rate to 1/16 of the rate programmed in the baud-rate generator.

Bit 4 This bit sets the slow receiver rate. If this bit is set, the receiver rate is set to 1/16 of the rate programmed in the baud-rate generator.

Note: Bits 4, 5, and 6 should be set as part of the async port initialization. Toggling these bits during transmit and receive can produce undefined results.

Bit 3 This bit resets the receiver by issuing the '-data set ready' signal (-DSR, bit 5 of the Modem Status register). If this function is enabled, the receiver is turned off when -DSR equals 0 (bit 5 of the Modem Status register equals 0) and is turned on when -DSR equals 1 (bit 5 of the Modem Status register equals 1). If -DSR becomes inactive, the character currently being received is discarded.

Bit 2 This bit controls the transmitter by issuing the '-data carrier detect' signal (-DCD, bit 3 of the Modem Status register). If this function is enabled, the transmitter is turned off when the -DCD equals 0 (bit 3 of the Modem Status register), and is turned on if -DCD equals 1. However, the transmitter must be initially turned on by a Start Sending command (After a Start Sending command has been issued, the transmitter is turned on and off based on the state of the '-data carrier detect' signal).

Note: If the transmitter is stopped, the Transmitter Shift register is emptied but no additional characters are loaded from the Transmitter FIFO or Transmitter Hold register.

Bit 1 This bit controls the transmitter via the '-data set ready' signal (-DSR). If this function is enabled, the transmitter is turned off when -DSR equals 0, and is turned on when -DSR equals 1. However, the transmitter must be initially turned on by a Start Sending command (After a Start Sending command has been issued the transmitter is turned on and off based on the state of the '-data set ready' signal).

Bit 0 This bit controls the transmitter via the '-clear-to-send' signal. (-CTS, bit 4 of the Modem Status register). If this function is enabled, the transmitter is turned off when -CTS equals 0, and is turned on when -CTS equals 1. However, the transmitter must be initially turned on by a Start Sending command (After a Start Sending command has been issued the transmitter is turned on and off based on the state of the 'clear-to-send' signal).

Enhanced Function Register 3 (Base e + 5)

This read and write register is used to control the Character Compare registers. There are three 8-bit Character Compare registers and three 4-bit Character Compare Function registers. The Character Compare registers contain match characters and the Character Compare Function registers contain match functions. A Character Compare register and its Character Compare Function register can be programmed independently of the other Character Compare registers and character compare function registers.

To read from or write to the Character Compare registers, the address for the register must be written to Enhanced Function Register 3. Then the registers can be read from or written to, using the Character Compare register.

Bits	Description
7 - 3	Reserved
2 - 1	Character Compare Address Lines
0	Select Character Compare Register

Figure 32. Enhanced Function Register 3 (Base e + 3)

Bits 7 - 3 These bits are reserved and are always set to 0.

Bits 2 - 1 These bits select the character compare address lines, the address of the character compare register, or the address of the Character Compare Function register.

Bit 0 This bit enables the Select Character Compare register. A logical 1 specifies the address in bits 1 and 2 for a Character Compare register. A logical 0 specifies the address for a Character Compare Function register.

The following table shows access to the Character Compare registers and the Character Compare Function registers for bits 2, 1 and 0.

Bits 2 1 0	Function of Character Compare Data Register	Result
0 0 0	Match Functions	R/W Character Compare Function Register 0
0 1 0	Match Functions	R/W Character Compare Function Register 1
1 0 0	Match Functions	R/W Character Compare Function Register 2
0 0 1	Match Character	R/W Character Compare Register 0
0 1 1	Match Character	R/W Character Compare Register 1
1 0 1	Match Character	R/W Character Compare Register 2

Figure 33. Access to CCRs and CCFRs

Character Compare Data Register (Base e + 6)

This register is used to read and write the match character for a Character Compare register, or the match function for a Character Compare Function register. The register is specified by first writing to Enhanced Function Register 3.

On a match, the Type 3 controller can be programmed to start the transmitter, stop the transmitter, delete the matched character from the incoming data stream, or to interrupt. Multiple match functions per Character Compare Function register are supported. If START and STOP are both set, then STOP takes precedence because they are mutually exclusive. Each character compare register is compared to the received data character, and if there is a match, then the programmed action takes place.

If the Type 3 controller is programmed to interrupt on a character match, then the interrupt occurs as soon as the match is detected. To disable a character compare register, clear the corresponding Character Compare Function register. The format of the Character Compare Data register for the Character Compare Function register is shown on the following page.

Bits	Description
3	Start Transmitter on Character Match
2	Stop Transmitter on Character Match
1	Delete Character on Character Match
0	Interrupt on Character Match

Figure 34. Character Compare Register (Base e + 6)

Bit 3 A1 starts the transmitter when a match occurs. The transmitter does not start unless a Start Transmitter command has been issued previously.

Bit 2 A1 stops the transmitter when a match occurs.

Bit 1 A1 causes the character to be deleted when a match occurs.

Bit 0 A1 enables an interrupt when a match occurs. This interrupt occurs as soon as there is a match with a received data character.

The format of the Character Compare Data register for a character compare register is an 8-bit match character. If the word length is less than eight bits, the match character should be right justified and any unused bits should be set to 0 when written to the Character Compare Data Register.

Receive Character Count Register (Base e + 7)

This 8-bit register is used in byte pacing and receive character count functions. The Receive Character Compare register is decremented when a character is read from the Receive FIFO register during a receive character count operation, or at every 256 receiver clocks during Byte Pacing operation.

If the interrupt on Receiver Character Count is set (Enhanced Function Register 1, Bit 0), then an interrupt is generated when the Receive Character Count register is decremented to 0, regardless of any operation.

Because this register is a countdown counter and does not wrap around when reaching zero, the user must load a value to the Receive Character Count register before using it. When read, this register contains the current count (the count cannot be exact since the receiver or 'receiver clocks' cannot be stopped to read this register).

Signal Descriptions

Modem-Control Input Signals

The following are input signals from the modem or external device to the controller. Bits 7 through 4 in the Modem Status register indicate the condition of these signals. Bits 3 through 0 monitor these signals to indicate when the modem changes state.

-Clear to Send (-CTS)

When active, this signal indicates that the modem is ready for the serial port to transmit data.

-Data Set Ready (-DSR)

When active, this signal indicates that the modem or data set is ready to establish the communications link and transfer data with the controller.

-Ring Indicator (-RI)

When active, this signal indicates that the modem or data set detected a telephone ringing signal.

-Data Carrier Detect (-DCD)

When active, this signal indicates that the modem or data set detected a data carrier.

Modem-Control Output Signals

The following are controller output signals. All are set inactive by a master reset operation. These signals are controlled by bits 3 through 0 in the Modem Control register.

-Data Terminal Ready (-DTR)

When active, this signal informs the modem or data set that the controller is ready to communicate.

-Request to Send (-RTS)

When active, this signal informs the modem or data set that the controller is ready to send data.

Voltage Interchange Information

The signal is considered in the *marking* condition when the voltage on the interchange circuit, measured at the interface point, is more negative than -3 Vdc, with respect to signal ground. The signal is considered in the *spacing* condition when the voltage is more positive than +3 Vdc with respect to signal ground. The region between +3 Vdc and -3 Vdc is defined as the transition region and is considered an invalid level. Voltage that is more negative than -15 Vdc or more positive than +15 Vdc also is considered an invalid level.

Interchange Voltage	Binary State	Signal Condition	Interface Control Function
Positive Voltage	Binary 0	Spacing	On
Negative Voltage	Binary 1	Marking	Off

Figure 35. Voltage Levels

Extended Performance Requirements

Extended performance applies to Type 3 serial port controllers only. Although the serial port is compatible with EIA-232-D at speeds up to 20,000 bits per second, there are additional requirements for operating the port at speeds up to 345,600 bits per second. These requirements fall into two areas, the interconnection cable and the attached equipment.

The cable should not be longer than 20 feet when operating at extended performance speeds. Each signal wire has an individual shield and should have capacitance between 100 and 450 picofarads to the shield. All individual shields are connected to pin 7 at each end. These requirements can be met by using one IBM Personal Computer Communications Adapter Cable for 10 feet, or two connected in series for 20 feet.

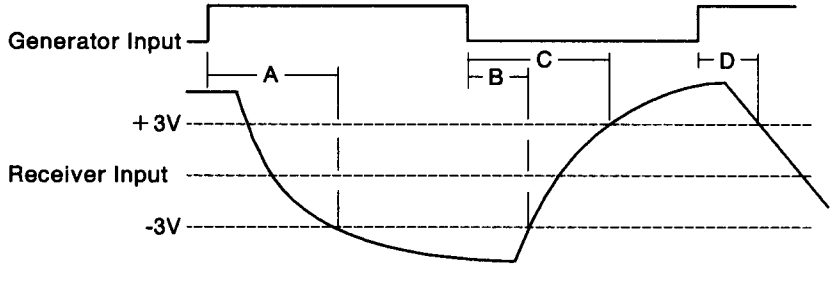
The attached equipment should meet the following requirements:

- The capacitance for an input or output signal should be less than or equal to 120 picofarads.
- The timing oscillator accuracy is ±.01%.
- The maximum generator skew equals 970 nanoseconds with the cable attached and a capacitive load (including cable) between 100 and 690 picofarads.
- The maximum receiver skew equals 160 nanoseconds.
- The receiver deserializer should decode the data stream by sampling a minimum of 16 times per unit interval such as is done in the NS8250 and similar Universal Asynchronous Receive Transmitters (UARTs).

In order to specify the maximum distortion in the signals, the concept of skew is introduced. The receiver skew is defined as the worst case difference in delay between the rising and falling edges from a 12V peak-to-peak (P-P) square wave connected to the input of the receiver to when it reaches the deserializer. For example, if the rising edge delay is 200 nanoseconds and the falling edge delay is 120 nanoseconds then the skew is 200 nanoseconds minus 120nanoseconds, which equals 80 nanoseconds. The 80 nanoseconds is well within the 160nS requirement.

The generator skew is measured using the sending serializer to generate a square wave and measuring the delays at the input of an attached receiver with the cable and all capacitive loadings (690 picofarad maximum) included.

The generator waveforms graphic shown below illustrates where the measurements are taken. The generator skew is A-B or C-D, whichever is larger.

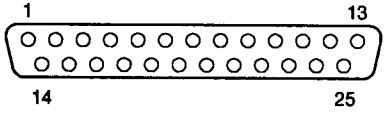


Generator Waveforms

Connectors

The hardware interface uses the standard 25-pin and 9-pin male D-shell connectors with pin assignments defined for EIA-232-D. The voltage levels are EIA-232-D only. Current loop interface is not supported.

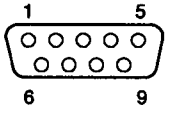
Figures 36 and 37 show the pin configurations and signal assignments for the serial port.



Pin No.	Signal Name	Pin No.	Signal Name
1	Not Connected	14	Not Connected
2	Transmit Data	15	Not Connected
3	Receive Data	16	Not Connected
4	Request to Send	17	Not Connected
5	Clear to Send	18	Not Connected
6	Data Set Ready	19	Not Connected
7	Signal Ground	20	Data Terminal Ready
8	Data Carrier Detect	21	Not Connected
9	Not Connected	22	Ring Indicator
10	Not Connected	23	Not Connected
11	Not Connected	24	Not Connected
12	Reserved	25	Not Connected
13	Not Connected		

Figure 36. Serial Port Connector Signal and Pin Assignments (25-Pin)

Figures 38 below shows the pin configuration and signal assignments for the serial port.



Pin No.	Signal Name
1	Data Carrier Detect
2	Receive Data
3	Transmit Data
4	Data Terminal Read
5	Signal Ground
6	Data Set Ready
7	Request To Send
8	Clear To Send
9	Ring Indicator

Figure 37. Serial Port Connector Signal and Pin Assignments (9-Pin)

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