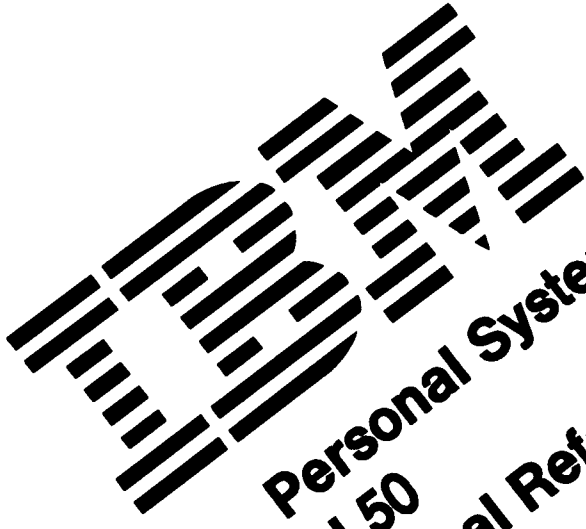

Personal System/2
Model 50
Technical Reference

Third Edition (October 1990)

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Preface

This technical reference contains hardware and software interface information specific to the IBM Personal System/2 Model 50 computer. It is intended for those who develop hardware and software products for these systems. Users should understand computer architecture and programming concepts.

This publication consists of the following sections:

Section 1, "System Overview," describes the system, features and specifications.

Section 2, "Programmable Option Select," describes registers used for configuration.

Section 3, "System Board," describes the system specific hardware implementations.

This technical reference should be used with the following publications:

IBM Personal System/2 Hardware Interface Technical Reference — Architectures

IBM Personal System/2 Hardware Interface Technical Reference — Common Interfaces

IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference

These publications contain additional information on many of the subjects discussed in this technical reference.

Warning: The term "Reserved" describes certain signals, bits, and registers that should not be changed. Use of reserved areas can cause compatibility problems, loss of data, or permanent damage to the hardware. When the contents of a register are changed, the state of the reserved bits must be preserved. When possible, read the register first and change only the bits that must be changed.

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Section 1. System Overview

Notes:

Description

The IBM* Personal System/2* Model 50 computer is a self-contained, desktop system that features the Micro Channel* architecture. This system can support two diskette drives and one internal fixed disk drive and comes with a keyboard.

A system can have either a Type 1 or Type 2 system board. The major differences between the system boards are component layout, the maximum amount of system board memory, and the processor performance. Programs identify the type by reading the model and submodel bytes and BIOS revision code. Interrupt hex 15, function code (AH) = hex C0, returns the model and submodel bytes and BIOS revision code. The following figure shows these bytes and the system board types.

Model Byte	Submodel Byte	Revision Code	System Board
FC	04	00	Type 1
FC	04	03	Type 2

Figure 1-1. Model and Submodel Bytes

System Board Features

The following figure lists the system board devices and features. The Hardware Interface Technical Reference manuals describe devices common to PS/2* products by type number.

* IBM, Personal System/2, PS/2, and Micro Channel are trademarks of the International Business Machines Corporation.

Device	Type	Features
Microprocessor	---	80286 24-bit address and 16-bit data interface
System Timers	1	Channel 0 – System timer Channel 2 – Tone generation for speaker Channel 3 – Watchdog timer
ROM Subsystem	---	128KB (KB = 1024 bytes)
RAM Subsystem	---	Type 1 - 1MB on the system board (MB = 1,048,576 Bytes) Type 2 - 1MB or 2MB on the system board
CMOS RAM Subsystem	---	64-byte CMOS RAM with real-time clock/calendar Battery backup
Video Subsystem	1	Auxiliary connector on the channel Analog output 256KB video memory
Audio Subsystem	1	Driven by: - System-timer channel 2 - The 'audio sum node' signal.
DMA Controller	1	Eight independent DMA channels Single or burst transfers and read verification
Interrupt Controller	1	16 levels of system interrupts Interrupts are level-sensitive
Keyboard/Auxiliary Device Controller	1	Keyboard connector Auxiliary device connector Password security
Diskette Drive Controller	1	Supports: - 720KB formatted diskette density - 1.44MB formatted diskette density.
Serial Controller	1, 2*	RS-232C interface Programmable as serial port 1 or 2
Parallel Controller	1	Programmable as parallel port 1, 2, or 3 Supports bidirectional input and output
Micro Channel	---	Four channel connectors for Type 3 adapters: - 8- or 16-bit device support - One with an auxiliary video extension - One occupied by the fixed disk drive adapter
Math Coprocessor Socket	---	Supports 80287 math coprocessor Same clock speed as the system microprocessor

* The Model 50 does not support the FIFO mode.

Figure 1-2. System Board Devices and Features

System Board Block Diagram

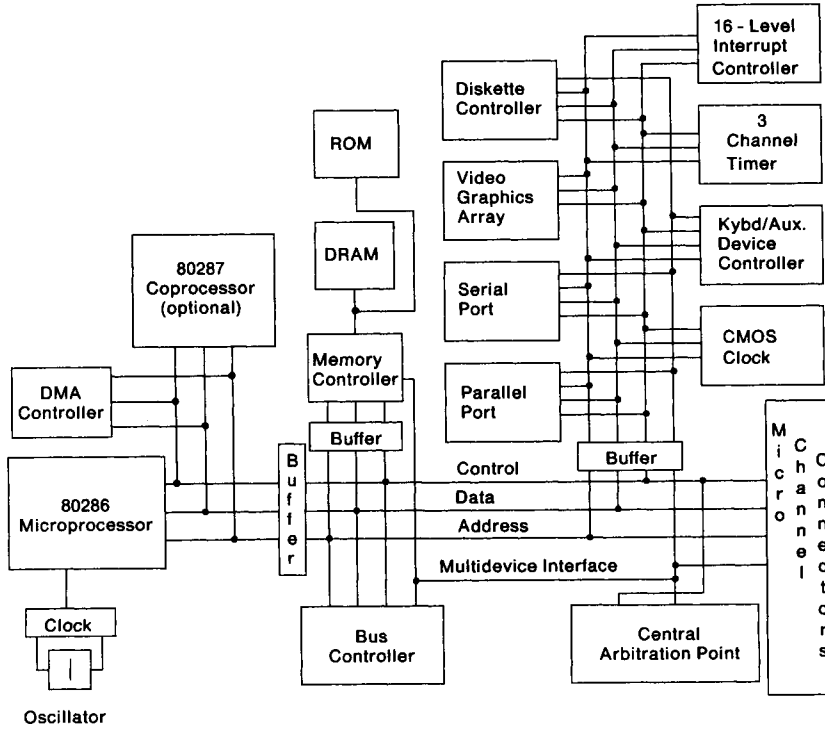

Figure 1-3. System Board

System Board I/O Address Map

Hex Addresses	Device
0000 - 001F	DMA Controller (0 – 3)
0020, 0021	Interrupt Controller (Master)
0040, 0042 - 0044, 0047	System Timers
0060	Keyboard, Auxiliary Device
0061	System Control Port B
0064	Keyboard, Auxiliary Device
0070, 0071	RT/CMOS and NMI Mask
0081 - 0083, 0087	DMA Page Registers (0 – 3)
0089, 008A, 008B, 008F	DMA Page Registers (4 – 7)
0090	Central Arbitration Control Point
0091	Card Selected Feedback Register
0092	System Control Port A
0094	System Board Enable/Setup Register
0096	Adapter Enable/Setup Register
00A0 - 00A1	Interrupt Controller (Slave)
00C0 - 00DF	DMA Controller (4 – 7)
00F0 - 00FF	Math Coprocessor
0100 - 0107	Programmable Option Select
01F0 - 01F8	Fixed Disk Drive Controller
0278 - 027B	Parallel Port 3
02F8 - 02FF	Serial Port 2 (RS-232C)
0378 - 037B	Parallel Port 2
03B4, 03B5, 03BA	Video Subsystem
03BC - 03BF	Parallel Port 1
03C0 - 03C5	Video Subsystem
03C6 - 03C9	Video DAC
03CA, 03CC, 03CE, 03CF	Video Subsystem
03D4, 03D5, 03DA	Video Subsystem
03F0 - 03F7	Diskette Drive Controller
03F8 - 03FF	Serial Port 1 (RS-232C)

Figure 1-4. System Board I/O Address Map

Specifications

The following figure describes the Type 1 system board performance.

Device	Number of Waits	Cycle Time (ns)
Microprocessor (10 MHz – 100 ns Clock):		
Access to System Board RAM	1	300
Access to System Board ROM	1	300
Access to Channel:		
Default Transfer Cycle:		
I/O Access	1	300
Memory Access	0	200
Synchronous Extended Transfer Cycle	1	300
Refresh Rate (Typically performed every 15.1 μs)		500 (min)
Bus Master Access to System Board RAM		300 (min)
DMA Controller (10 MHz – 100 ns Clock):		
Single Transfer: 300 + I/O Access + Memory Access		
Burst Transfers: 300 + (I/O Access + Memory Access)N*		
System Board Memory Access		300
Default Transfer Cycle:		
I/O Access		300
Memory Access		200
Synchronous Extended Transfer Cycle		300

* N is the number of transfers in the burst.

Figure 1-5. Performance Specifications – Type 1 System Board

The following figure describes the Type 2 system board performance. The Type 2 system board supports two speeds of system board memory. Cycle times differ depending upon the speed. See Figure 3-7 on page 3-11.

Device	Number of Waits	Cycle Time (ns)
Microprocessor (10 MHz – 100 ns Clock):		
Access to System Board RAM:		
85-ns Memory	0	200
120-ns Memory	1	300
Access to System Board ROM	1	300
Access to Channel:		
Default Transfer Cycle:		
I/O Access	1	300
Memory Access	0	200
Synchronous Extended Transfer Cycle	1	300
Refresh Rate (Typically performed every 15.1 μs)		500 (min)
Bus Master Access to System Board RAM		300 (min)
DMA Controller (10 MHz – 100 ns Clock):		
Single Transfer: 300 + I/O Access + Memory Access		
Burst Transfers: 300 + (I/O Access + Memory Access)N*		
System Board Memory Access		
85-ns Memory		200
120-ns Memory		300
Default Transfer Cycle:		
I/O Access		300
Memory Access		200
Synchronous Extended Transfer Cycle		300

* N is the number of transfers in the burst.

Figure 1-6. Performance Specifications – Type 2 System Board

The following figure describes the physical specifications of the system.

Size:	
Width	360 mm (14.1 in)
Depth	420 mm (16.5 in)
Height	140 mm (5.5 in)
Weight	9.55 kg (21 lb)
Cables:	
Power Cable	1.8 m (6 ft)
Keyboard Cable	1.8 m (6 ft)
Air Temperature:	
System On	15.6 to 32.2°C (60 to 90°F)
System Off	10.0 to 43.0°C (50 to 110°F)
Humidity:	
System On	8% to 80%
System Off	8% to 80%
Maximum Altitude	2133.6 m (7000 ft)
Heat Output	150 Watts(512 BTUs/hour)
Acoustical Readings	(See Figure 1-8 on page 1-10)
Electrical Input:	
Input Voltage (Range is automatically selected; sinewave input is required):	
Low Range	90 (min) – 137 (max) Vac
High Range	180 (min) – 265 (max)Vac
Frequency:	
Low Range	47 (min) – 53 (max) Hz
High Range	57 (min) – 63 (max) Hz
Input in Kilovolt-Ampere (kVA):	
Minimum configuration (as shipped by IBM)	0.11 kVA
Maximum configuration	0.25 kVA
Electromagnetic Compatibility	FCC Class B

Figure 1-7. Physical Specifications

The following figure describes the acoustical readings of the system.

Description	L_{WAd} in bels Operate	Idle	L_{pAm} in dB Operate	Idle	$<L_{pA}>_m$ in dB Operate	Idle
Model 50	5.1	5.1	41	40	38	37

Notes:

L_{WAd} is the declared sound power level for the random sample of machines.

L_{pAm} is the mean value of the A-weighted sound pressure levels at the operator position (if any) for the random sample of machines.

$<L_{pA}>_m$ is the mean value of the A-weighted sound pressure levels at the one-meter positions for the random sample of machines.

All measurements made in accordance with ANSI S12.10, and reported in conformance with ISO DIS 9296.

The measurements are preliminary data and subject to change.

Figure 1-8. Acoustical Readings

Power Supply

The power supply requires a sinewave input and converts the ac input voltage to three dc output voltages. The power supply provides power for the following:

- System board
- Channel adapters
- Internal diskette drives
- Internal fixed disk drives
- Auxiliary device
- Keyboard.

The power switch and one light-emitting diode (LED) is on the front of the system unit. The power supply is operating when the LED is lit.

Outputs

The power supply provides separate voltage sources for the system board and the drives. The system-board voltages are +5 Vdc, +12 Vdc, and −12 Vdc. The drive voltages are +5 Vdc and +12 Vdc. The following is a list of the approximate power provided for system components.

System Component	Maximum Current	
	+12 Vdc	+5 Vdc
Auxiliary Device	None	300 mA
Keyboard	None	275 mA

Figure 1-9. Component Maximum Current

The following are the load currents allowed for each Micro Channel connector.

Supply Voltage	Maximum Current
+ 5.0 Vdc	1.6 A
+12.0 Vdc	0.175 A
−12.0 Vdc	0.040 A

Figure 1-10. Channel Load Current

The formulas used to determine the power requirements and the voltage regulation tolerances are in the Micro Channel adapter design information in the *Hardware Interface Technical Reference - Architectures* manual.

Output Protection

A short circuit placed on any dc output (between outputs or between an output and dc return) latches all dc outputs into a shutdown state with no damage to the power supply.

If an overvoltage fault occurs (internal to the power supply), the power supply latches all dc outputs into a shutdown state before any output exceeds 130% of its nominal value.

If either of these shutdown states is actuated, the power supply returns to normal operation only after the fault has been removed and the power switch has been turned off for at least ten seconds.

Voltage Sequencing

At power-on time, the output voltages track within 50 milliseconds of each other when measured at the 50% points.

Section 2. Programmable Option Select

Notes:

Description

Programmable Option Select (POS) eliminates the need for switches by replacing their function with programmable registers. This section describes the POS information used specifically by the Model 50 system board. For additional POS information, refer to the Hardware Interface Technical Reference Micro Channel architecture information.

Warning:

- IBM recommends that programmable options be set only through the System Configuration utilities. Directly setting the POS registers or CMOS RAM POS parameters can cause multiple assignment of the same system resource, improper operation of the feature, loss of data, or possible damage to the hardware.
- Application programs should not use the adapter identification (ID) unless absolutely necessary. Compatibility problems can result.
- If an adapter and the system board are in setup mode at the same time, bus contention will occur, no useful programming can take place, and damage to the hardware can occur.
- After setup operations are complete, the Adapter Enable/Setup register (hex 0096) should be set to hex 00, and the System Board Enable/Setup register (hex 0094) should be set to hex FF.
- The channel reset bit (bit 7) in the Adapter Enable/Setup register must be 0 to program the adapters.
- The system board does not support 16-bit I/O operations to 8-bit POS registers. Using 16-bit I/O instructions on 8-bit POS registers will cause erroneous data to be written to or read from the registers. Only 8-bit transfers are supported for setup operations.

Setup functions respond to I/O addresses hex 0100 through 0107 only when their unique setup signal is active. The following precautions must be taken before setting individual bits in the POS registers.

System Board Video Subsystem Setup:

- Bit 5 in the System Board Enable/Setup register (hex 0094) must be set to 0 to place the system board video into the setup mode.
- Bit 3 in the Adapter Enable/Setup register (hex 0096) must be set to 0 to avoid driving a 'setup' signal to an adapter.
- Bit 7 in the System Board Enable/Setup register (hex 0094) must be set to 1 to avoid driving a 'setup' signal to other system board functions.

Adapter Setup:

- Bit 3 in the Adapter Enable/Setup register (hex 0096) must be set to 1 to allow adapter setup.
- Bit 5 in the System Board Enable/Setup register (hex 0094) must be set to 1 to avoid driving a 'setup' signal to the Video Subsystem.
- Bit 7 in the System Board Enable/Setup register (hex 0094) must be set to 1 to avoid driving a 'setup' signal to a system board function.

Other System Board Setup:

- Bit 7 in the System Board Enable/Setup register (hex 0094) must be set to 0 to allow setup of other system board functions.
- Bit 3 in the Adapter Enable/Setup register (hex 0096) must be set to 0 to avoid driving a 'setup' signal to an adapter.
- Bit 5 in the System Board Enable/Setup register (hex 0094) must be set to 1 to avoid driving a 'setup' signal to the Video Subsystem.

POS Address Map

The following figure shows the organization of the I/O address space used by POS. The POS registers are 8-bit registers. Bit 0 of POS Register 2 and bits 6 and 7 of POS Register 5 are defined. All other bits in POS Registers 2 through 5 are free-form.

Address (Hex)	Function
0094	System Board Enable/Setup Register
0096	Adapter Enable/Setup Register
0100	POS Register 0 – Adapter Identification Byte (Low Byte)
0101	POS Register 1 – Adapter Identification Byte (High Byte)
0102	POS Register 2 – Option Select Data Byte 1 Bit 0 is Card Enable.
0103	POS Register 3 – Option Select Data Byte 2
0104	POS Register 4 – Option Select Data Byte 3
0105	POS Register 5 – Option Select Data Byte 4 Bit 7 is the channel check active indicator. Bit 6 is the channel check status-available indicator.
0106	Reserved
0107	Reserved

Figure 2-1. POS I/O Address Map

Card Selected Feedback

When the adapter is addressed, it responds by setting the '-card selected feedback' signal (-CD SFDBK) to active. -CD SFDBK is derived from the address decode and driven by a totem pole driver. It is latched by the system board and can be read through the Card Selected Feedback register at address hex 0091. Diagnostic and automatic configuration programs use this signal to verify the operation of an adapter at a given address or DMA port. This signal must not be active during a setup cycle.

The Card Selected Feedback register is a read-only register at address hex 0091. It allows programs to monitor -CD SFDBK and thereby determine if the video subsystem, system board I/O, or an adapter is addressed and functioning.

Bit	Function
7 - 1	Reserved
0	-Card Selected Feedback

Figure 2-2. Card Selected Feedback Register (Hex 0091)

Bits 7 - 1 Reserved.

Bit 0 This bit is set to 1 whenever -CD SFDBK was active on a previous cycle or whenever the system board I/O functions (diskette drive, serial, or parallel interfaces) are accessed by an I/O cycle. Reading this register resets the bit to 0.

System Board Setup

The integrated I/O functions on the system board use POS information during setup. The diskette drive controller, serial port, and parallel port are treated as a single device. The video subsystem is also an integrated part of the system board; however, POS treats it as a separate device. The System Board Enable/Setup register is used to place the system board or video subsystem into the setup mode.

System Board Enable/Setup Register (Hex 0094)

This is a read/write register; all bits in this register default to 1 (enabled).

Bit	Function
7	Enable/-Setup System Board Functions
6	Reserved
5	Enable/-Setup Video Subsystem
4 - 0	Reserved

Figure 2-3. System Board Enable/Setup Register (Hex 0094)

Bit 7 When this bit is set to 0, various system board I/O functions are placed in the setup mode. The diskette drive controller, serial port, and parallel port are controlled through System Board POS Register 2 (hex 0102). The memory is controlled through System Board POS Register 3 (hex 0103).

When this bit is set to 1, the system board functions are enabled.

Bit 6 Reserved.

Bit 5 When this bit is set to 0, the video subsystem is placed in the setup mode and controlled through POS Register 2 (hex 0102). When set to 1, and bit 0 in hex 0102 is set to 1, video is enabled.

Bit 0 of POS Register 2 is the video enable bit. When this bit is set to 0, the video subsystem does not respond to commands, addresses, or data. If video is being generated when the video enable bit is set to 0, the output is still generated. For information on BIOS calls to enable or disable the video, see the *IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference*.

Note: When the video is disabled, access to the video DAC registers is disabled.

Bits 4 - 0 Reserved.

System Board POS Register 2 (Hex 0102)

When the system board is in the setup mode, the diskette drive controller, serial port, and parallel port are controlled by this read/write register. Reading this register returns the current state of these system board functions.

Bit	Function
7	Disable Parallel Port Extended Mode
6, 5	Parallel Port Select
4	Enable Parallel Port
3	Serial Port Select
2	Enable Serial Port
1	Enable Diskette Drive Interface
0	Enable System Board

Figure 2-4. System Board POS Register 2 (Hex 0102)

Bit 7 When set to 0, this bit allows the parallel port to be configured as an 8-bit, parallel, bidirectional interface. When set to 1, this bit disables the bidirectional mode. This bit is set to 0 at power-on, and POST sets it to 1.

Bits 6, 5 These bits select the configuration of the system board parallel port.

Bits 6 5	Assignment	Hex Address	Interrupt Level
0 0	Parallel 1	03BC - 03BF	7
0 1	Parallel 2	0378 - 037B	7
1 0	Parallel 3	0278 - 027B	7
1 1	Reserved	----------	-

Figure 2-5. Parallel Port Select Bits

Bit 4 When this bit and bit 0 are set to 1, the system board parallel port is enabled.

Bit 3 When set to 1, this bit sets the system board serial port as Serial 1 (addresses hex 03F8 through 03FF), which uses interrupt level 4. When set to 0, this bit sets the serial port as Serial 2 (addresses hex 02F8 through 02FF), which uses interrupt level 3.

Bit 2 When this bit and bit 0 are set to 1, the system board serial port is enabled.

Bit 1 When this bit and bit 0 are set to 1, the diskette drive interface is enabled.

Bit 0 When set to 1, this bit allows bits 4, 2, and 1 to enable and disable their respective devices. When set to 0, this bit disables the diskette drive interface, system board serial port, and system board parallel port, regardless of the state of bits 4, 2, and 1.

System Board POS Register 3 (Hex 0103)

With the system board in setup, this register controls the system board memory.

Bit	Function
7 - 1	Reserved
0	Enable System Board RAM

Figure 2-6. System Board POS Register (Hex 0103)

Bit 7 - 1 Reserved.

Bit 0 When set to 1, this bit enables the system board memory. When set to 0, this bit disables the memory. All system board memory is enabled or disabled by this operation.

Adapter Enable/Setup Register (Hex 0096)

The Adapter Enable/Setup register selects the connector to be configured.

Bit	Symbol
7	Channel Reset
6 - 4	Reserved
3	Card Setup Enable
2 - 0	Channel Select 2 - 0

Figure 2-7. Adapter Enable/Setup Register (Hex 0096)

Bit 7 When set to 1, this bit activates the 'channel reset' signal to all connectors.

Bits 6 - 4 These bits are reserved.

Bit 3 When set to 1, this bit enables the '-card setup' signal selected by bits 2 through 0.

Bits 2 - 0 These bits are the address bits for the '-card setup' signal Connectors 1 through 4 are addressed as 0 through 3, respectively. When bit 3 is set to 1, these bits select the connector that is put into setup.

Each channel connector has a unique '-card setup' signal (-CD SETUP) associated with it. This signal is used to put the adapters in the setup mode, which allows access to the POS registers. The individual connectors are selected through the Adapter Enable/Setup register. Setup information is then read from or written to the selected adapter through I/O addresses hex 0100 through 0107.

Notes:

1. -CD SETUP goes active only when an operation is performed in the I/O address range hex 0100 through 0107.
2. The status of port hex 0096 can be read by software. However, when the port is read, bits 6, 5, and 4 are set to 1.

Section 3. System Board

Notes:

Description

This section provides information about the Model 50 implementation of the Micro Channel, memory subsystem, and miscellaneous system ports. Additional information on these topics can be found in the Hardware Interface Technical Reference manuals listed in the preface of this manual.

Micro Channel Implementation

The POST routines and registers used to implement programmable features of the Micro Channel architecture may vary from system to system. This section provides information about the Model 50 implementation of the Micro Channel architecture.

Exception Reporting

Exceptions should be reported using the asynchronous channel check procedure. The synchronous channel check procedure is not supported.

Adapter Identification

When the system is powered on, an adapter can issue an ID of hex 0000 for up to 1 second after channel reset to indicate it is not ready. Any adapter that continues to issue an adapter ID of hex 0000 (not ready) for more than 1 second is considered defective. On the Model 50, if the channel reset was caused by a keyboard sequence or a program routine, this time is reduced to 740 milliseconds.

Central Arbiter

The central arbitration control point gives intelligent subsystems on the channel the ability to share and control the system. It allows burst data transfers and prioritization of control between devices. This arbiter supports up to 16 arbitrating devices.

Arbitration Bus Priority Assignments

The following figure shows the assignment of arbitration levels. The functions with the lowest arbitration level have the highest priority.

ARB Level	Primary Assignment
-2	Memory Refresh
-1	NMI
0	DMA Channel 0 (Programmable to any arbitration level)
1	DMA Channel 1
2	DMA Channel 2
3	DMA Channel 3
4	DMA Channel 4 (Programmable to any arbitration level)
5	DMA Channel 5
6	DMA Channel 6
7	DMA Channel 7
8-E	Available
F	System Microprocessor

Figure 3-1. Arbitration Bus Priority Assignments

Note: Devices designed for arbitration level 0 or 1 should have limited bandwidth or short bursts so diskette overruns can be prevented or recovered by retry operations. The diskette drive controller, on arbitration level 2, can be held inactive by devices on levels 0 and 1, by a refresh operation, and by the previous controlling master. The diskette drive controller should not be held inactive for more than 12 microseconds to prevent overrun.

NMI service is executed at a priority level higher than 0, called -1. Memory refresh is prioritized at -2, two levels higher than 0. Levels -1 and -2 are reached on the system board only, while the 'arbitrate/-grant' signal (ARB/-GNT)) is in the arbitrate state.

When the central arbitration control point receives a level -1 request (NMI, a system-board internal signal), it activates -PREEMPT, waits for the end of transfer, and then places ARB/-GNT in the arbitrate state, which denies channel activity to arbitrating devices. The central arbitration control point gives the grant to the level -1 request, and holds ARB/-GNT in the arbitrate state until the operation is complete and the NMI is reset.

Central Arbiter Programming

The central arbitration control point provides access to programmable options through the Arbitration register, which is accessed at I/O address hex 0090. The bits are defined differently for read and write operations, as shown in the following figures.

Bit	Definition
7	Enable System Microprocessor Cycle
6	Arbitration Mask
5	Enable Extended Arbitration
4 - 0	Reserved

Figure 3-2. Arbitration Register, Write to Hex 0090

Bit	Definition
7	Enable System Microprocessor Cycle
6	Arbitration Masked by NMI
5	Bus Time-out
4	Reserved
3 - 0	Value of Arbitration Bus During Previous Grant State

Figure 3-3. Arbitration Register, Read Hex 0090

Bit 7 Setting this bit to 1 enables system microprocessor cycles during arbitration cycles. This bit can be set to 0 if an arbitrating device requires total control of the channel bandwidth. This bit is set to 0 by a system reset.

Reading this bit as a 1 indicates system microprocessor cycles are enabled during arbitration.

Bit 6 Setting this bit to 1 causes the central arbitration control point to enter the arbitration state. The system microprocessor controls the channel until this bit is reset to 0. This bit is set to 0 by a system reset.

Reading this bit as a 1 indicates that an NMI has occurred and has masked arbitration.

Warning: This bit should be set to 1 only by diagnostic routines and system error-recovery routines.

Bit 5 Setting this bit to 1 enables extended arbitration. The minimum arbitration cycle is 300 nanoseconds; this bit extends that minimum cycle to 600 nanoseconds. This bit is set to 0 during a system reset.

Reading this bit as a 1 indicates that a bus time-out has occurred, and resets bit 6 in this register to 0.

Bit 4 This bit is reserved and should be 0.

Bits 3 - 0 These bits are undefined for a write operation and should be set to 0.

Reading these bits returns the arbitration level of the arbiter controlling the channel during the most recent grant state. This information allows the system microprocessor to determine the arbitration level of the device that caused a bus time-out.

Memory

The Model 50 system uses the following types of memory:

- Read-only memory (ROM)
- Random access memory (RAM)
- Real-time Clock and CMOS RAM.

Read-Only Memory Subsystem

The ROM subsystem on the Type 1 system board consists of four 32Kb by 8-bit modules in a 64Kb by 16-bit arrangement (Kb equals 1024 bits). The ROM subsystem on the Type 2 system board consists of two 64Kb by 8-bit modules in a 64Kb by 16-bit arrangement.

ROM is not parity-checked and is assigned addresses at the top of the first and last 1MB of address space (hex 0E0000 and FE0000).

Random Access Memory Subsystem

The RAM subsystem on the system board starts at address hex 000000 of the 16MB address space. It consists of 1MB of RAM modules.

The Type 1 system board uses two, 512KB by 9-bit memory module packages that operate with one wait state. The Type 2 system board supports the following memory module packages:

- 1MB, 120 nanosecond (one wait state)
- 1MB, 85 nanosecond (zero wait state)
- 2MB, 85 nanosecond (zero wait state).

Memory-refresh typically occurs once every 15 microseconds.

The timing of the memory signals on the Type 1 system board is similar to the Hitachi** HB61009BR-15, 150-nanosecond DRAM or equivalent.

** Hitachi is a trademark of the Hitachi Corporation.

The timing of the memory signals on the Type 2 system board with 85-nanosecond memory installed is similar to the Hitachi HM51256CP-8, 85-nanosecond DRAM or equivalent. The timing of the memory signals on the Type 2 system board with 120-nanosecond memory installed is similar to the Hitachi HM51256CP-12, 120-nanosecond DRAM or equivalent.

System Memory Maps

The following figure shows the mapping of the memory locations on the Model 50. A 256-byte portion of this RAM is reserved as a BIOS data area. A 1KB portion of this RAM is reserved as an extended BIOS data area. See the *IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference* for details.

Hex Range	Function
000000 to 09FFFF	640KB System Board RAM *
0A0000 to 0BFFFF	128KB Video RAM
0C0000 to 0DFFFF	128KB I/O Expansion ROM
0E0000 to 0FFFFF	128KB System Board ROM
100000 to 15FFFF	384KB System Board RAM
160000 to FDFFFF	Channel Expansion Memory Addresses
FE0000 to FFFFFF	128KB System Board ROM

* With the system board in the setup mode, the system board memory can be disabled through System Board POS Register 3 (see page 2-9).

Figure 3-4. System Memory Map

System Board Memory Connector

The Type 1 and 2 system boards use different types of memory connectors. The Type 1 system board has two 30-pin connectors and comes with two 512KB memory module packages installed. The Type 2 system board has one 72-pin connector and comes with one 1MB memory module package installed. The following figures show the pin assignments and signal definitions for these connectors.

Pin	I/O	Signal	Pin	I/O	Signal
1	N/A	5 Vdc	2	I	-Column Address Strobe
3	I/O	Data Bit 1	4	I	Address Bit 1
5	I	Address Bit 2	6	I/O	Data Bit 2
7	I	Address Bit 3	8	I	Address Bit 4
9	N/A	Ground	10	I/O	Data Bit 3
11	I	Address Bit 5	12	I	Address Bit 6
13	I/O	Data Bit 4	14	I	Address Bit 7
15	I	Address Bit 8	16	I/O	Data Bit 5
17	I	Address Bit 9	18	N/A	No Connection
19	I	Row Address Strobe 1	20	I/O	Data Bit 6
21	I	-Write Strobe	22	N/A	Ground
23	I/O	Data Bit 7	24	O	Presence Detect
25	I/O	Data Bit 8	26	O	Presence Detect
27	I	Row Address Strobe	28	N/A	No Connection
29	I/O	Data Bit 9 (Parity)	30	N/A	+5 Vdc

Figure 3-5. System Board Memory Connector, Type 1

Type 2 Memory Connector

Pin	I/O	Signal	Pin	I/O	Signal
1	N/A	Ground	37	I/O	Parity Data 1
2	I/O	Data 0	38	I/O	Parity Data 3
3	I/O	Data 16	39	N/A	Ground
4	I/O	Data 1	40	O	Column Address Strobe 0
5	I/O	Data 17	41	O	Column Address Strobe 2
6	I/O	Data 2	42	O	Column Address Strobe 3
7	I/O	Data 18	43	O	Column Address Strobe 1
8	I/O	Data 3	44	O	Row Address Strobe 0
9	I/O	Data 19	45	O	Row Address Strobe 1
10	O	+5 Vdc	46	O	Block Select 1
11	O	-Column Address Strobe P	47	O	Write Enable
12	O	Address 0	48	N/A	Reserved
13	O	Address 1	49	I/O	Data 8
14	O	Address 2	50	I/O	Data 24
15	O	Address 3	51	I/O	Data 9
16	O	Address 4	52	I/O	Data 25
17	O	Address 5	53	I/O	Data 10
18	O	Address 6	54	I/O	Data 26
19	N/A	Reserved	55	I/O	Data 11
20	I/O	Data 4	56	I/O	Data 27
21	I/O	Data 20	57	I/O	Data 12
22	I/O	Data 5	58	I/O	Data 28
23	I/O	Data 21	59	O	+5 Vdc
24	I/O	Data 6	60	I/O	Data 29
25	I/O	Data 22	61	I/O	Data 13
26	I/O	Data 7	62	I/O	Data 30
27	I/O	Data 23	63	I/O	Data 14
28	O	Address 7	64	I/O	Data 31
29	O	Block Select 0	65	I/O	Data 15
30	O	+5 Vdc	66	O	Block Select 2
31	O	Address 8	67	I	Presence Detect 0
32	N/A	Reserved	68	I	Presence Detect 1
33	O	Row Address Strobe 3	69	I	Presence Detect 2
34	O	Row Address Strobe 2	70	I	Presence Detect 3
35	I/O	Parity Data 2	71	O	Block Select 3
36	I/O	Parity Data 0	72	N/A	Ground

Figure 3-6. System Board Memory Connector, Type 2

The 'presence detect' signals are used by the system to determine memory card size and memory speed. The pins are either connected to ground (G) or not connected (N). The following table shows those combinations supported by Model 50.

Type of Memory Module Package	Presence Detect Signals			
	0	1	2	3
1 MB Memory at 120 ns	G	N	N	N
1 MB Memory at 85 ns	G	N	N	G
2 MB Memory at 85 ns	N	G	N	G

Figure 3-7. Presence Detect Encoding

Real-Time Clock/Complementary Metal-Oxide Semiconductor RAM

The real-time clock/complementary metal-oxide semiconductor RAM (RT/CMOS) chip contains the real-time clock and 64 bytes of CMOS RAM. The internal clock circuitry uses 14 bytes of this memory, and the rest is allocated to configuration and system status information.

A 6-Vdc lithium battery maintains voltage to the RT/CMOS RAM when the power supply is not in operation.

The system cover can be locked to prevent battery removal and loss of password and configuration information.

The following figure shows the RT/CMOS RAM bytes and their addresses.

Address (Hex)	RT/CMOS RAM Bytes
000 - 00D	Real-Time Clock Bytes
00E	Diagnostic Status Byte
00F	Shutdown Status Byte
010	Diskette Drive Type Byte
011	First Fixed Disk Drive Type Byte
012	Second Fixed Disk Drive Type Byte
013	Reserved
014	Equipment Byte
015 - 016	Low and High Base Memory Bytes
017 - 018	Low and High Expansion Memory Bytes
019 - 031	Reserved
032 - 033	Configuration CRC Bytes
034	Reserved
035 - 036	Low and High Useable Memory Bytes
037	Date Century Byte
038 - 03F	Reserved

Figure 3-8. RT/CMOS RAM Address Map

RT/CMOS Address Register and NMI Mask (Hex 0070)

This register is used in conjunction with the port at hex 0071 to read and write the RT/CMOS RAM bytes.

Bit	Function
7	NMI Mask
6	Reserved
5 - 0	RT/CMOS RAM Address

Figure 3-9. RT/CMOS Address Register and NMI Mask (Hex 0070)

Warning: The operation following a write to hex 0070 should access port hex 0071; otherwise intermittent malfunctions and unreliable operation of the RT/CMOS RAM can occur.

Bit 7 When this bit is set to 1, the NMI is masked off (the NMI is disabled). This bit is set to 1 by a power-on reset and is a write-only bit.

Bit 6 Reserved.

Bits 5 - 0 These bits are used to select RT/CMOS RAM addresses.

RT/CMOS Data Register (Hex 0071)

This port is used in conjunction with the address register at hex 0070 to read and write the RT/CMOS RAM bytes.

Bit	Function
7 - 0	RT/CMOS Data

Figure 3-10. RT/CMOS Data Register (Hex 0071)

RT/CMOS RAM I/O Operations

During I/O operations to the RT/CMOS RAM addresses, interrupts should be masked to prevent other interrupt service routines from changing the CMOS address register before data is read or written. After I/O operations, the RT/CMOS and NMI Mask register (hex 0070) should be left pointing to Status Register D (hex 00D).

Warning: The operation following a write to hex 0070 should access hex 0071; otherwise intermittent malfunctions and unreliable operation of the RT/CMOS RAM can occur.

The following steps are required to perform I/O operations to the RT/CMOS RAM addresses:

1. Write the RT/CMOS RAM address to the RT/CMOS and NMI Mask register (hex 0070).
2. Write the data to address hex 0071.

Reading RT/CMOS RAM requires the following steps:

1. Write the RT/CMOS RAM address to the RT/CMOS and NMI Mask register (hex 0070).
2. Read the data from address hex 0071.

Real-Time Clock Bytes (Hex 000-00D)

Bit definitions and addresses for the real-time clock bytes are shown in the following figure.

Address (Hex)	Function	Byte Number
000	Seconds	0
001	Second Alarm	1
002	Minutes	2
003	Minute Alarm	3
004	Hours	4
005	Hour Alarm	5
006	Day of Week	6
007	Date of Month	7
008	Month	8
009	Year	9
00A	Status Register A	10
00B	Status Register B	11
00C	Status Register C	12
00D	Status Register D	13

Figure 3-11. Real-Time Clock Bytes

Note: The Setup program initializes status registers A, B, C, and D when the time and date are set. Interrupt hex 1A is the BIOS interface to read and set the time and date and it initializes the register the same way as the Setup program.

Status Register A (Hex 00A)

Bit	Function
7	Update in Progress
6 - 4	22-Stage Divider
3 - 0	Rate Selection Bits

Figure 3-12. Status Register A

Bit 7 When set to 1, this bit indicates the time-update cycle is in progress. When set to 0, it indicates the current date and time can be read.

Bits 6 - 4 These three divider-selection bits identify which time-base frequency is being used. The system initializes these bits to binary 010, which selects a 32.768 kHz time-base. This is the only value supported by the system for proper time-keeping.

Bits 3 - 0 These bits allow the selection of a divider output frequency. The system initializes the rate selection bits to a binary 0110, which selects a 1.024 kHz square-wave output frequency and a 976.562-microsecond periodic interrupt rate.

Status Register B (Hex 00B)

Bit	Function
7	Set
6	Periodic Interrupt Enable
5	Alarm Interrupt Enable
4	Update-Ended Interrupt Enabled
3	Square Wave Enabled
2	Date Mode
1	24-Hour Mode
0	Daylight Savings Enabled

Figure 3-13. Status Register B

Bit 7 When set to 0, this bit updates the cycle, normally by advancing the counts at a rate of one per second. When set to 1, this bit immediately ends any update cycle in progress, and the program can initialize the 14 time bytes without any further updates occurring until this bit is set to 0.

Bit 6 This bit is a read/write bit that allows an interrupt to occur at a rate specified by the rate and divider bits in Status Register A. When set to 1, this bit enables the interrupt. The system initializes this bit to 0.

Bit 5 When set to 1, this bit enables the alarm interrupt. The system initializes this bit to 0.

Bit 4 When set to 1, this bit enables the update-ended interrupt. The system initializes this bit to 0.

Bit 3 When set to 1, this bit enables the square-wave frequency as set by the rate-selection bits in Status Register A. The system initializes this bit to 0.

Bit 2 This bit indicates if the time-and-date calendar updates use binary or binary-coded-decimal (BCD) formats. When set to 1, this bit indicates a binary format. The system initializes this bit to 0.

Bit 1 This bit establishes if the hours byte is in the 24-hour or 12-hour mode. When set to 1, this bit indicates the 24-hour mode. The system initializes this bit to 1.

Bit 0 When set to 1, this bit enables the daylight savings time mode. When set to 0, it disables the mode, and the clock reverts to standard time. The system initializes this bit to 0.

Status Register C (Hex 00C)

Bit	Function
7	Interrupt Request Flag
6	Periodic Interrupt Flag
5	Alarm Interrupt Flag
4	Update-Ended Interrupt Flag
3 - 0	Reserved

Figure 3-14. Status Register C

Note: Interrupts are enabled by bits 6, 5, and 4 in Status Register B.

Bit 7 This bit is used in conjunction with bits 6, 5, and 4. When set to 1, this bit indicates that an interrupt has occurred; bits 6, 5, and 4 indicate the type of interrupt.

Bit 6 When set to 1, this bit indicates that a periodic interrupt occurred.

Bit 5 When set to 1, this bit indicates that an alarm interrupt occurred.

Bit 4 When set to 1, this bit indicates that an update-ended interrupt occurred.

Bits 3 - 0 Reserved.

Status Register D (Hex 00D)

Bit	Function
7	Valid RAM
6 - 0	Reserved

Figure 3-15. Status Register D

Bit 7 This read-only bit monitors the power-sense pin. A low state of this pin indicates a loss of power to the real-time clock (dead battery). When set to 1, this bit indicates that the real-time clock has power. When set to 0, it indicates that the real-time clock has lost power.

Bits 6 - 0 Reserved.

CMOS RAM Configuration

The following shows the bit definitions for the CMOS RAM configuration bytes.

Diagnostic Status Byte (Hex 00E)

Bit	Function
7	Real-Time Clock Chip Power
6	Configuration Record and Checksum Status
5	Incorrect Configuration
4	Memory Size Miscompare
3	Fixed Disk Controller/Drive C Initialization Status
2	Time Status Indicator
1	Adapter Configuration Miscompare
0	Adapter ID Time-Out

Figure 3-16. Diagnostic Status Byte

Bit 7 When set to 1, this bit indicates the real-time clock chip lost power.

Bit 6 When this bit is set to 1, the checksum is incorrect.

Bit 5 This is a check, at power-on time, of the Equipment byte. When set to 1, the configuration information is incorrect. Power-on checks require that at least one diskette drive be installed (bit 0 of the Equipment byte, hex 014, is set to 1).

Bit 4 When set to 1, this bit indicates the power-on check determined that the memory size is not the same as in the configuration record.

Bit 3 When set to 1, this bit indicates that the controller or drive C failed initialization, which prevents the system from attempting a power-on reset.

Bit 2 When set to 0, this bit indicates the time is valid. When set to 1, this bit indicates the time is invalid.

Bit 1 This bit indicates if the installed adapters match the configuration information. When this bit is set to 1, the adapters do not match the configuration information.

Bit 0 When set to 1, this bit indicates a time-out occurred while an adapter ID was being read.

Shutdown Status Byte (Hex 00F): This byte is defined by the power-on diagnostic programs.

Diskette Drive Type Byte (Hex 010): This byte indicates the type of diskette drive installed.

Bit	Function
7 - 4	First Diskette Drive Type
3 - 0	Second Diskette Drive Type

Figure 3-17. Diskette Drive Type Byte

Bits 7 - 4 These bits indicate the first diskette drive type, as shown in the following figure.

Bits 7 6 5 4	Function
0 0 0 0	No drive present
0 0 0 1	Double-sided diskette drive (48 tracks per inch, 360KB)
0 0 1 1	High-capacity diskette drive (720KB)
0 1 0 0	High-density diskette drive (1.44MB)

All combinations that are not shown are reserved.

Figure 3-18. Diskette Drive Type Byte (Bits 7 - 4)

Bits 3 - 0 These bits indicate the second diskette drive type, as shown in the following figure.

Bits 3 2 1 0	Function
0 0 0 0	No drive present
0 0 0 1	Double-sided diskette drive (48 tracks per inch, 360KB)
0 0 1 1	High-capacity diskette drive (720KB)
0 1 0 0	High-density diskette drive (1.44MB)

All combinations that are not shown are reserved.

Figure 3-19. Diskette Drive Type Byte (Bits 3 - 0)

First Fixed Disk Drive Type Byte (Hex 011): This byte defines the type of the first fixed disk drive (drive C). Hex 00 indicates that a fixed disk drive is *not* installed.

Second Fixed Disk Drive Type Byte (Hex 012): This byte defines the type of the second fixed disk drive (drive D). Hex 00 indicates that a fixed disk drive is *not* installed.

Note: For more information about fixed disk drive types, refer to the *IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference*.

Reserved Byte (Hex 013): This byte is reserved.

Equipment Byte (Hex 014): The equipment byte defines the basic equipment in the system for the power-on diagnostic tests.

Bit	Function
7, 6	Number of Diskette Drives
5, 4	Display Operating Mode
3, 2	Reserved
1	Math Coprocessor Presence
0	Diskette Drive Presence

Figure 3-20. Equipment Byte

Bits 7, 6 These bits indicate the number of diskette drives installed, as shown in the following figure.

Bits 7 6	Number of Diskette Drives
0 0	One Drive
0 1	Two Drives
1 0	Reserved
1 1	Reserved

Figure 3-21. Equipment Byte (Bits 7, 6)

Bits 5, 4 These bits indicate the operating mode of the display attached to the video port, as shown in the following figure.

Bits 5 4	Display Operating Mode
0 0	Reserved
0 1	40-Column Mode
1 0	80-Column Mode
1 1	Monochrome Mode

Figure 3-22. Equipment Byte (Bits 5, 4)

Bits 3, 2 Reserved.

Bit 1 When set to 1, this bit indicates that a math coprocessor is installed.

Bit 0 When set to 1, this bit indicates that a diskette drive is installed.

Low and High Base Memory Bytes (Hex 015 and 016): These bytes define the amount of memory below the 640KB address space.

The value from these bytes represents the number of 1KB blocks of base memory. For example, hex 0280 is equal to 640KB. The low byte is hex 15; the high byte is hex 16.

Low and High Expansion Memory Bytes (Hex 017 and 018): These bytes define the amount of memory above the 1MB address space.

The hexadecimal values in these bytes represent the number of 1KB blocks of expansion memory. For example, hex 0800 is equal to 2048KB. The low byte is hex 17; the high byte is hex 18.

Reserved Bytes (Hex 019 through 031): These bytes are reserved.

Configuration CRC Bytes (Hex 032 and 033): These bytes contain the cyclic-redundancy-check data for bytes hex 010 through hex 031 of the 64-byte CMOS RAM. The low byte is hex 33; the high byte is hex 32.

Reserved Byte (Hex 034): This byte is reserved.

Low and High Useable Memory Bytes (Hex 035 and 036): These bytes define the total amount of useable memory above the 1MB address space.

The hexadecimal values in these bytes represent the number of 1KB blocks of useable memory. For example, hex 0800 is equal to 2048KB. The low byte is hex 35; the high byte is hex 36.

Date Century Byte (Hex 037): Bits 7 through 0 of this byte contain the BCD value for the century. Refer to the *IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference* for information about reading and setting this byte.

Reserved Bytes (Hex 038 through 03F): These bytes are reserved.

Miscellaneous System Functions

Nonmaskable Interrupt

The nonmaskable interrupt (NMI) signals the system microprocessor that a parity error, a channel check, a system channel time-out, or a system Watchdog time-out has occurred. The NMI stops all arbitration on the bus until bit 6 of the Arbitration register (I/O address hex 0090) is set to 0. This can result in lost data or an overrun error on some I/O devices. The NMI masks all other interrupts and the IRET instruction restores the interrupt flag to the state it was in prior to the interrupt. A system reset causes a reset of the NMI.

Nonmaskable interrupt requests from system board parity and channel check are subject to mask control with the NMI mask bit in the RT/CMOS Address register. The Watchdog Timer and system channel time-out are not masked by this bit. (See "RT/CMOS RAM I/O Operations" on page 3-14). The power-on default of the NMI mask is 1 (NMI disabled). Prior to enabling the NMI after a power-on reset, the parity check and channel check state are initialized by the POST.

Warning: The operation following a write to hex 0070 should access port hex 0071; otherwise intermittent malfunctions and unreliable operation of the RT/CMOS RAM can occur.

System Control Port B (Hex 0061)

Bit definitions for the read and write functions of this port are shown in the following figures.

Bit	Function
7	Reset Timer 0 Output Latch (IRQ0)
6 - 4	Reserved
3	Enable Channel Check
2	Enable Parity Check
1	Speaker Data Enable
0	Timer 2 Gate to Speaker

Figure 3-23. System Control Port B (Write)

Bit	Function
7	Parity Check
6	Channel Check
5	Timer 2 Output
4	Toggle with Each Refresh Request
3	Enable Channel Check
2	Enable Parity Check
1	Speaker Data Enable
0	Timer 2 Gate to Speaker

Figure 3-24. System Control Port B (Read)

Bit 7 Setting this bit to 1 during a write operation, resets IRQ 0. When this port is read and this bit is set to 1, a parity check has occurred.

Bit 6 When this port is read and this bit is set to 1, a channel check has occurred.

Bit 5 When this port is read, this bit indicates the condition of the timer/counter 2 'output' signal.

Bit 4 When this port is being read, this bit toggles for each refresh request.

Bit 3 Setting this bit to 0 enables channel check. It is set to 1 during a power-on reset.

Bit 2 Setting this bit to 0 enables parity checking. This bit is set to 1 during a power-on reset.

Bit 1 Setting this bit to 1 enables speaker data. This bit is set to 0 during a power-on reset.

Bit 0 Setting this bit to 1 enables the timer 2 gate.

System Control Port A (Hex 0092)

Bit	Function
7, 6	Fixed Disk Activity Light
5	Reserved
4	Watchdog Timer Status
3	Security Lock Latch
2	Reserved
1	Alternate Gate A20
0	Alternate Hot Reset

Figure 3-25. System Control Port A (Hex 0092)

Bits 7, 6 These bits control the fixed-disk activity light. Setting either bit to 1 turns the fixed-disk activity light on. Setting both bits to 0 turns the light off. The power-on reset condition of each bit is 0.

Bit 5 Reserved.

Bit 4 This read-only bit indicates the Watchdog Timer status. When this bit is set to 1, a Watchdog time-out has occurred. For more information about the Watchdog Timer, refer to the *Hardware Interface Technical Reference — Architectures* manual.

Bit 3 This bit provides the security lock for the secured area of RT/CMOS. Setting this bit to 1 electrically locks the 8-byte, power-on password. Once this bit is set by POST, it can only be cleared by turning the system off.

Bit 2 Reserved.

Bit 1 This bit is used to enable the 'address 20' signal (A20) when the microprocessor is in the real address mode. When this bit is set to 0, A20 cannot be used in real mode addressing. This bit is set to 0 during a system reset.

Bit 0 This bit provides an alternate method of resetting the system microprocessor. This alternate method supports operating systems requiring faster operation than was provided on the IBM Personal Computer AT*. Resetting the system microprocessor is used to switch the microprocessor from the protected mode to the real address mode. The alternate reset takes 13.4 microseconds.

This bit is set to 0 either by a system reset or a Write operation. When a Write operation changes this bit from 0 to 1, the alternate reset pin is pulsed high for 100 to 125 nanoseconds. The reset occurs after a minimum delay of 6.72 microseconds. While the reset is occurring, the latch remains set so that POST can read this bit. If the bit is 0, POST assumes the system was just powered on. If the bit is 1, POST assumes a switch from the protected mode to the real mode has taken place.

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* Personal Computer AT is a trademark of the International Business Machines Corporation.

Power-On Password

RT/CMOS RAM has 8 bytes reserved for the power-on password and its check character. The 8 bytes are initialized to hex 00. The microprocessor can only access these bytes during power-on self-test (POST). After POST is completed, if a power-on password is installed, the password bytes are locked and cannot be accessed by a program. A power-on password can be from 1 to 7 characters.

During power-on password installation, the password (1 to 7 keyboard scan codes), is stored in the security space.

Power-on password installation is a function of a program contained on the Reference diskette. Once the power-on password utility has been installed, the password can be changed only during the POST. When the new power-on password is installed, changed, or removed, the password is not visible on the display.

The system unit cover can be physically locked to prevent unauthorized access to the battery. This helps prevent unauthorized battery removal and loss of power-on password and configuration information.

For information about the keyboard password, see the keyboard/auxiliary device controller information in the *Hardware Interface Technical Reference — Common Interfaces* manual.

Type 2 Serial Port Controller

The Model 50 does not support FIFO mode operations even if a Type 2 serial controller is installed. Do not enable FIFO operations if the model/submodel byte is hex FC/04.

The serial controller on some Type 2 system boards does not respond the same as other Personal System/2 products. After the initial transmitter-holding-register-empty interrupt, rewriting bit 1 of the Interrupt Enable register as a 1 will not reissue an interrupt. The interrupt is generated only when the Transmitter Holding register becomes empty.

Hardware Compatibility

The Model 50 maintains many of the interfaces used by the IBM Personal Computer AT. In most cases, command and status organization of these interfaces is maintained.

The functional interfaces for the Personal System/2 products are compatible with the following interfaces:

- The Intel** 8259 interrupt controllers (without edge triggering).
- The Intel 8253 timers driven from 1.193 MHz (timer 0 and 2 only).
- The Intel 8237 DMA controller-address/transfer counters, page registers and status fields only. The Command and Request registers are not supported. The rotate and mask functions are not supported. The Mode register is partially supported.
- Generally compatible with the NS16450 serial communications controller.
- The Intel 8088, 8086, and 80286 microprocessors.
- The Intel 8272 diskette drive controller.
- The Motorola** MC146818 Time of Day Clock command and status (CMOS reorganized).
- The Intel 8042 keyboard port at address hex 0060.
- Display modes supported by the IBM Monochrome Display and Printer Adapter, the IBM Color/Graphics Monitor Adapter, and the IBM Enhanced Graphics Adapter.

** Intel is a trademark of the Intel Corporation.

** Motorola is a trademark of Motorola, Incorporated.

- The parallel printer ports (Parallel 1, Parallel 2, and Parallel 3) in compatibility mode.
- Generally compatible with the Intel 80287 and 8087 math coprocessors.

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