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Stretchable temperature-sensing circuits with strain suppression based on carbon nanotube transistors

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For the next generation of wearable health monitors, it is essential to develop stretchable and conformable sensors with robust electrical performance. These sensors should, in particular, provide a stable electrical output without being affected by external variables such as induced strain. Here, we report circuit design strategies that can improve the accuracy and robustness of a temperature sensor based on stretchable carbon nanotube transistors. Using static and dynamic differential readout approaches, our circuits suppress strain-dependent errors and achieve a measured inaccuracy of only ±1 °C within a uniaxial strain range of 0–60%. We address device variability by using a one-time, single-point calibration approach. In contrast with previous approaches, which infer temperature change through a normalized measurement at two temperatures, our prototype devices provide an absolute output without temperature cycling. This is essential for practical deployment because heating and cooling the sensor is prohibitively slow and costly during real-time operation and production testing.

Stretchable electronics are of significant interest in the development of applications such as wearable/implantable physiological monitoring and stimulation[1–3], prostheses, soft robotics[4–6] and human–machine interfaces[7,8]. Among the core components of these systems are sensors that acquire physical quantities and accurately convert them into electronically processable outputs. Thus, there is a growing effort to develop stretchable sensors that can conformably adhere to human skin or tissue. While an ideal sensor would only be sensitive to the intended measurand, practical stretchable sensors often suffer from cross-sensitivities due to external parameters such as strain and/or other undesired physical inputs.

One possible approach for reducing such cross-sensitivities is to apply post-processing techniques to computationally infer the measurand from multiple inputs or sensors[9]. For our stretchable sensor, this approach would be challenging because the strain information is not easily accessible, and measuring it accurately poses its own instrumentation challenge. For this reason, we adopted a pre-processing approach using local conditioning and error-suppression circuits[9]. Although such signal-conditioning techniques are commonly used in rigid sensor systems[10–13], they have not been explored in stretchable circuits.

Body temperature is an important vital sign that provides useful diagnostic information. For example, an abnormal rise in body temperature can be correlated to inflammation and fever, and tracking the basal body temperature is frequently used for fertility awareness[1,14,15]. In addition to these epidermal sensor applications, implantable, subcutaneous temperature sensors are also of interest[16–18]. To enable comfortable and continuous measurements during movement, stretchable temperature sensors using a variety of structures and materials have been reported. Examples include stretchable thermistors with silver nanowire electrodes and graphene detection channels embedded in a polydimethylsiloxane (PDMS) matrix as the temperature responsive material[19], as well as all-elastomeric transistors with poly(3,4-ethylenedioxythiophene):poly(styrenesulfonate) (PEDOT:PSS) as electrodes and graphene oxide nanosheet channels in an elastomeric polyurethane (PU) matrix[20]. These stretchable sensor elements are typically characterized by a temperature coefficient that is also a relatively strong function of strain[21]. However, because the strain of the device is usually unknown, it is unclear how an accurate temperature measurement can be inferred from electrical measurements without an impractical calibration overhead. Consequently, an important next step in these developments is to devise a robust readout strategy that minimizes the cross-sensitivity to strain.

In this Article, we report circuit design strategies that enable strain suppression, and demonstrate stretchable temperature sensors without using any strain engineering, such as wrinkle buckling and rigid-island design[22,23], which either prevent close contact with the skin or decrease the device density. To achieve an accurate electrical output that represents temperature, we employed static and dynamic differential voltage readout schemes. The static differential sensing circuit achieves a sensitivity of −24.2 mV °C^{-1} in the temperature range of 15–55 °C and is thus applicable to ambient and body temperature readings. Using the dynamic approach, we obtain a tunable sensitivity in the range of −20.2 mV °C^{-1} to −41.7 mV °C^{-1}. The obtained sensing resolution is as high as 0.5 °C, and the circuit can be operated down to a supply voltage of 6 V. The absolute inaccuracy of the output is within ±1 °C for uniaxial strains from 0 to 60%.

Intrinsically stretchable transistors

An overview of our approach is provided in Fig. 1. A stretchable temperature sensor with a stretchable carbon nanotube transistor circuit is shown in Fig. 1a. Conformability is demonstrated by

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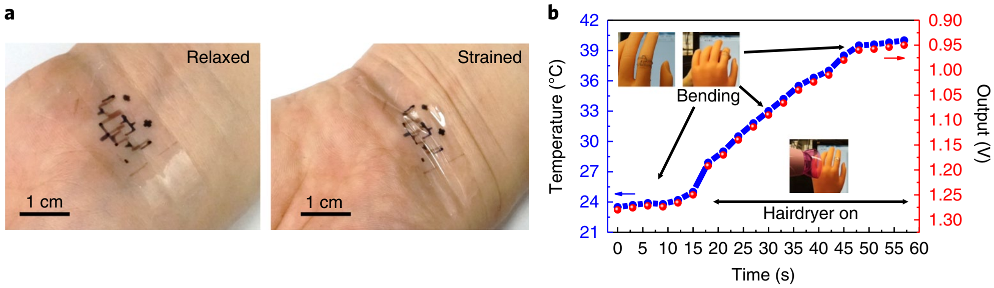

Fig. 1 | Stretchable integrated circuit for strain-independent temperature sensing. a, Optical photograph showing the conformability of the temperature-sensing circuit. The photograph highlights the skin-like nature of the intrinsically stretchable temperature sensor attached on the medial aspect of the wrist (left), and laminated to the skin during wrist bending (right). **b**, Demonstration of the stretchable temperature sensor attached to the knuckle area of a flexible rubber prosthetic hand. The temperature sensor showed stable functionality during repeated bending.

placing the sensor on the surface of the epidermis at the medial aspect of the wrist (Fig. 1a, left), and laminating it to the skin during wrist bending (Fig. 1a, right). To demonstrate the functionality of our stretchable temperature sensor circuit qualitatively, we conformably attached a sensor (with a dynamic differential circuit) to the knuckle of a flexible rubber prosthetic hand, and traced the sensor output as a function of temperature. We observed an increase in temperature as an operating hairdryer started to approach the temperature sensor. During the experiment, we repeatedly bent the finger, inducing a uniaxial strain of ~15% in the device, and observed negligible change in the temperature output, despite the resulting strains (Fig. 1b and Supplementary Video 1).

Stretchable thin-film transistors (TFTs) were developed and characterized for their mechanical and electrical performance. TFTs with a bottom-gate/top-contact structure (Fig. 2a) were fabricated on styrene-ethylene-butadiene-styrene (SEBS) hydrogenated elastomer as the substrate by a transfer and lamination method[24]. A nonpolar SEBS thin film served as the gate dielectric. Unsorted single-walled carbon nanotubes (SWCNTs) were photolithography-patterned as source–drain and gate electrodes, and supramolecular-polymer-sorted semiconducting SWCNTs were patterned as the semiconductor[25,26] (Supplementary Fig. 1). Scanning electron microscope (SEM) images from the stretchable sample (Fig. 2b) show dense unsorted SWCNT networks at the source–drain electrodes and thin-film SWCNTs in the channel region. Our previously reported stretchable conductor, PEDOT:PSS with ionic liquid, was used to create vias and interconnects by screen printing[27]. The devices were protected by a thin SEBS encapsulation layer. As described in previous work[27–29], all the materials in our devices have a similar Young's modulus and have high stretchability, which ensures a fully stretchable circuit without any stress concentrations. The static differential circuit consists of five transistors with various geometries (see Supplementary Fig. 2 for the layout and Fig. 2c for an optical micrograph). The mechanical performance of the stretchable temperature sensor is demonstrated qualitatively in Fig. 2d, with sequential stretching under ~25% uniaxial strain, twisting, and while being poked by a fingertip with ~60% maximum uniaxial strain. (Strain measurements for arbitrary orientations will be addressed in future work.)

The transfer and output characteristics of the stretchable TFT are shown in Fig. 2e,f, respectively. Due to the nonpolar SEBS gate dielectric, the device shows negligible hysteresis with dual sweeps, and the initial threshold voltage (V_{Tp}) is close to 0 V (ref. [30]). The on/off ratio is ~10^4 with a V_{GS} sweep from 10 V to −50 V, while the gate leakage current remains at a reasonably low level. Low-voltage device operation ($V_{GS}=10$ V to −20 V, $V_{DS}=-20$ V) is achieved with an on current higher than 10 μA and off current lower than 1 nA (Fig. 2e inset). These numbers are attributed to the large mobility of plasma-torch (plasma) semiconducting SWCNTs[31,32]. The output characteristics appear linear at low bias (Fig. 2f inset), indicating that there is good contact between the channel semiconductor and source–drain electrodes. On examining 150 fabricated devices, an average mobility of $6.18\pm0.31\ \mathrm{cm^2\,V^{-1}\,s^{-1}}$ was obtained (Supplementary Fig. 3).

Temperature dependence of a single transistor

The starting point of our work was to assess the temperature dependence of individual transistors, and we thus measured the transfer curves of a plasma semiconducting SWCNT TFT in the temperature range 16–55 °C (see Supplementary Fig. 4 for raw data). Figure 3a shows these data in a normalized plot, where all I_D curves are divided by their respective *y*-axis value at 55 °C. A monotonic decrease in drain current (I_D) was observed with decreased temperature at fixed voltages, indicating a large negative temperature coefficient[33]. However, capacitors with the same gate dielectric between the SWCNT bottom and top electrodes showed less than 0.06% $^{\circ}\mathrm{C}^{-1}$ change in capacitance with temperature (Supplementary Fig. 5), indicating that the gate dielectric plays a minor role in the observed temperature dependence. The main mechanism responsible for the temperature dependence of I_D is therefore charge transport in the semiconducting SWCNT network, which is known to vary with temperature[34]. This assumption is consistent with the observed higher temperature dependence at lower terminal voltages (Fig. 3a). Because charge transport in the channel area is dominated by the electric field from the applied voltages, the effect of temperature on charge transport becomes more influential when the electric field is small. The measured temperature coefficient is −1.435% $^{\circ}\mathrm{C}^{-1}$ with $V_{GS}=V_{DS}=-30$ V, and −1.882% $^{\circ}\mathrm{C}^{-1}$ with $V_{GS}=V_{DS}=-5$ V.

A high-pressure carbon monoxide (HiPCO) semiconducting SWCNT TFT was also evaluated in the temperature range 15–48 °C (see Supplementary Fig. 6 for raw data). Figure 3b shows these data in a normalized plot, where the I_D curves are divided by their respective *y*-axis value at 48 °C. The normalized I_D shows reversible temperature dependence and negligible hysteresis between the sweep of heating and cooling. The temperature coefficient of the HiPCO semiconducting SWCNT TFT is −1.909% $^{\circ}\mathrm{C}^{-1}$ with $V_{GS}=V_{DS}=-30$ V. The larger temperature dependence of the HiPCO TFT compared to the plasma TFT is explained by its larger bandgap[30,35], which is again consistent with our hypothesized mechanism in temperature-dependent charge transport.

To evaluate the suitability of a single TFT as a temperature-sensing element, electrical characteristics were collected at different temperatures and strains. The devices were operated in the saturation regime, where the standard (p-channel) equation for I_D is

$$-I_D=\frac{1}{2}\mu C\frac{W}{L}(V_{SG}+V_{Tp})^2=\frac{1}{2}K_p(V_{SG}+V_{Tp})^2 \qquad (1)$$

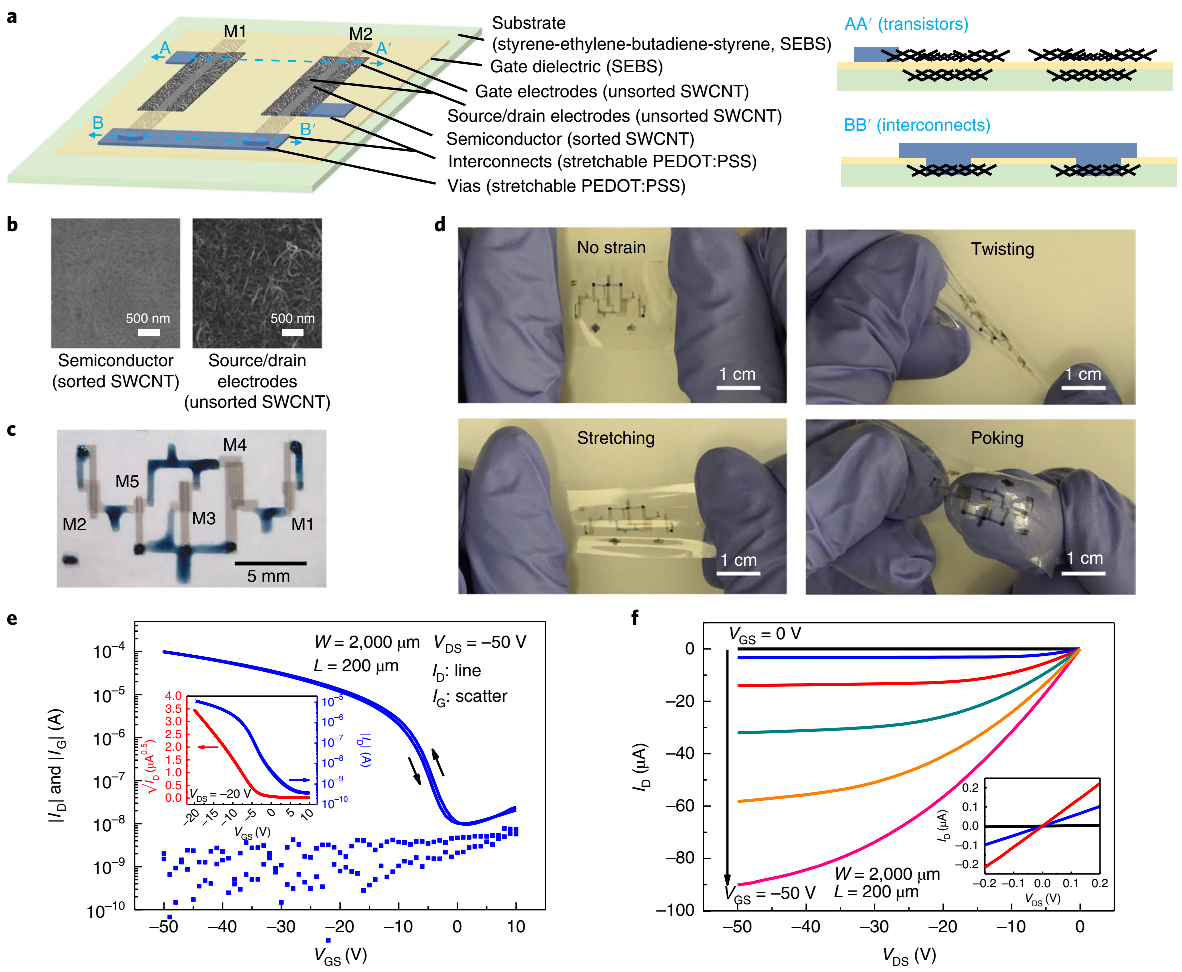

Fig. 2 | Stretchable SWCNT TFTs for circuits. a, Schematic of the structure of an intrinsically stretchable circuit comprising SWCNT TFT devices (left), and cross-sectional images of transistors (AA′) and interconnects (BB′) (right). **b**, SEM images of the carbon nanotube network in the semiconductor channel (left) and source–drain electrodes (right). **c**, Optical micrograph of a stretchable temperature-sensing circuit consisting of five TFTs. **d**, Optical photographs of a stretchable temperature sensor without tensile strain, stretching with 25% uniaxial strain, twisting, and when poked by a fingertip with a maximum uniaxial strain of ~60%. **e**, A typical transfer curve (I_D–V_{GS}, line) and gate leakage curve (I_G–V_{GS}, scatter) of a TFT with forward and backward sweep at $V_{DS} = -50$ V. Inset: transfer curve (I_D–V_{GS}) with forward and backward sweep at $V_{DS} = -20$ V. **f**, Output curves (I_D–V_{DS}) of the same TFT with V_{GS} varying from 0 V to −50 V. Inset: I_D–V_{DS} curves under low drain bias (±0.2 V), indicating good contact between the channel semiconductor and source–drain electrodes.

where μ is the mobility, C is the capacitance of the gate dielectric per unit area, and W and L are the device width and channel length, respectively. The transconductance parameter K_p is defined as $\mu C\frac{W}{L}$, and V_{Tp} is the threshold voltage[36]. Our measurement shows that K_p is more sensitive to temperature than to strain (Supplementary Fig. 7). On the other hand, V_{Tp} shows larger shifts with strain than with temperature, and larger variation between samples (Supplementary Fig. 8). This is further illustrated in Fig. 3c, which plots raw data from Supplementary Fig. 9 using a normalized y axis (K_p is divided by its value at 49 °C, without strain and at $V_{GS} = V_{DS} = -50$ V). The curves are for K_p at 34 °C without strain and with 20% strain (parallel to the charge transport direction), and at 49 °C without strain and with 40% strain. Both cases show that K_p changes mainly with temperature, and shows little response to strain (the changes in K_p are limited to about 3%). When the device is stretched, the geometry changes to the channel length and width decrease the aspect ratio W/L (ref. [28]). This is countered by the decreased thickness of the gate dielectric film under strain, which results in increased gate capacitance[28,37]. Furthermore, the mobility is enhanced by the increased gate capacitance through a reduction in tunnelling barriers between semiconducting SWCNT networks[30]. Consequently, the relatively small impact of strain on the K_p of our device is attributed to cancellation effects between these competing factors.

This behaviour suggests that it might be possible to minimize the effect of strain on temperature if the readout can isolate and cancel the threshold voltage variations. To take a first step in this direction, we note that for a TFT connected in diode configuration, if follows from equation (1) that

$$V_{SG} = \sqrt{\frac{2I_D}{K_p}} - V_{Tp} = V_O \qquad (2)$$

Hence, any shift in V_{Tp} (due to strain or other undesired effects) will be directly reflected in the output voltage V_O. This is confirmed in Fig. 3d, which shows that V_O varies substantially with strain at constant temperature. Although this configuration cannot serve as a reliable temperature sensor, it offers the possibility of cancelling the exposed V_{Tp} shift due to strain.

Strain suppression with static differential circuits

One way to nullify the strain-induced threshold voltage shift is to employ the static differential circuit configuration of Fig. 4a. This

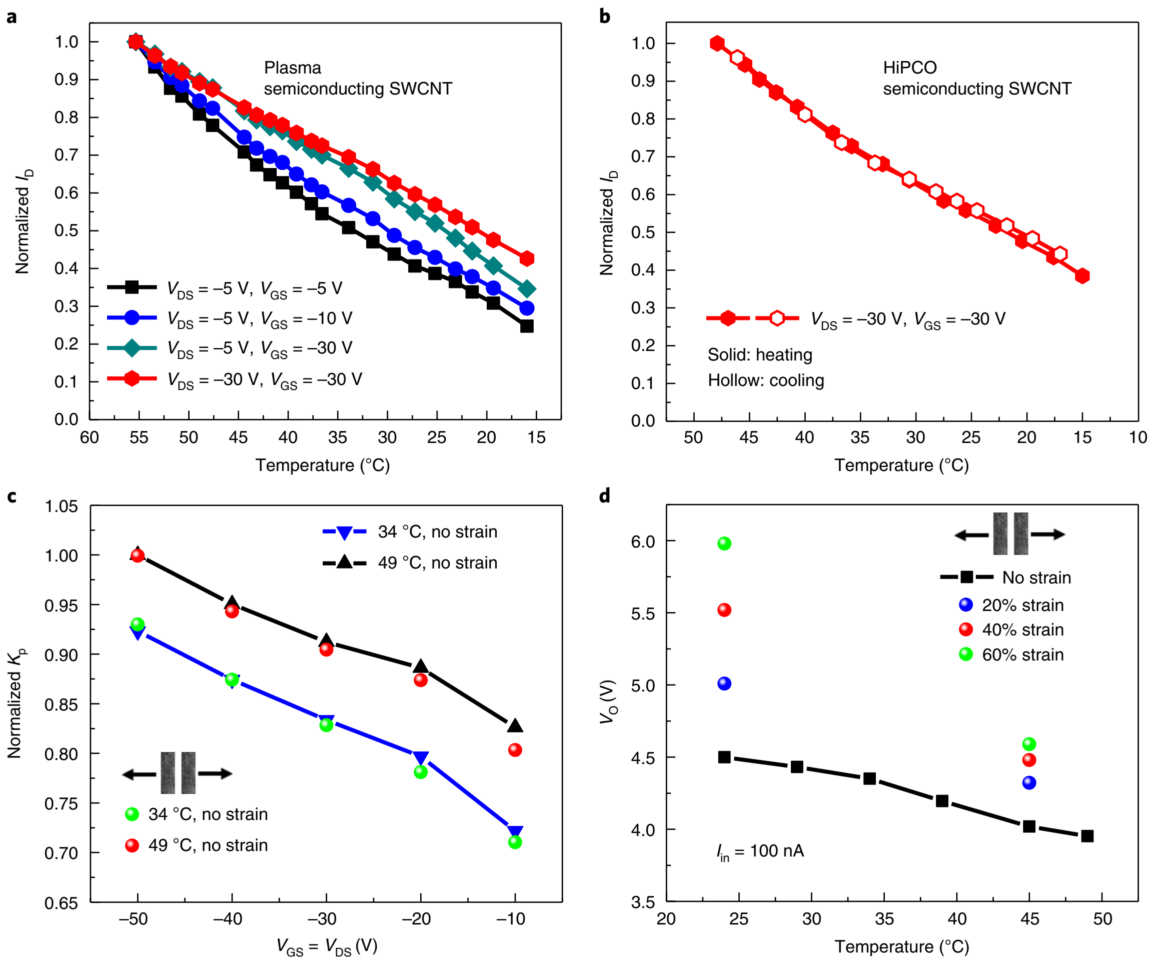

Fig. 3 | Temperature dependence of the stretchable TFT devices. **a**, Normalized drain current of the plasma-torch (plasma) semiconducting SWCNT TFT from 15 to 55 °C (all curves are divided by their respective *y*-axis value at 55 °C). **b**, Normalized drain current of the HiPCO semiconducting SWCNT TFT from 15 to 48 °C with heating and cooling (the I_D curves are divided by their respective *y*-axis value at 48 °C). **c**, Plasma semiconducting SWCNT TFT transconductance parameter ($K_p = \mu C\frac{W}{L}$) as a function of temperature and strain. In this normalized plot, K_p is divided by its value at 49 °C, without strain and at $V_{GS} = V_{DS} = -50$ V. K_p changes mainly with temperature, and shows little response to strain. **d**, Temperature-sensing performance based on a single TFT. The absolute electrical output V_O varies substantially with strain at constant temperature.

circuit consists of two single-ended branches. Transistors M1 and M2 (Fig. 4a) are nominally identical ($K_p = K_{p1} = K_{p2}$, $V_{Tp} = V_{Tp1} = V_{Tp2}$) and are both diode-connected, thus operating in saturation. Transistors M3, M4 and M5 form a current mirror that biases the two branches at some multiple of the input current ($I_1 = N_1 I_{in}$, $I_2 = N_2 I_{in}$). The differential output voltage (V_{OD}) is thus

$$\begin{aligned} V_{OD} &= V_{OS1} - V_{OS2} \\ &= \left(\sqrt{\frac{2I_1}{K_{p1}}} - V_{Tp1}\right) - \left(\sqrt{\frac{2I_2}{K_{p2}}} - V_{Tp2}\right) \\ &= \sqrt{\frac{2I_{in}}{K_p}}\,(\sqrt{N_1} - \sqrt{N_2}) \end{aligned} \tag{3}$$

V_{Tp} shifts will thus be suppressed as long as they match between the two branches. Our measurement results show that this is indeed the case for two TFT devices fabricated on the same substrate (Supplementary Fig. 8b).

To evaluate this concept through simulations, we developed a compact model for the transistors by fitting the measured transfer and output curves at different temperatures and strains (Supplementary Fig. 10). The simulated performance of the designed differential circuit is shown in Fig. 4b. These plots show V_{OD}, V_{OS1} and V_{OS2} as heatmaps and functions of temperature and strain. Although V_{OS1} and V_{OS2} vary with both temperature and strain, V_{OD} is relatively independent of strain (signified by the vertical lines). This simulation demonstrates that the differential circuit strongly suppresses strain effects.

The approach was further verified by measurement of a stretchable temperature-sensing circuit based on the plasma semiconducting SWCNT TFTs. The temperature sensors were initially measured without strain, and then subjected to uniaxial strains of 20, 40 and 60% over the temperature range 22–55 °C. The observed V_{OD} versus temperature is plotted with strain in Fig. 4c for sample 1, and in Fig. 4e for sample 2. Both samples show nearly overlapping temperature-sensing curves between various strains, indicating effective removal of the cross-sensitivity of strains. V_{OD}, V_{OS1} and V_{OS2} of these two representative samples are plotted as heatmaps in Fig. 4d,f. Once again, we see nearly straight-line contours in V_{OD}. The inaccuracy of the temperature sensor caused by strain is only within ±1 °C for the uniaxial strain range from 0 to 60%, as indicated in Fig. 4d,f (left). In contrast, the single-ended outputs of V_{OS1} and V_{OS2} show severe strain sensitivity at a fixed temperature, which is consistent with the results from the single TFT (Fig. 3d). Sample 1 shows positive offset and sample 2

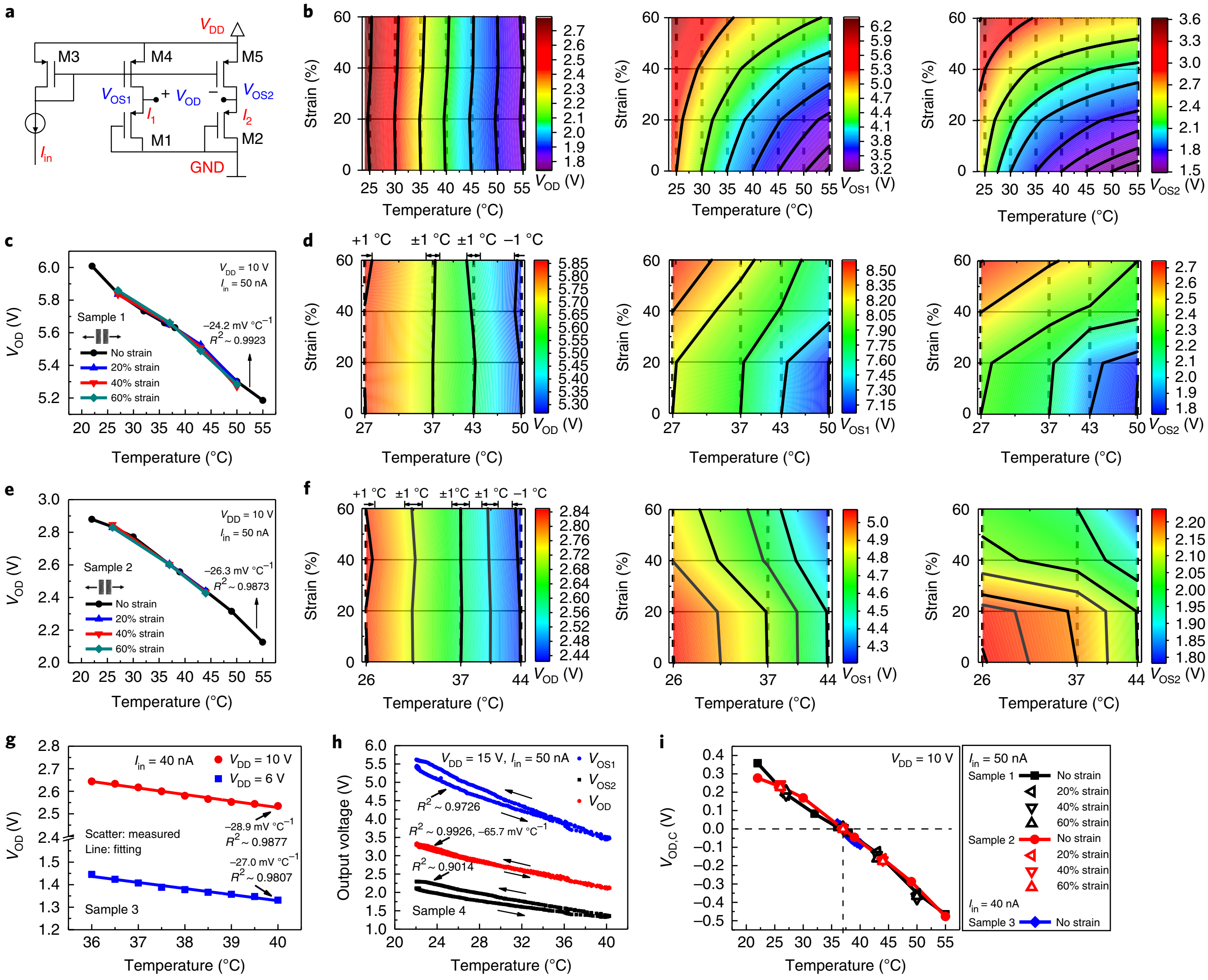

Fig. 4 | Performance of stretchable temperature sensors based on static differential sensing circuit architecture. **a**, Circuit schematic of the static differential sensing approach: V_{OS1} and V_{OS2} are the single-ended outputs, and V_{OD} is the differential output. **b**, Heatmaps as functions of temperature and strain for V_{OD} (left), V_{OS1} (middle) and V_{OS2} (right) from the circuit simulation. V_{OD} is relatively independent of strain (signified by vertical lines), while V_{OS1} and V_{OS2} vary with both temperature and strain. **c**, Temperature-sensing performance of sample 1 (plasma semiconducting SWCNT TFTs) over the temperature range 22–55 °C, with strains of 0, 20, 40 and 60%. R_2, coefficient of determination. **d**, Heatmaps as functions of temperature and strain for V_{OD} (left), V_{OS1} (middle) and V_{OS2} (right) of sample 1. V_{OD} shows a measured inaccuracy within ±1 °C, while V_{OS1} and V_{OS2} show a typical positive 10 °C inaccuracy from the strain effect. **e**, Temperature-sensing performance of sample 2 (plasma semiconducting SWCNT TFTs) over the temperature range 22–55 °C, with uniaxial strains of 0, 20, 40 and 60%. **f**, Heatmaps as functions of temperature and strain for V_{OD} (left), V_{OS1} (middle) and V_{OS2} (right) of sample 2. V_{OD} shows a measured inaccuracy within ±1 °C, while V_{OS1} and V_{OS2} show a typical negative 8 °C inaccuracy from the strain effect. **g**, Temperature-sensing performance of sample 3 (plasma semiconducting SWCNT TFTs) over the fine temperature range of 36–40 °C in steps of 0.5 °C. **h**, Temperature-sensing performance of sample 4 (HiPCO semiconducting SWCNT TFTs) over the temperature range 22–40 °C by heating and cooling. **i**, Sensing curves after single-point calibration (calibrating V_{OD} to 0 V at 37 °C) for samples 1, 2 and 3.

shows negative offset, which is attributed to the variation of TFT samples with positive or negative V_{Tp} shift from strain (Supplementary Fig. 8b). In this case, for a constant value of V_{OS1} for sample 1 (Fig. 4d: middle), the temperature was 37, 37.3, 42.2 and 46.5 °C for uniaxial strain values of 0, 20, 40 and 60%, respectively, which indicates an inaccuracy as high as 9.5 °C. Thus, the differential circuit achieves approximately an order-of-magnitude reduction in inaccuracy.

In addition to its strain suppression, the designed temperature sensor provides high sensitivity, linearity, and low hysteresis. The sensitivity is defined as the slope of the output curve ($\partial V/\partial T$, in V °C^{-1}), and the R^2 value from a linear fit to the curve quantifies the linearity. The sensitivities of samples 1 and 2 were −24.2 mV °C^{-1} ($R^2 = 0.9923$) and −26.3 mV °C^{-1} ($R^2 = 0.9873$), respectively, both in the temperature range 22–55 °C. With a supply voltage of 10 V, the power dissipation was around 300 nW for sample 1 and 144 nW for sample 2. Figure 4g shows a fine temperature sweep (see Methods for the set-up) from 36 to 40 °C in 0.5 °C steps for supply voltages of 6 V and 10 V, indicating that a lower-voltage operation is feasible for body temperature measurements. The achieved sensitivity and power consumption of this circuit-based temperature sensor compare favourably with other reported flexible and stretchable temperature sensors[21,22]. We estimate, based on reported data[19,20,38], that the inaccuracies of other stretchable temperature sensors are as high as 35 °C with 10% uniaxial strain (Supplementary Table 1).

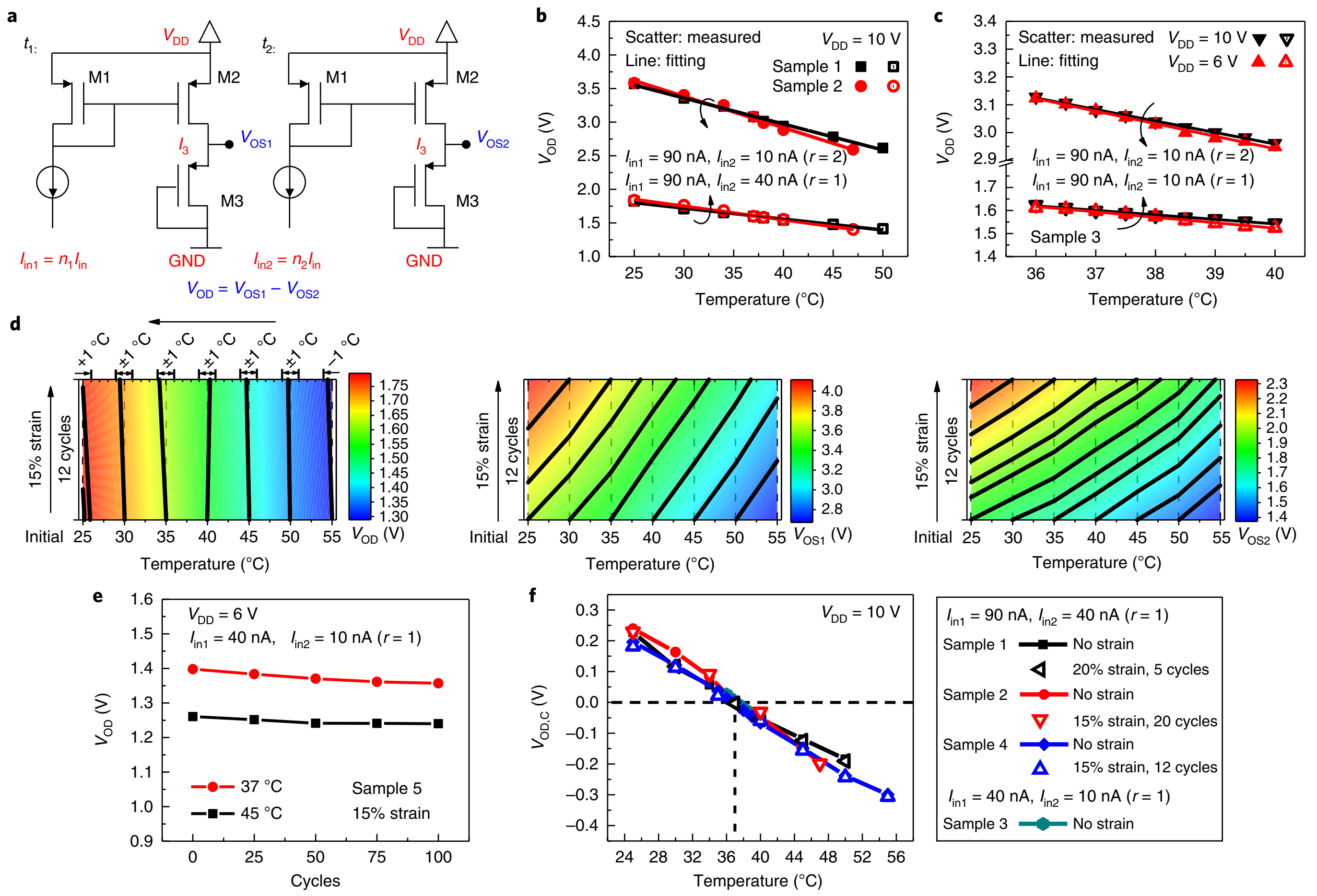

Fig. 5 | Performance of stretchable temperature sensors based on dynamic differential sensing circuit architecture. **a**, Circuit schematic of the dynamic differential sensing approach: V_{OS1} and V_{OS2} are the single-ended outputs corresponding to dynamic input currents with a designed ratio for t_1 and t_2, respectively. V_{OD} is the output from dynamic sensing. **b**, Temperature-sensing performance of samples 1 and 2 (plasma semiconducting SWCNT TFTs) over the temperature range 25–50 °C. **c**, Temperature-sensing performance of sample 3 (plasma semiconducting SWCNT TFTs) over the temperature range 36–40 °C in steps of 0.5 °C. **d**, Heatmaps and functions of temperature and strain for V_{OD} (left), V_{OS1} (middle) and V_{OS2} (right) from the measurement of sample 4 (plasma semiconducting SWCNT TFTs). V_{OD} shows a measured inaccuracy within ±1 °C, while V_{OS1} and V_{OS2} drift dramatically after strain cycling. **e**, Temperature-sensing performance of sample 5 (plasma semiconducting SWCNT TFTs) after 15% uniaxial strain cycling. **f**, Single-point calibration (calibrating V_{OD} to 0 V at 37 °C) for samples 1, 2, 3 and 4, showing almost identical temperature-sensing curves for the different samples.

To investigate hysteresis effects, an intrinsically stretchable temperature sensor with HiPCO semiconducting SWCNT TFTs was measured by heating and cooling over a temperature range from 22 to 40 °C (Fig. 4h). We observed substantial hysteresis in both V_{OS1} and V_{OS2}, due to bias stress that results in V_{Tp} shift[39]. However, the differential output V_{OD} shows closely overlapping traces between heating and cooling, indicating low hysteresis. There is also a notable improvement in linearity (R^2 improving to 0.9926, compared to 0.9726 and 0.9014). These results show that the static differential circuit helps to compensate bias stress effects and even-order nonlinearity. We also note that because the HiPCO semiconducting SWCNT TFT devices used in these measurements have a higher temperature dependence than the plasma semiconducting SWCNT TFTs, the HiPCO temperature sensor shows a correspondingly higher temperature sensitivity of −65.7 mV °C^{-1}.

Finally, we considered the calibration requirements of the sensor. Today's mass-produced temperature sensors typically undergo no more than a single-point calibration to remove mismatch-induced offsets[10–12]. In other words, multiple calibration steps at different temperatures are avoided due to the high production test cost that the heating and cooling of each device would require. In our sensors, V_{OD} suffers from a random offset between samples due to the distribution of initial V_{Tp} values (Supplementary Fig. 3). For the plot in Fig. 4i we nulled these offsets at a fixed temperature of 37 °C and no strain (corresponding to a single-point calibration), and overlaid the outputs for two devices and various amounts of strain. The plotted quantity $V_{OD,C}$ is thus given by $V_{OD}(T) - V_{OD}(37\,°C)$. We observed almost identical temperature-sensing curves between samples, indicating that the sample-to-sample variation of V_{OD} is effectively eliminated by a one-point calibration.

Strain suppression with dynamic differential circuits

As an alternative to the static differential sensor circuit described above, we also investigated a dynamic variant for strain suppression. The main idea of this approach is to switch the circuit between two states, and to infer the temperature from changes in the observed outputs. Figure 5a shows the circuit schematic and measurement method. Transistors M1 and M2 serve as a current mirror to provide a bias current (I_3) for the diode-connected sensing transistor M3 (K_p, V_{TP}). At time t_1, the input current is set to $I_{in1} = n_1 I_{in}$ (and $I_3 = NI_{in1}$ via the current mirror), and the output is recoded as V_{OS1}. Sequentially, at time t_2, the input current is set to $I_{in2} = n_2 I_{in}$ ($I_3 = NI_{in2}$), and the output is recoded as V_{OS2}. Then the dynamic output (V_{OD}) is computed as

$$\begin{aligned} V_{\mathrm{OD}} &= V_{\mathrm{OS1}} - V_{\mathrm{OS2}} \\ &= \left(\sqrt{\frac{2Nn_1 I_{\mathrm{in}}}{K_{\mathrm{p}}}} - V_{\mathrm{Tp}}\right) - \left(\sqrt{\frac{2Nn_2 I_{\mathrm{in}}}{K_{\mathrm{p}}}} - V_{\mathrm{Tp}}\right) \\ &= \sqrt{\frac{2NI_{\mathrm{in}}}{K_{\mathrm{p}}}}\,(\sqrt{n_1} - \sqrt{n_2}) \\ &= \sqrt{\frac{2NI_{\mathrm{in}}}{K_{\mathrm{p}}}}\,r \end{aligned} \tag{4}$$

This result is similar to equation (3) and thus the circuit is expected to achieve the same error compensation as the static approach. The main difference is that parameters N_1 and N_2 in equation (3) are determined by sizing the current mirror, whereas parameters n_1 and n_2, here, are controlled by the input current from the measurement set-up. Also, note that the V_{Tp} term cancels in the equation, because only one single transistor is involved (this is in contrast to the approximate cancellation of V_{Tp1} and V_{Tp2} in equation (3)).

Samples 1 and 2 were characterized using the dynamic sensing approach over the temperature range 25–50 °C (Fig. 5b) and sample 3 was characterized from 36 to 40 °C in steps of 0.5 °C (Fig. 5c). All measurements use two different input current settings of $r=2$ and $r=1$ (equation (4)). Both samples yield an approximate ratio of two in V_{OD} between these two measurement settings, which is consistent with equation (4). Sample 3 yields a sensitivity of −23.1 mV °C^{-1} when $r=1$ and −45.2 mV °C^{-1} when $r=2$.

For strain characterization, sample 4 was initially measured without strain, and then measured after applying 15% uniaxial strain over 12 cycles, and within the temperature range 22–55 °C. Note that, for this experiment, we use a smaller strain range that corresponds to the intended application (a larger strain was used earlier for robustness in transistor modelling). As explained in the literature, 15% is a borderline tolerable (and already uncomfortable) level of strain for the human skin[40]. From the data of Fig. 5d (left), we observe that V_{OD} changes by less than 0.02 V between measurements without strain and after strain cycling. As shown, the inaccuracy from strain cycling lies within ±1 °C. As expected, V_{OS1} (Fig. 5d: middle) and V_{OS2} (Fig. 5d: right) drift dramatically after cycling. The robustness of the stretchable temperature sensor is further demonstrated by its stable V_{OD} over 100 repeated stretching cycles (Fig. 5e).

Compared to the static differential sensing circuit, the variation in V_{OD} between samples of the dynamic differential sensing circuit is expected to be much smaller, because the distribution of initial V_{Tp} has no effect. However, there can still be a small offset in V_{OD} between samples due to the bias-current-induced variation of V_{Tp} for the same device. Thus, we performed a single-point calibration at 37 °C as explained before. The results in Fig. 5f once again confirm the effective suppression of sample-to-sample variation in V_{OD}.

Conclusions

We have reported circuit design strategies that provide robust and accurate temperature sensing with stretchable devices. First, the temperature dependence of individual single-walled carbon nanotube thin-film transistors was comprehensively evaluated and interpreted to devise a suitable sensing approach. This led to the design and experimental validation of both static and dynamic differential circuits that reject strain-induced errors in the temperature reading. Sensor performance, including sensitivity, linearity and power dissipation, was evaluated, and a single-point calibration was shown to be effective in eliminating sample-to-sample variations. Future iterations on the reported concepts would benefit from smaller feature sizes, so that non-uniformities in strain and temperature can be minimized for added robustness. Similarly, smaller feature sizes will enable the integration of instrumentation electronics close to the sensor elements, and thereby allow real-time monitoring during fast stretching cycles. Although this work has principally dealt with temperature sensing, we expect that generalizations towards other stretchable sensor modalities are possible.

Methods

Materials. SWCNTs were procured from commercial sources. HiPCO SWNTs were from Nano-integris, as were plasma-torch (plasma) CNTs (product no. RN 020), and arc-discharged SWNTs were P2-SWNTs from Carbon Solutions. The supramolecular sorting polymer was synthesized according to our previously published procedure[22]. Hydrogenated SEBS with 20% styrene content (Tuftec H1052) was supplied by Asahi Kasei Elastomers. PEDOT:PSS (PH1000) was obtained from Clevios and the ionic liquid 4-(3-butyl-1-imidazolio)-1-butanesulfonic acid triflate from Santa Cruz Biotechnology.

Fabrication. SWCNTs were sorted for semiconducting SWCNTs as described previously[22]. In brief, 5 mg SWCNTs and 10 mg sorting polymer were combined with 20 ml toluene. The mixture was sonicated for 30 min at 30% power using a Cole Parmer 750 W tip sonicator. The resulting dispersion was centrifuged at 17,000 r.p.m. for 30 min and the supernatant was retained to be utilized for the semiconductor coating.

To prepare the electrodes, unsorted (as produced) arc-discharged SWCNTs were spray-coated onto silicon wafers as previously described[21]. Electrodes were patterned using a photolithography approach[25]. The SWCNT electrodes on Si wafers were annealed at 200 °C to dehydrate and improve adhesion. Shipley S1813 photoresist was spin-coated at 2,000 r.p.m. and baked at 100 °C for 3 min. After exposure and development, the substrates were exposed to oxygen plasma for 5 min to remove photoresist residue and pattern the SWCNTs. After patterning, the substrates were annealed at 120 °C for 5 min and the photoresist was removed by sequentially soaking in three clean acetone baths for 3 min each. The substrates were rinsed with 2-propanol and dried.

SEBS substrates were prepared by casting a 150 mg ml^{-1} solution in toluene onto a glass slide and evaporating the toluene solvent of toluene. The thickness of the substrate was ~120 µm. SEBS gate dielectric layers were prepared by spin-coating a 60 mg ml^{-1} solution in toluene onto a non-stick surface-modified wafer[25]. The thickness of the gate dielectric was ~1.2 µm. SEBS encapsulation layers were prepared by spin-coating a 100 mg ml^{-1} solution in toluene at 1,000 r.p.m. for 1 min onto a non-stick surface-modified wafer[25]. The thickness the encapsulation layer was ~3 µm.

To prepare the PEDOT:PSS solutions for vias and interconnects, 4-(3-butyl-1-imidazolio)-1-butanesulfonic acid triflate (45.5 wt%) was added to the PEDOT:PSS aqueous dispersion (1.1–1.3 wt%) and stirred vigorously for 5 min, then left stirring at 250–300 r.p.m. to keep the dispersion from gelling until use[24]. Fluorinated treatment was applied for shadow masks of screen printing for interconnects.

For the multi-step transfer fabrication method, a solution of 20 mg ml^{-1} SEBS in toluene was spin-coated onto the patterned gate electrodes as an adhesion layer. The gate electrodes were then transfer-printed onto the SEBS substrate. The vias were fabricated by dropcasting stretchable PEDOT:PSS onto the gate electrodes to achieve a feature size of ~0.25 mm^2, followed by annealing at 60 °C for 3 min. The fabricated gate dielectric layer with substrate was transferred onto the gate electrode by lamination, and the vias were self-aligned through the dielectric layer. Interconnects were screen-printed using designed patterns. A separate Si wafer with the patterned source and drain electrodes was soaked in semiconducting SWCNT solution for 30 min, washed in toluene, and blow-dried with nitrogen. The masks for patterning the semiconducting SWCNTs were prepared with a PDMS thin layer. O_2 plasma was used to dry etch the semiconducting SWCNTs. After patterning the semiconducting SWCNTs, the source/drain/semiconductor substrate was annealed at 100 °C for 1 min to improve adhesion. Subsequently, a solution of 1% trifluoroacetic acid in toluene was spin-coated onto the source/drain/semiconductor substrate to remove the sorting polymer, followed by spin-coating toluene with one bath to rinse off the residual trifluoroacetic acid. The source/drain/semiconductor on Si was transferred by lamination onto the interconnect/dielectric/vias/gate on the SEBS substrate. Transfer printing was carried out at a pressure of ~150 kPa, applied manually. Finally, the prepared encapsulation layer was transferred by lamination onto the device, mainly to protect the semiconductor and increase adhesion.

Characterization. SEM images were collected using a Magellan 400 XHR with an acceleration voltage of 1 kV. Devices and circuits were characterized using a Keithley 4200 probe station in an ambient atmosphere. Strain-dependent and temperature-dependent measurements were collected using a stretching apparatus with a temperature controller. The sensing readout was implemented through a LabVIEW program.

Temperature controller set-up. Temperature measurements were performed using a stretching apparatus with a temperature controller, as shown in Supplementary Fig. 11. The set-up consisted of two copper blocks with embedded K-type thermocouples (OMEGA Engineering) electrically isolated from the blocks with a thin layer of polyimide. The temperatures of the copper blocks were independently controlled and monitored with a CN7900 Dual-zone PID controller (OMEGA Engineering) connected to two TEC1-06303 Peltier devices (Denshi Trade). The Peltier devices were powered by a switching power supply (Meanwell-RS-150-12), and were sandwiched between the copper and aluminium blocks, with paste on either side to ensure good thermal contact. The copper blocks were attached to the aluminium blocks with glass-fibre-reinforced nylon screws (McMaster-Carr). The aluminium blocks were threaded onto a dowel pin with a steel spring between them and a screw at one end to accurately control the spacing between them along with a caliper. During measurements, the sample was attached to the copper blocks via copper clamps screwed onto the surface, with thermal paste between the sample and copper blocks to ensure good thermal contact. Peltier devices were used to set the temperature, and the thermocouples monitored the temperature within a feedback loop. A metal cover was placed onto the apparatus to ensure a stable temperature environment.

Simulation. The compact model was implemented using Verilog-A in the Cadence Virtuoso Circuit Simulator, and the simulations were run using a DC Analysis.

Data availability. The data that support the plots within this paper and other findings of this study are available from the corresponding author upon reasonable request.

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References

1. Gao, W. et al. Fully integrated wearable sensor arrays for multiplexed in situ perspiration analysis. *Nature* **529**, 509–514 (2016).
2. Park, S. I. et al. Soft, stretchable, fully implantable miniaturized optoelectronic systems for wireless optogenetics. *Nat. Biotechnol.* **33**, 1280–1286 (2015).
3. Chortos, A., Liu, J. & Bao, Z. Pursuing prosthetic electronic skin. *Nat. Mater.* **15**, 937–950 (2016).
4. Tee, B. C.-K. et al. A skin-inspired organic digital mechanoreceptor. *Science* **350**, 313–316 (2015).
5. Wehner, M. et al. An integrated design and fabrication strategy for entirely soft, autonomous robots. *Nature* **536**, 451–455 (2016).
6. Gupta, S. & Loh, K. J. Noncontact electrical permittivity mapping and pH-sensitive films for osseointegrated prosthesis and infection monitoring. *IEEE Trans. Med. Imag.* **36**, 2193–2202 (2017).
7. Lee, S. et al. A strain-absorbing design for tissue–machine interfaces using a tunable adhesive gel. *Nat. Commun.* **5**, 5898 (2014).
8. Soekadar, S. R. et al. Hybrid EEG/EOG-based brain/neural hand exoskeleton restores fully independent daily living activities after quadriplegia. *Sci. Robot.* **1**, eaag3296 (2016).
9. Meijer, G., Pertijs, M. & Makinwa, K. *Smart Sensor Systems: Emerging Technologies and Applications* (Wiley, New York, NY, 2014).
10. Hsu, Y.-C. et al. An 18.75 µW dynamic-distributing-bias temperature sensor with 0.87°C (3σ) untrimmed inaccuracy and 0.00946 mm^2 area. *2017 IEEE Int. Solid-State Circuits Conf.* https://doi.org/10.1109/ISSCC.2017.7870281 (2017).
11. Yousefzadeh, B., Shalmany, S. H. & Makinwa, K. A. A. A BJT-based temperature-to-digital converter with ±60 mK (3σ) inaccuracy from −55 °C to +125 °C in 0.16-µm CMOS. *IEEE J. Solid-State Circuits* **52**, 1044–1052 (2017).
12. Deng, C. et al. A CMOS smart temperature sensor with single-point calibration method for clinical use. *IEEE Trans. Circuits Syst. II* **63**, 136–139 (2016).
13. Ha, D. et al. Time-domain CMOS temperature sensors with dual delay-locked loops for microprocessor thermal monitoring. *IEEE Trans. Very Large Scale Integr. Syst.* **20**, 1590–1601 (2012).
14. Hattori, Y. et al. Multifunctional skin-like electronics for quantitative, clinical monitoring of cutaneous wound healing. *Adv. Healthcare Mater.* **3**, 1597–1607 (2014).
15. Jin, H., Abu-Raya, Y. S. & Haick, H. Advanced materials for health monitoring with skin-based wearable devices. *Adv. Healthcare Mater.* **6**, 1700024 (2017).
16. Yokota, T. et al. Ultra-flexible, large-area, physiological temperature sensors for multipoint measurements. *Proc. Natl Acad. Sci. USA* **112**, 14533–14538 (2015).
17. Kim, D.-H. et al. Materials for multifunctional balloon catheters with capabilities in cardiac electrophysiological mapping and ablation therapy. *Nat. Mater.* **10**, 316–323 (2011).
18. Xu, L. et al. 3D multifunctional integumentary membranes for spatiotemporal cardiac measurements and stimulation across the entire epicardium. *Nat. Commun.* **5**, 3329 (2014).
19. Yan, C., Wang, J. & Lee, P. S. Stretchable graphene thermistor with tunable thermal index. *ACS Nano* **9**, 2130–2137 (2015).
20. Trung, T. Q., Ramasundaram, S., Hwang, B.-U. & Lee, N.-E. An all-elastomeric transparent and stretchable temperature sensor for body-attachable wearable electronics. *Adv. Mater.* **28**, 502–509 (2016).
21. Khan, Y., Ostfeld, A. E., Lochner, C. M., Pierre, A. & Arias, A. C. Monitoring of vital signs with flexible and wearable medical devices. *Adv. Mater.* **28**, 4373–4395 (2016).
22. Webb, R. C. et al. Ultrathin conformal devices for precise and continuous thermal characterization of human skin. *Nat. Mater.* **12**, 938–944 (2013).
23. Salowitz, N. P. et al. Microfabricated expandable sensor networks for intelligent sensing materials. *IEEE Sens. J.* **14**, 2138–2144 (2014).
24. Chortos, A. et al. Mechanically durable and highly stretchable transistors employing carbon nanotube semiconductor and electrodes. *Adv. Mater.* **28**, 4441–4448 (2016).
25. Pochorovski, I. et al. H-bonded supramolecular polymer for the selective dispersion and subsequent release of large-diameter semiconducting single-walled carbon nanotubes. *J. Am. Chem. Soc.* **137**, 4328–4331 (2015).
26. Lei, T., Pochorovski, I. & Bao, Z. Separation of semiconducting carbon nanotubes for flexible and stretchable electronics using polymer removable method. *Acc. Chem. Res.* **50**, 1096–1104 (2017).
27. Wang, Y. et al. A highly stretchable, transparent, and conductive polymer. *Sci. Adv.* **3**, e1602076 (2017).
28. Xu, J. et al. Highly stretchable polymer semiconductor films through the nanoconfinement effect. *Science* **355**, 59–64 (2017).
29. Li, Y. & Shimizu, H. Toward a stretchable, elastic, and electrically conductive nanocomposite: morphology and properties of poly[styrene-*b*-(ethylene-*co*-butylene)-*b*-styrene]/multiwalled carbon nanotube composites fabricated by high-shear processing. *Macromolecules* **42**, 2587–2593 (2009).
30. Chortos, A. et al. Investigating limiting factors in stretchable all-carbon transistors for reliable stretchable electronics. *ACS Nano* **11**, 7925–7937 (2017).
31. Wang, H. & Bao, Z. Conjugated polymer sorting of semiconducting carbon nanotubes and their electronic applications. *Nano Today* **10**, 737–758 (2016).
32. Zhou, X. J., Park, J. Y., Huang, S. M., Liu, J. & McEuen, P. L. Band structure, phonon scattering, and the performance limit of single-walled carbon nanotube transistors. *Phys. Rev. Lett.* **95**, 146805 (2005).
33. Gao, J. & Loo, Y.-L. Temperature-dependent electrical transport in polymer-sorted semiconducting carbon nanotube networks. *Adv. Funct. Mater.* **25**, 105–110 (2015).
34. Yao, Z., Postma, H. W. C., Balents, L. & Dekker, C. Carbon nanotube intramolecular junctions. *Nature* **402**, 273–276 (1999).
35. Rother, M. et al. Understanding charge transport in mixed networks of semiconducting carbon nanotubes. *ACS Appl. Mater. Interfaces* **8**, 5571–5579 (2016).
36. Murmann, B. *Analysis and Design of Elementary MOS Amplifier Stages* (NTS Press, Austin, TX, 2013).
37. Cai, L., Zhang, S., Miao, J., Yu, Z. & Wang, C. Fully printed stretchable thin-film transistors and integrated logic circuits. *ACS Nano* **10**, 11459–11468 (2016).
38. Huang, C.-C., Kao, Z.-K. & Liao, Y.-C. Flexible miniaturized nickel oxide thermistor arrays via inkjet printing technology. *ACS Appl. Mater. Interfaces* 5, 12954–12959 (2013).
39. Lee, S. W. et al. Positive gate bias stress instability of carbon nanotube thin film transistors. *Appl. Phys. Lett.* **101**, 053504 (2012).
40. Markenscoff, X. & Yannas, I. V. On the stress–strain relation for skin. *J. Biomech.* **12**, 127–129 (1979).

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Author contributions

C.Z. and B.M. conceived the concept. C.Z., B.M. and Z.B. conceived the experiments. C.Z., A.C., Y.W. and T.L. developed the fabrication processes. C.Z. and R.P. performed data collection and analysis of temperature-dependence for transistors. A.C.H., C.Z. and J.Y.O. designed the test station with strain and temperature. X.Y. and I.P. synthesized the supramolecular sorting polymer. J.W.-F.T. collected SEM images. Z.B. and B.M. supervised the project. All authors provided comments for the manuscript.

Competing interests

The authors declare no competing interests.

Additional information

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