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Process design kit and design automation for flexible hybrid electronics

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Abstract

High-performance and low-cost flexible hybrid electronics (FHE) are desirable for applications such as Internet of Things (IoT), wearable electronics, and flexible displays. However, design toolkit, design methodology, and compact models that play an essential role in designing complex FHE circuits and systems are still missing today. To fill this gap, here we report (a) the process design kit (PDK) dedicated to electronic design automation for FHE circuits and systems and (b) solution process–proven intellectual property (IP) blocks, which serves as a stepping stone for designing large-scale flexible thin-film transistor (TFT) circuits. The proposed FHE-PDK is made compatible with modern electronics design tools for users to design, simulate, and verify physical design of flexible hybrid systems.

KEYWORDS

flexible hybrid electronics, printed electronics, thin-film transistors, thinned silicon chips

1 | INTRODUCTION

Flexible and printable electronics have exponential growth in performance and cost reduction in recent years, which enables new applications such as disposable sensors, radio-frequency identification (RFID) tags, and low-cost Internet of Things (IoT).[1,2] To design a large-scale (more than 1000 transistor counts) digital and analog flexible thin-film transistor (TFT) circuitry that is manufacturable with low-cost printing and solution-based processes, however, is another story. Because of large printing process variations, as well as the lack of complementary and reliable TFTs, complex TFT circuits often suffer from high static power consumption, low noise margin, and poor circuit yield. These limitations make TFT circuits targeting low power and low supply voltages a significant challenge.

On the other hand, the hybrid integration of thinned silicon chips with printable TFTs on the same flexible substrate opens another door leading to a wide range of applications. The flexible printed sensors and TFT circuits that benefit from low manufacturing costs for large areas and their conformal form factors are an ideal complement to thinned low-power silicon chips for flexible IoT endpoints or wearable devices. We have previously reported our device fabrication and material properties in

Lei,[3] device models in Shao,[4] and previous progress of flexible hybrid electronics (FHE)-process design kit (PDK) in Shao[5] and Huang[6] that includes (a) simulation models of printable passive and active devices, such as carbon-nanotube (CNT) TFTs, resistors, inductors, and capacitors; (b) design rules of printable devices validated using specific printing or solution processing technologies; (c) multi-physics simulation models that can capture the interactions among electrical-thermal-mechanical performance; and (d) codesign capability for both printed electronics and thinned silicon chips, using the same design environment and electronic design automation (EDA) toolsets to improve the design productivity and design time.

In this paper, we focus on our latest progress regarding FHE-PDK to include (a) model validations against fabricated devices for CNT, organic, and indium-gallium-zinc-oxide (IGZO) TFTs, CNT resistors, and parallel-plate capacitors; (b) experimentally validated design rules and physical design verification capability, such as design rule checker (DRC) for physical layout; and (c) low-voltage (3 V) TFT digital and analog open-source design intellectual property (IP) blocks. The technologies files, simulation models, and parameterized cells (p-cell) are fully compatible with mainstream IC-centric EDA toolsets for silicon complementary metal oxide semiconductor (CMOS) design, which makes FHE-PDK an ideal choice for codesign, cosimulate, and coverify FHE design containing both printed TFTs and thinned silicon chips. Latest FHE-PDK also supports printed circuit board (PCB)-centric toolsets for DRC, signal, and power integrity analysis (SI/PI) to provide FHE system design and verification supports of FHE design projects. This paper is meant to provide an overview of the development for FHE-PDK and how it can help electronics designers to significantly improve their design capability and productivity using solution process–proven device models and IP blocks, as well as state-of-the-art design and verification tools.

2 | DEVICE MODELING

2.1 | Compact TFT models

Several TFT compact models targeting specific technologies have been developed,[7] which may not be generalized for other technologies. Some studies focus only on modeling the DC behavior,[8] which does not support transient simulations. In this paper, we present an unified compact model of TFTs covering DC, AC, and technology scaling factor for supporting TFT circuit design and also validate the proposed models against measurement results using three TFT technologies: CNT-TFT, IGZO-TFT, and organic TFT.[4] The model-measurement validation using current-voltage (I-V) curves is shown in Figure 1, and the extracted TFT parameters are shown in Table 1. On the basis of this model, we further perform circuit level

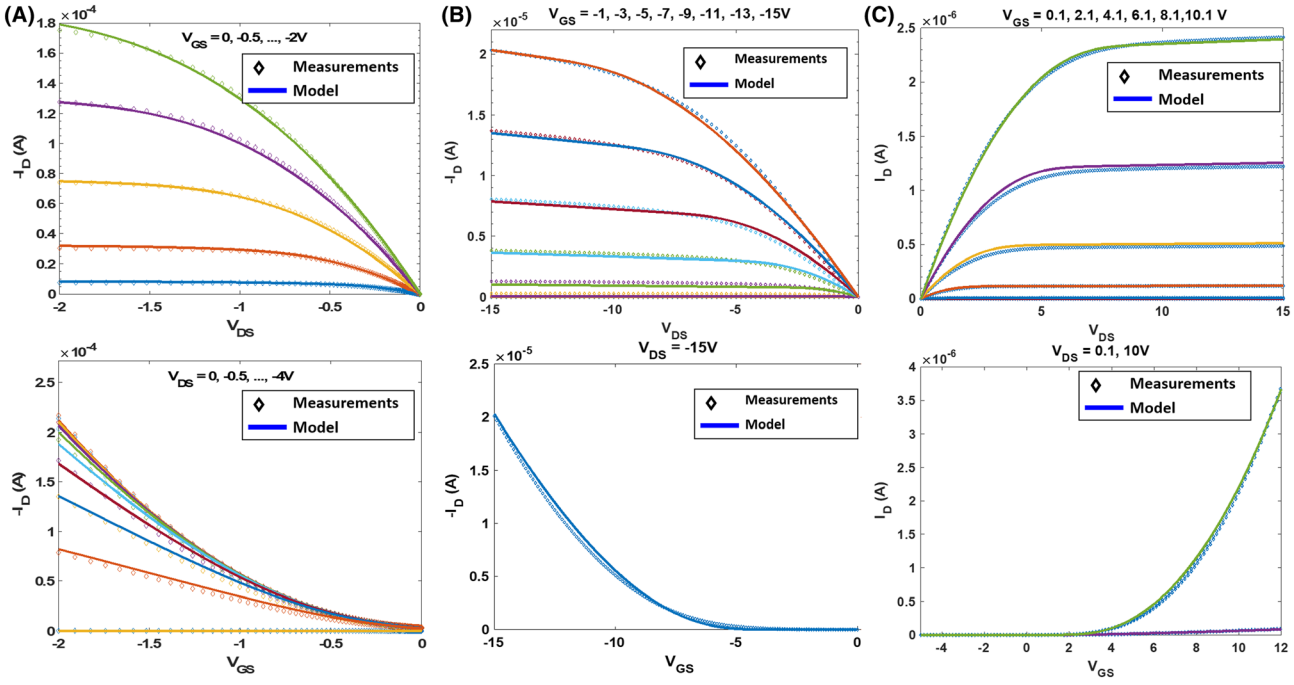

FIGURE 1 Measured (dotted) and fitted (solid) current-voltage (I-V) curves for (A) carbon-nanotube (CNT)-thin-film transistor (TFT) (W = 125 μm, L = 25 μm), (B) Organic TFT (W = 5000 μm, L = 10 μm), and (C) indium-gallium-zinc-oxide (IGZO)-TFT (W = 30 μm, L = 20 μm)[4]

validation based on fabricated *Pseudo-CMOS*[9] inverters, sequence generators, and ring oscillators. The proposed model is implemented using Verilog-A in order to perform cosimulations with thinned silicon CMOS circuitry, thus enables FHE designers to explore a variety of design and integration options for TFT-CMOS flexible hybrid circuits and evaluate their performance for a wide range of commercial and military applications from sensing, display, IoT, healthcare, to wearable medical devices.[4]

2.2 | Resistor models

In addition to TFTs, the CNT film can also be used to realize a linear resistor, and the manufacturing process of a CNT resistor is fully compatible with CNT-TFTs. The CNT resistors have a wide range of applications such as linear and transimpedance amplifiers and low-pass filters.

TABLE 1 Extracted parameters for CNT, IGZO, and organic TFT technologies

Notation (Unit)	CNT-TFT [μ, σ]	IGZO-TFT [μ]	OTFT [μ]
L (μm)	[25, -]	[20]	[10]
W (μm)	[125, -]	[30]	[5000]
L_{OV} (μm)	[10,-]	[10]	[20]
C_{OX} (nF/cm^2)	[200,-]	[70]	[15]
V_{TH} (V)	[0.5, 0.102]	[1.9]	[−4.2]
SS (V/dec)	[0.28, 0.0388]	[0.8]	[0.6]
μ_0 (cm^2/V.s)	[25.69, 0.19]	[1.6]	[0.02]
R_C (Ω)	[1531, 291]	[2500]	[80000]
λ (V^{-1})	[0.064, 0.0185]	[0.002]	[0.028]
γ (Unitless)	[0.2, 0.116]	[0.3]	[0.5]
θ (V^{-1})	[0.01, 0.002]	[0.005]	[0.002]

Abbreviations: CNT, carbon-nanotube; IGZO, indium-gallium-zinc-oxide; TFT, thin-film transistor.

To further study the CNT resistor's linearity and process variations, we fabricated and characterized 864 CNT resistors on a flexible substrate shown in Figure 2. With 40-μm resistor width W, the length L is varied from 2 to 100 μm, and the measured I to V curves are shown in Figure 3. CNT resistors show a good linearity when the length is greater than 10 μm, when compared against a linear fitting curve. Figure 4 further reveals the process variations of the CNT resistors, where a total of 96 test samples are included for each test case of the resistor lengths L = 10, 50, and 100 μm, and a total of 384 test samples are included for the resistor length L = 20 μm. While the histograms follow normal distributions, we can learn that the standard deviations of the CNT resistance reduce when the resistor length L increases. The sheet resistance of the CNT film is around 137 kΩ for L = 10 μm and decreases to 103 kΩ for L = 100 μm. For the CNT resistors, the resistance values can be readily calculated using $R_{CNT} = R_{CH} * L/W_R + R_C/W_R$, where R_{CNT} is the total resistance in KΩ, R_{CH} is the channel resistance in KΩ, R_C in KΩ is the contact resistance attributed by metal-CNT interfaces, L is the resistor length in micrometers (μm), and W_R is the resistor width also in micrometers (μm). While in this practice, the critical dimensions, such as the resistor length L and width W, are defined using traditional lithography, the materials of CNT films are fully compatible with solution or printing processes that could significantly reduce the manufacturing costs. The fitted linear resistor models and distributions are included into FHE-PDK models for SPICE simulations.

2.3 | Capacitor models

In addition to CNT resistors, flexible capacitors can also be realized using TFT compatible solution processes for applications such as signal filters and equalizers. Here, we use simple top-bottom parallel-plate structures to

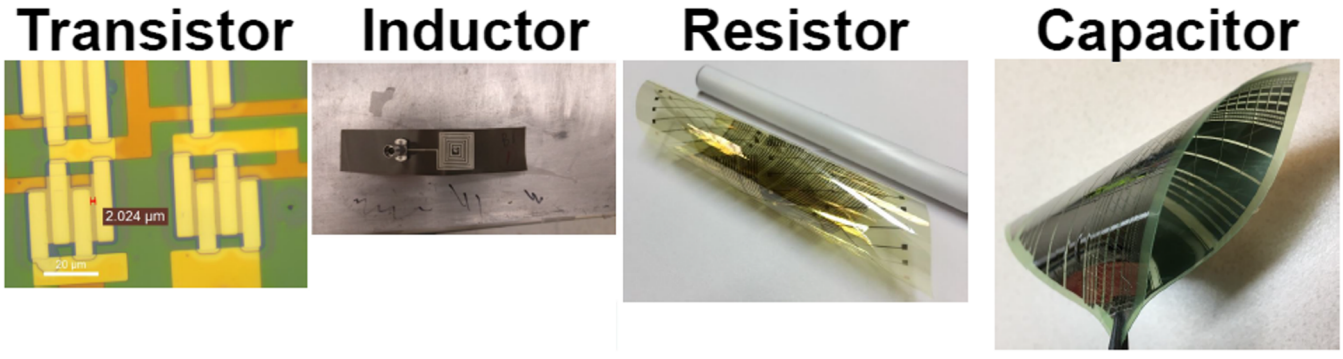

FIGURE 2 Fabricated physical samples of flexible active and passive devices including CNT-TFTs, spiral inductors, CNT resistors, and parallel-plate capacitors. TFTs, resistors, and capacitors are fabricated using lithography-assisted solution processes, and the spiral inductors are printed using screen printers

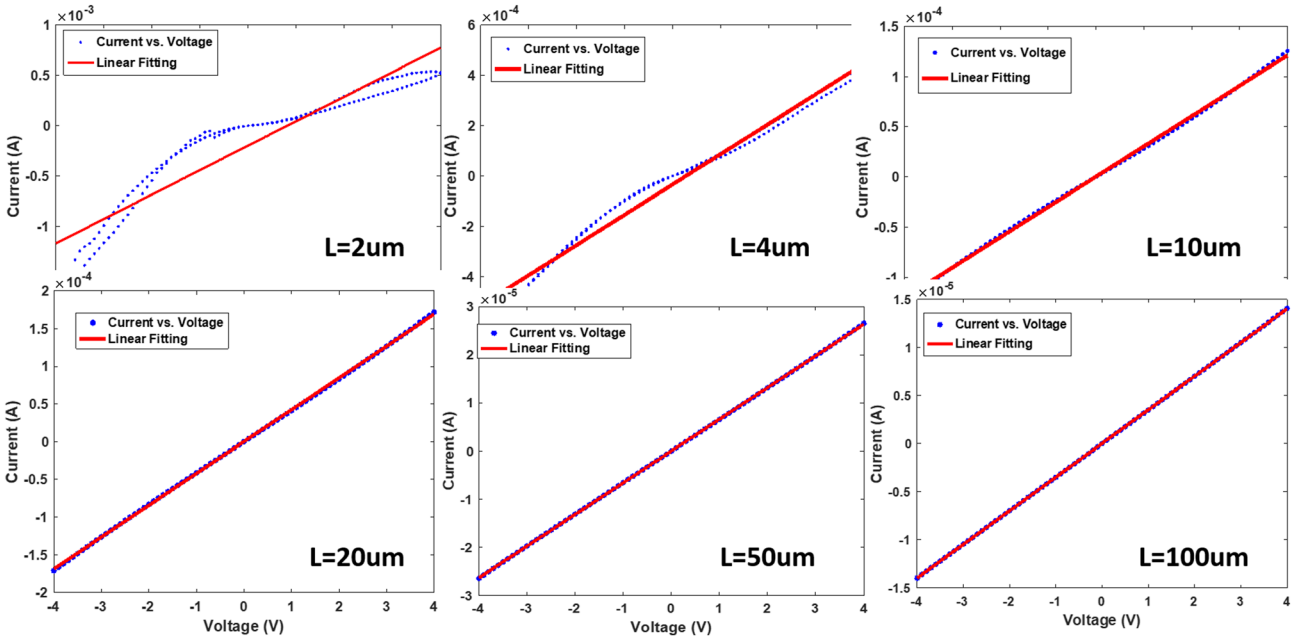

FIGURE 3 Measured current-voltage (I-V) curves (blue-dot) of carbon-nanotube (CNT) resistors against linear fitting model (red-line) for resistor lengths from 2 to 100 μm, and the width is fixed to 40 μm

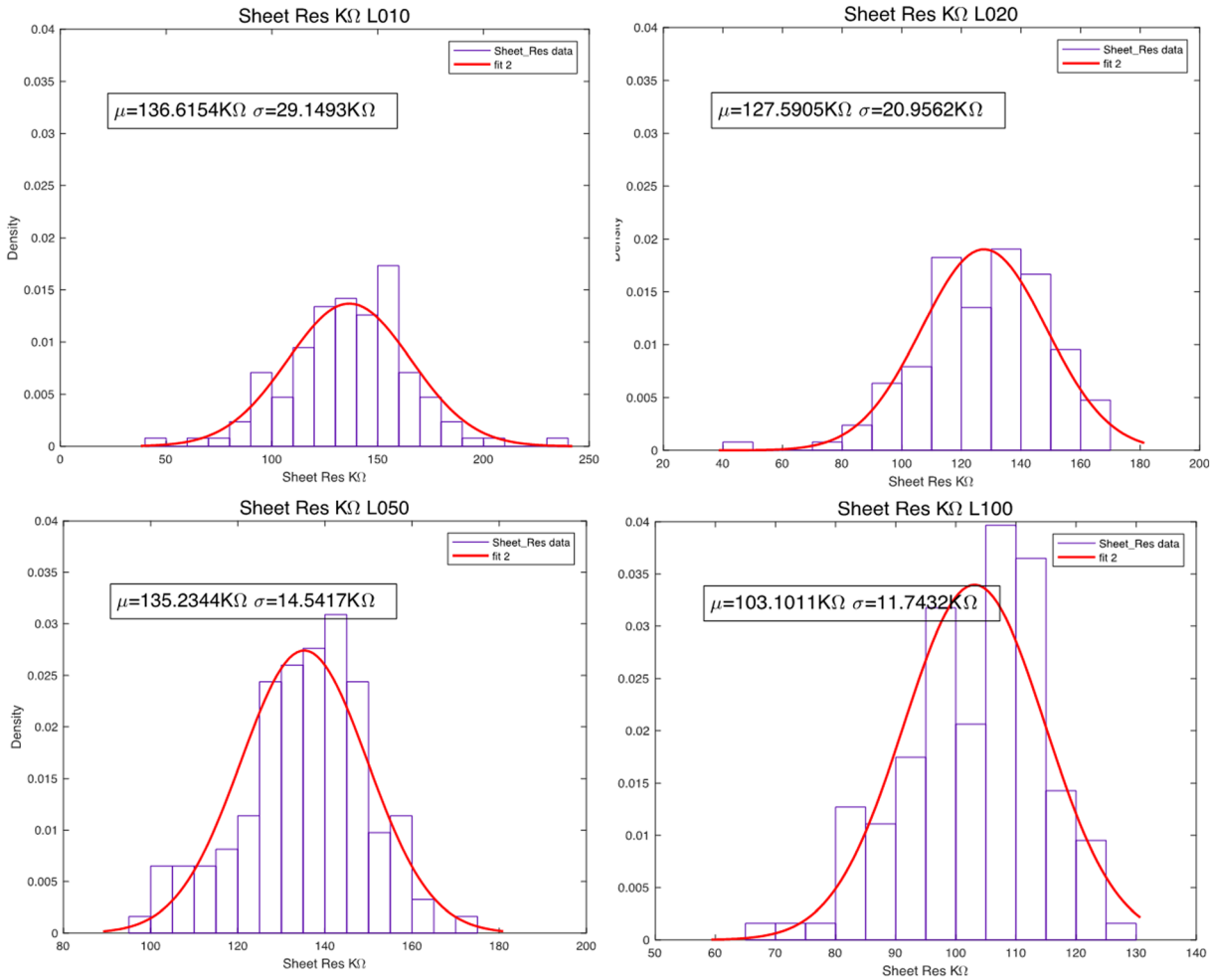

FIGURE 4 Measured statistical histograms of CNT resistors for resistor lengths from 10 to 100 μm, and the resistor width is fixed to 40 μm

realize the flexile capacitors with 25 nm thick Al_2O_3 dielectrics as shown in Figure 2. To further study the process variations of the capacitance, we designed and characterized 431 parallel-pate capacitors, and the measurement results of the unit capacitance, ie, capacitance per unit area can be found in Figure 5 for the capacitor widths W_C ranging from 45 to 1415 μm. We can learn that while the standard deviations of the unit capacitance (approximately 3 fF/μm^2) are similar among different capacitor widths W_C, the average unit capacitance increases with larger capacitor widths. We attribute this phenomenon to thinner dielectrics for larger-sized capacitors. The 2D spatial analysis in Figure 6 shows the unit capacitance variations across the same flexible substrate, using which figure we can learn that the unit capacitance is higher at the center of the substrate. This could be attributed to thinner dielectrics at the center of the substrate due to nonuniformity of the dielectrics thickness, which is often seen in solution or printing processes.

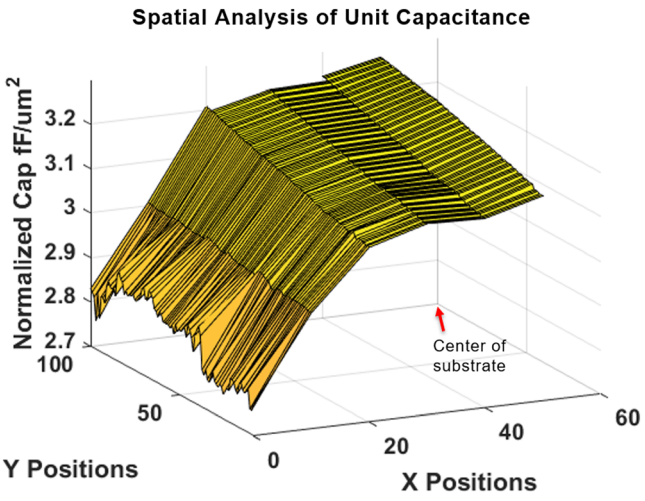

FIGURE 6 Measured 2D spatial analysis of the unit capacitance (fF/μm^2) against the substrate dimensions in millimeters (mm)

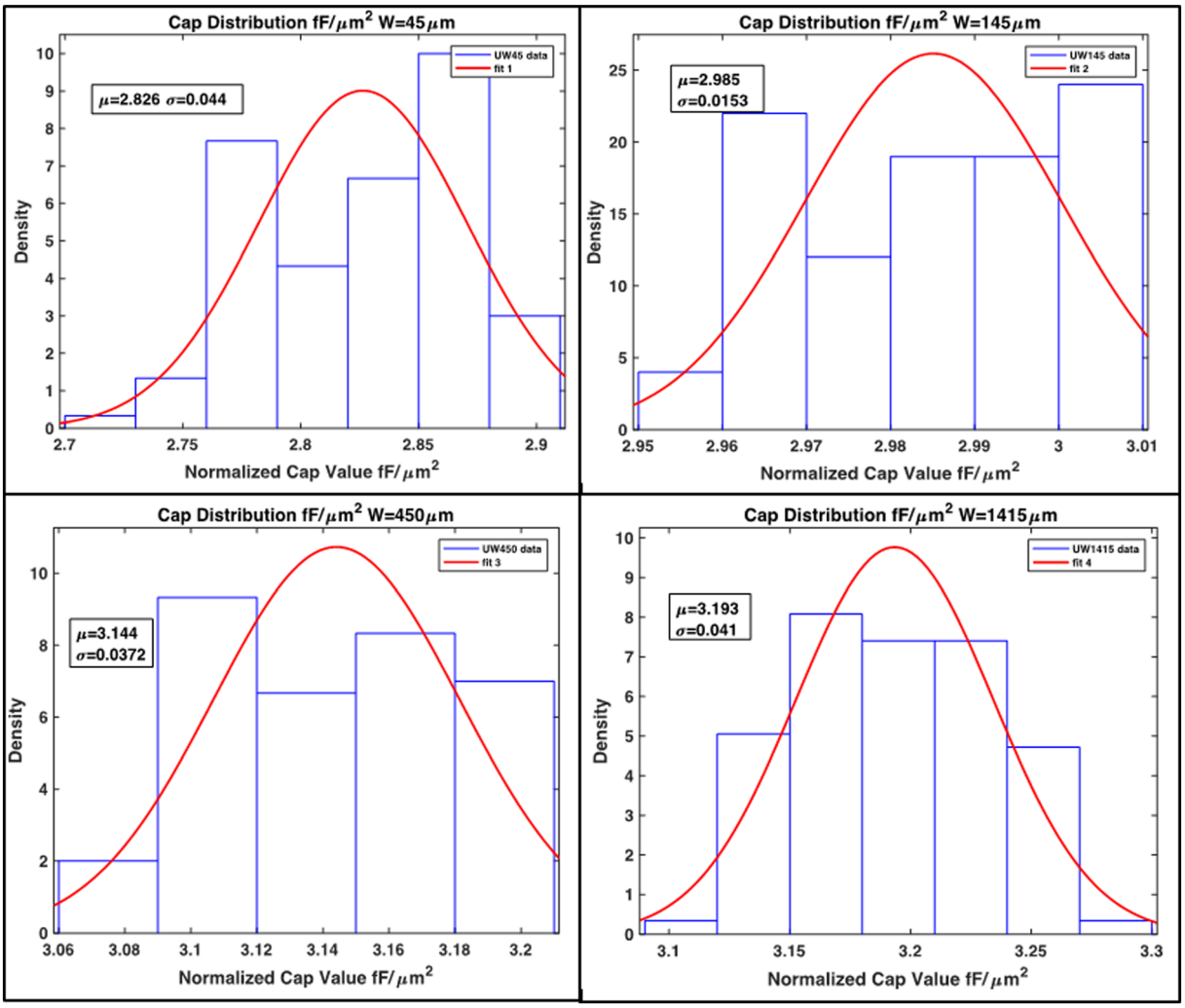

FIGURE 5 Measured statistical histograms of unit capacitance for the parallel-plate capacitors. The capacitor widths W_C are from 45 to 1415 μm

3 | DESIGN VERIFICATION AND AUTOMATION

Because of the complexity of FHE circuit and system design, it is error-prone and time-consuming without proper design aids or design automation capability. To enhance the design productivity and also reduce the design time required for designing a complex FHE system, we incorporate both silicon CMOS design, ie, IC-centric and PCB-centric design toolsets for FHE-PDK to perform system design, simulation, and physical layout verification flow. We also create experimentally proven design rules of CNT-TFTs, CNT resistors, parallel-plate capacitors using solution processes, and design rules of spiral inductors using screen printing. On the basis of these design rules, we create technology files using Standard Verification Rule Format (SVRF), which is T-cl or Python-based formats to perform physical verification using mainstream IC-centric toolsets including Mentor Graphics *Calibre*. All basic elements such as CNT transistors and parallel-plate capacitors are constructed as parameterized cells (P-cell). FHE designers therefore can simply use various P-cells as the basic elements to build functional circuits that range from a digital random pattern generator to an analog circuitry such as variable gain amplifier (VGA). The simulation models and design rules of given P-cells and design geometries are included in FHE-PDK, and designers can use FHE-PDK in the graphical user interface (GUI) design environment to perform circuit simulations and design rule checking for the physical layout of the complex FHE circuits. In addition to physical design verifications, we also incorporate material properties to create technology files for layout parasitic extraction (LPE). Layout-related parasitic in flexible circuits can be significantly larger, compared with silicon chips, which is due to larger physical footprints. Thus, it is essential to include accurate estimates of physical layout-dependent parasitics such as layout resistance and capacitance in order to perform post-layout analysis, particularly for high-performance FHE circuits.

In addition to TFT circuit-level simulations, FHE-PDK is also capable of performing system-level simulations and design rule checking for FHE system design using PCB-centric design toolsets such as Mentor Graphics *HyperLynx*.

4 | FOUNDATIONAL DESIGN IP FOR TFT CIRCUITS

4.1 | Digital logic

Complementary circuits with both p- and n-types of transistors are essential in silicon CMOS design to reduce the static power consumption and also to improve the noise margin. However, certain TFT technologies such as IGZO and amorphous silicon (a-Si:H) do not offer good complementary TFTs, which makes low-power and robust TFT digital design difficult. To overcome these design challenges such as the lack of complementary reliable TFTs, as well as large process variations for printed and solution-processed TFT circuits, we have previously reported a robust design style *Pseudo-CMOS*.[9] On the basis of *Pseudo-CMOS*, we have developed a variety of solution process–proven flexible digital logic circuit design IP blocks ranging from a simple inverter, logic gates, to linear-feedback shifter registers (LFSR) using only p-type CNT-TFTs as shown in Figure 7. Without complementary TFTs, the static noise margin of digital circuits, particularly at low supply voltages, is much

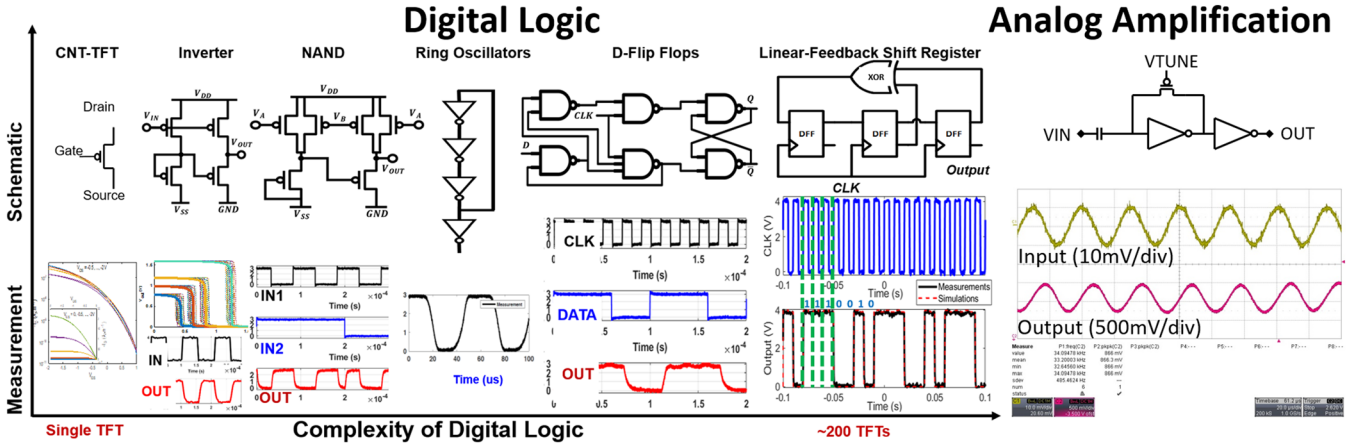

FIGURE 7 Overview of foundational TFT design intellectual property (IP) blocks using CNT-TFTs for digital logic and analog amplification

inferior to that of complementary circuits. Therefore, the signal degrades after propagating a dozen of logic gates or simple sequential circuits with multiple feedbacks. In this paper, complex sequential logic circuits such as shift registers are demonstrated using only p-type CNT-TFTs as shown in Figure 8D,F, in which shift registerthe 50 KHz clock is used as the input, and the measured output waveforms of the cascaded registers after eight stages do not show any noticeable signal degradations, even with only p-type CNT-TFTs.[3] With the aids of trustworthy simulation models and design rules developed for FHE-PDK, we can now readily design, simulate, and verify complex TFT digital logic circuits with thousands of CNT-TFTs using popular electronics design and verification tools such as Cadence *Virtuoso* and Mentor Graphics *Calibre*. The simulated TFT circuit performance and power consumption also provide a good correlation with the fabricated CNT-TFT circuits at low supply voltages (3 V). More details of model validations can be found in our previous work.[4]

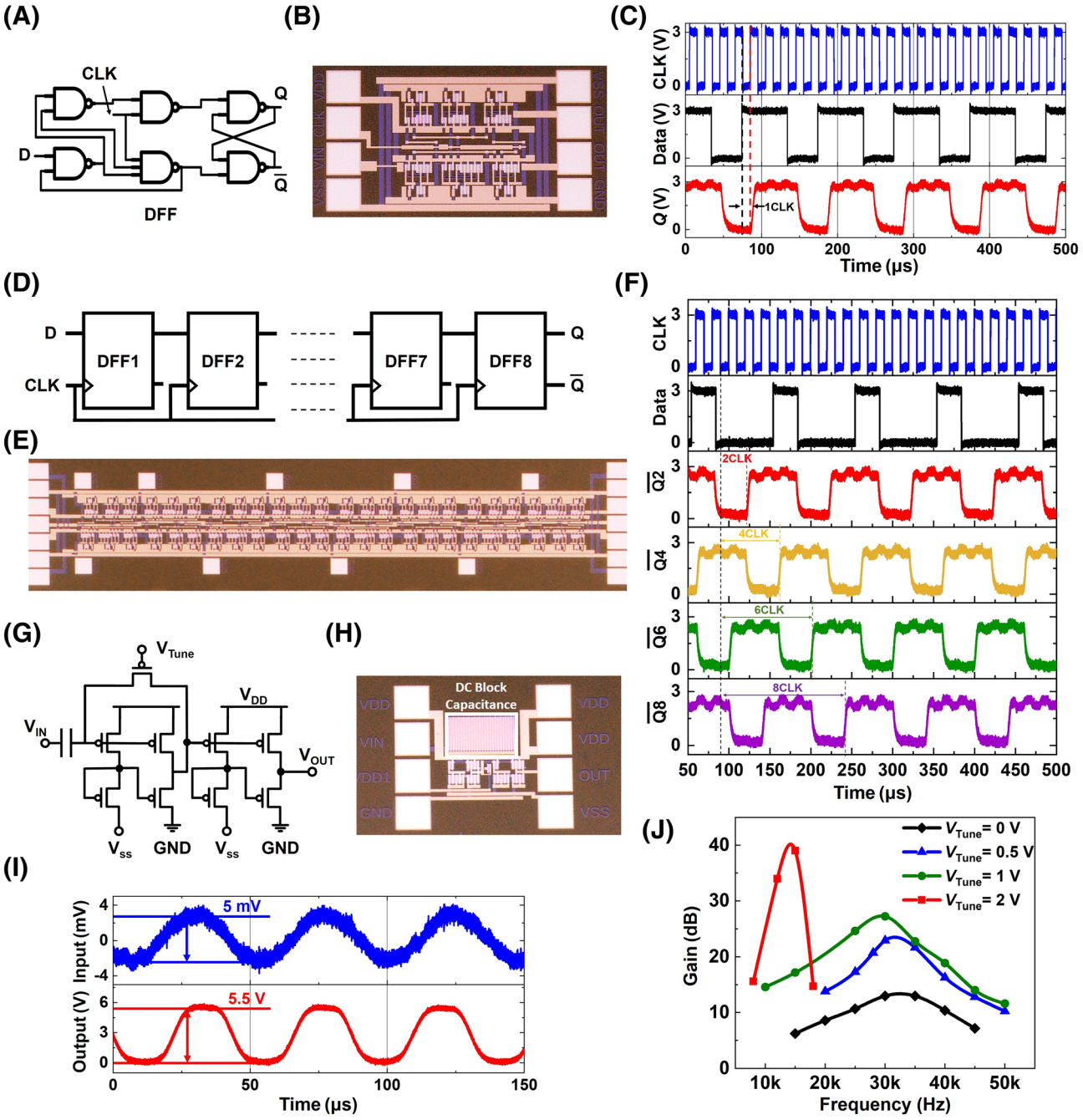

FIGURE 8 (A)-(C) *Pseudo-CMOS* flip-flop schematics and measured waveforms, (D)-(F) shift-register schematics and measured waveforms, and (G)-(J) variable gain amplifier (VGA) schematics, measured waveforms, and frequency response[3]

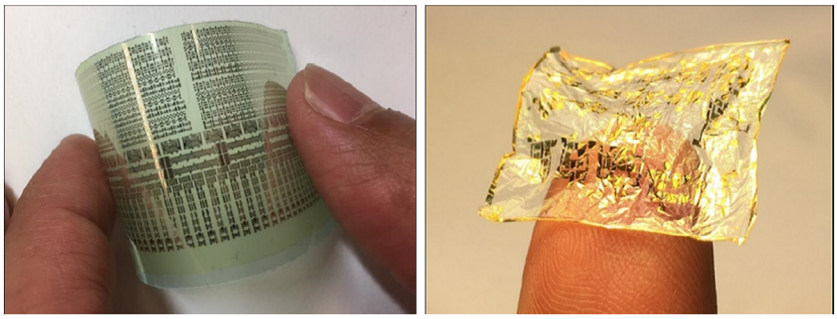

FIGURE 9 Circuit design intellectual property (IP) blocks, including *Pseudo-CMOS*[9] digital logic, analog amplifies, and passive elements (R/C). (Left) solution-processed CNT-TFT circuits on the 10-μm thick flexible substrate for bending test, and (right) CNT-TFT circuits on the 1-μm thick substrate

4.2 | Analog signal amplification

In addition to digital logic, we also develop analog circuit design IP blocks such as VGA that is commonly used in sensor interfaces for signal amplifications. The schematics and measured input-output waveforms of the 9T-1C VGA is shown in Figures 7 and 8. The voltage gain of the VGA is tunable by varying the gate voltage VTUNE of the feedback TFT. The physical size of the 9T-1C amplifier has a compact footprint of 350 × 350 μm^2 including a parallel-plate input capacitor to attenuate low-frequency input noises and block the dc current feedback to the input terminal. The gain-bandwidth of the VGA can then be fine-tuned by varying VTUNE voltages, and the measured frequency responses of VGA with different VTUNE voltages are shown in Figure 8J. The minimum input range is 5 mV, and the measured waveforms are shown in Figure 8I. The physical samples of *Pseudo-CMOS* digital and analog circuits with CNT-TFTs are shown in Figure 9.

5 | CONCLUSION

In this paper, we report our latest development and overview of FHE-PDK as the design aids for FHE circuit and system design, simulation, and physical verification. While FHE is emerging as a viable solution for high-performance and low-cost IoT and wearable applications, the device models, design rules, and technology files are still missing today to enable the codesign and cosimulations of flexible TFT circuits and thinned silicon chips. FHE-PDK aims to fill these gaps in FHE design by incorporating experimentally validated device models, design rules, technology files, P-cells, and open-source digital and analog design IP blocks for flexible circuits. We believe that FHE-PDK will emerge as the must-have toolbox for FHE circuit and system designers.

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