# **Development of Upstream Tracker using MAPS for LHCb Upgrade II**



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# ICHEP 2024 PRAGUE

The 42<sup>nd</sup> International Conference on High Energy Physics, 17-24 July 2024, Prague

# LHCb Upgrade II

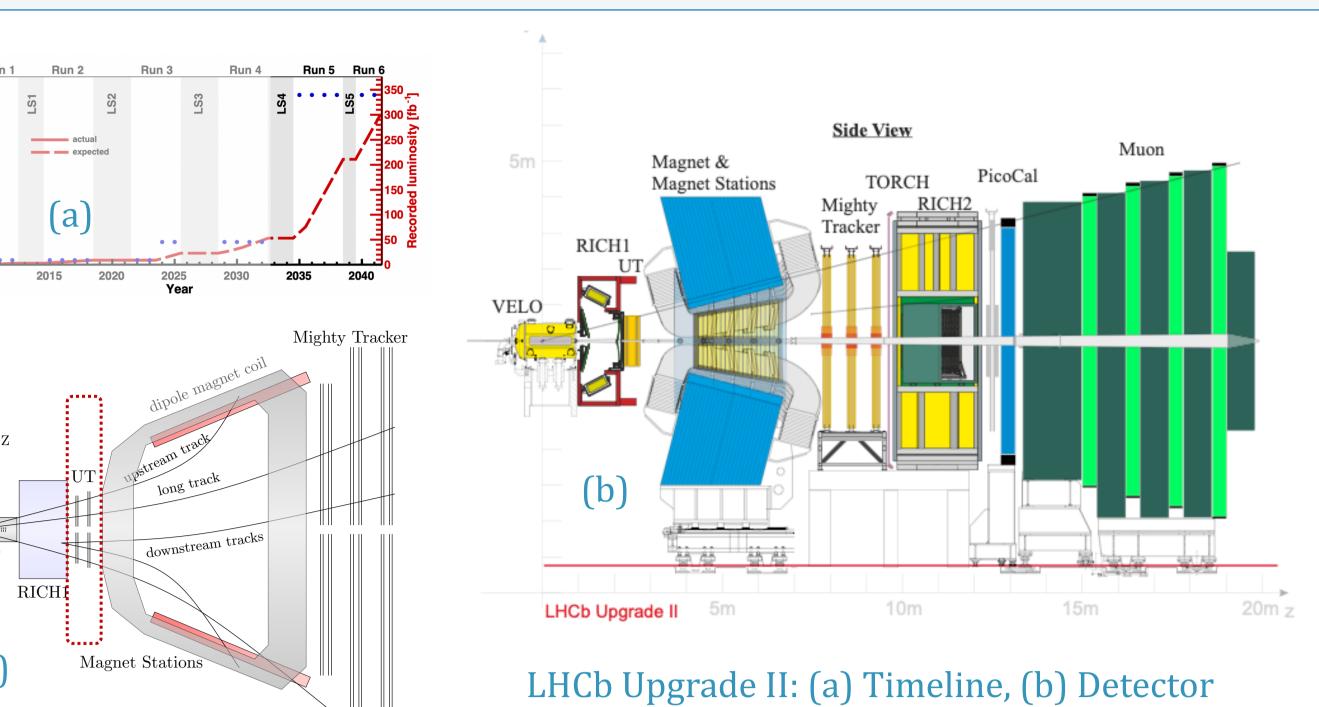
LHCb is a single-armed forward spectrometer at the Large Hadron Collider. To fully exploit the flavour physics potential at the High-Lumi LHC, LHCb is planning a major upgrade (Upgrade II) in the long-shutdown 4, to achieve:

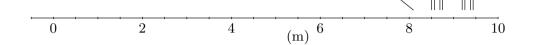
- Instantaneous luminosity of  $1.5 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$
- An integrated luminosity of  $\sim 300 \text{ fb}^{-1}$  in the whole LHC lifetime
- Fully software-based trigger system

Upstream Tracker (UT) is a key component of the tracking system, located upstream of the magnet, playing important roles:

- Reducing false matching between VELO and T-station segments
- Speeding up real-time reconstruction of long tracks
- Ensuring reconstruction efficiency of long-lived particles like  $K_S$  and  $\Lambda$

Current UT, based on silicon strip detectors, will not be able to operate under the Upgrade II condition, and has to be upgraded with high-granularity, radiation-hard technology, and MAPS is a most promising technology option.



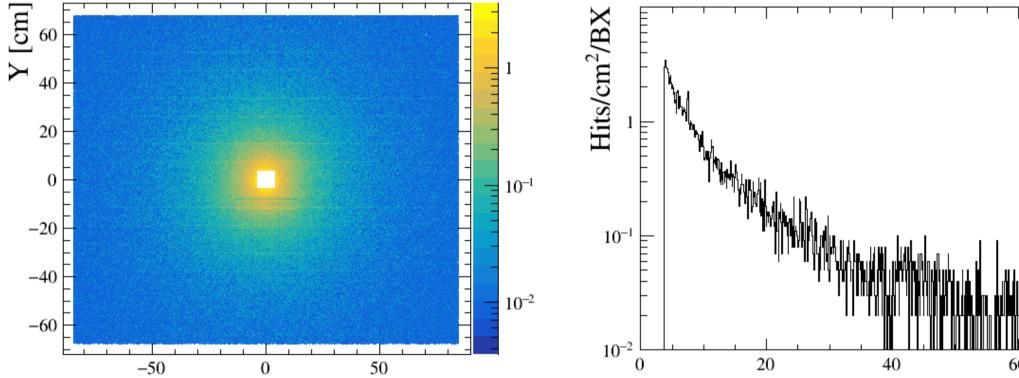


layout and (c) Tracking system configuration

### UT upgrade requirements

The CMOS sensors considered UT in Upgrade II must for provide good spatial resolution, especially in x-direction; it should has good timing resolution to tag the 25ns HL-LHC bunches. The sensor and electronics should be able to endure a maximum fluence of  $3 \times 10^{15} n_{eq} \text{ cm}^{-2}$ .

Characteristics	Specification		
Hit density	~6 hits/cm²/BX		
Time resolution	O(1ns) for BX tagging		
Pixel size	$30 \times 30 \mu m^2$ or $50 \times 150 \mu m^2$		
Power	$100 \sim 300 \text{ mW/cm}^2$		
Radiation	$3 \times 10^{15} n_{eq}$ cm <sup>-2</sup> , 240MRad		

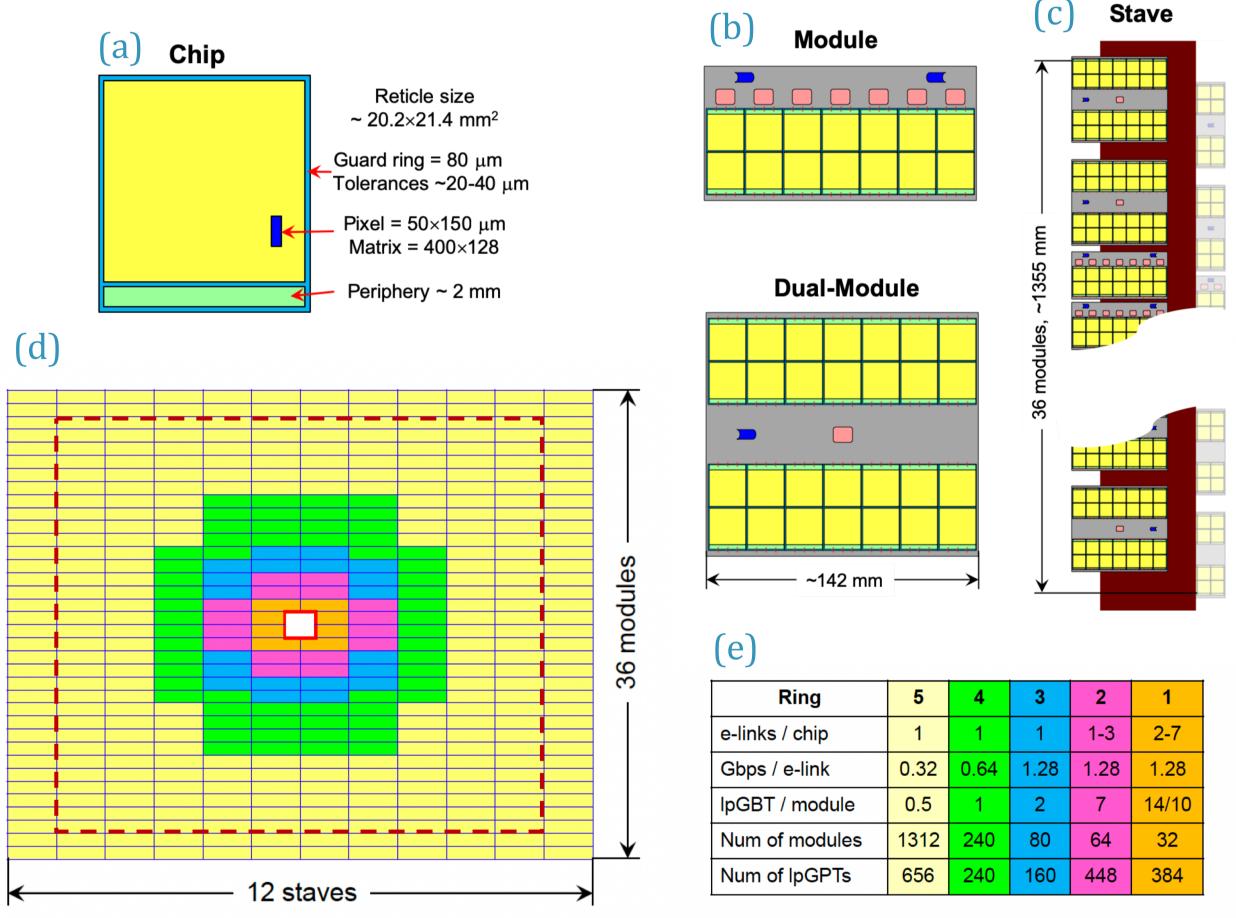


## System design and layout

The U2UT detector has 4 detector planes, at z-positions similar to current UT

- Each plane consists of 12 staves, each has 36 modules mounted on both sides
- Assuming  $2 \times 2$  cm<sup>2</sup> chip size, a module has 14 or 28 chips for optimal use of lpGBT links; optical conversion on the modules

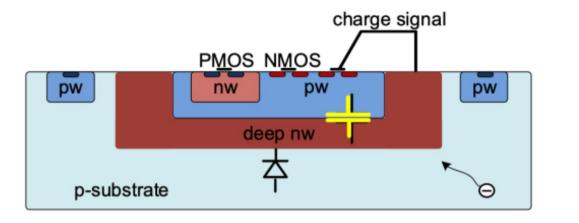
Updated baseline considers reducing coverage in the outermost region for cost reduction with minimal impact on physics.



#### Y [cm] X [cm] Hit density during proton-proton collision at a UT plane in Upgrade II condition

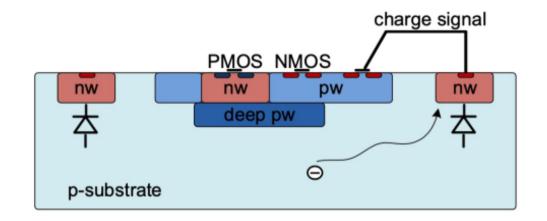
# CMOS sensor options

### Two approaches are being pursued for sensor development:



### High-Voltage CMOS

- Circuitry inside collection well
- Intrinsically radiation hard
- Uniform electric field
- Fast charge collection
- Existing chip like ATLASPix3 in TSI 180nm process shows performance close to demand



### CMOS with small electrode

- Small capacitance, low noise and low power consumption
- Radiation hardness with process modification
- Many successful prototypes chips like MATLA for other applications

### Technology options considered

### AMS 180nm / LFoundry 150nm

MightyPix under development for Mighty Tracker (MT), synergy with UT expected. Note that MightyPix is aimed for a lower radiation level.

### *TowerJazz 180nm*

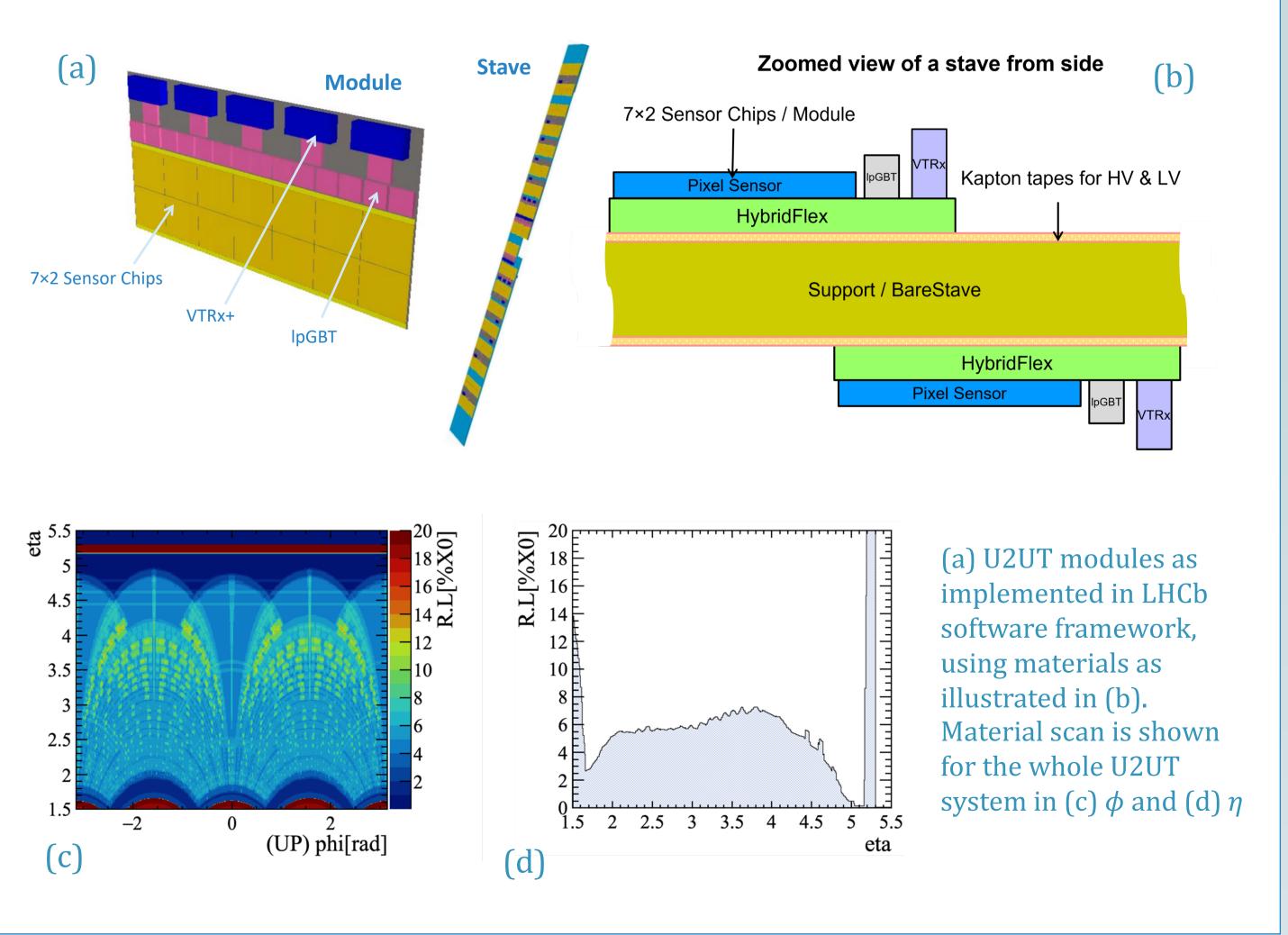
Based on MALTA3 chip, development of LHCb-oriented readout periphery needed to cope with the high data rate.

(e)					
Ring	5	4	3	2	1
e-links / chip	1	1	1	1-3	2-7
Gbps / e-link	0.32	0.64	1.28	1.28	1.28
lpGBT / module	0.5	1	2	7	14/10
Num of modules	1312	240	80	64	32
Num of lpGPTs	656	240	160	448	384

A preliminary design of the U2UT system: (a) chip size, (b) single and dualmodule, (c) a stave, (d) layout of a plane. Each box corresponds to a 2×7-chip module; the colour code corresponds to modules with different number of electronics components such as lpGBTs as listed in (e). The red dashed line indicate updated baseline with reduced coverage.

# Detector modeling and simulation

The detector description has been implemented in the LHCb software framework, with realistic material assuming carbon dioxide cooling as in current UT.



#### SMIC 55nm

COFFEE prototypes developed to validate the process. COFFEE1 response to laser signal observed. COFFEE2 chip, on  $1k\Omega$  cm high-res substrate, shows a break-down voltage up to -70V.

### TPSCo 65nm

Design of SPARC prototype on development of digitial blocks of readout periphery in TPSCo 65nm ongoing. Submission planned in 2024.

#### (a) Laser signal at COFFEE1; (b) IV curve at COFFEE2; Photos of (c) COFFEE1 and (d) COFFEE2

